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Faculté des Sciences et de la Technologie
Département de Génie Electrique
Filière : Electronique
Option : Microélectronique

Réf:.....

Mémoire de Fin d'Etudes
En vue de l'obtention du diplôme:

MASTER

Thème

Conception d'un amplificateur faible bruit
Design of Low Noise Amplifier (LNA)

Présenté par :
BEN AMOR Zakaria
Soutenu le : 29 Juin 2013

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Avis favorable du Président du Jury

BEKHOUCHE Khaled ***Signature***

Cachet et signature

Acknowledgment

Firstly, I thank **Allah**, the Most High, for the opportunity He gave me to study, to research and to write this dissertation. **Thank Allah,** my outmost thanks, for giving me the ability, the strength, attitude and motivation through this research and to complete this work.

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List of abbreviation

2DEG	Two dimensional electron gas
AC	Alternative Current
ADS	System of Agilent Advanced Design System
AlAs	Arsenuire of aluminum
AlGaAs	Aluminum gallium arsenid
AsGa	arsenuire of gallium
CMOS	Complementary Metal oxide semi-conductor
DC	Direct current
dB	Decibels
EE-HEMT	Model of transistor HEMT non-linear
E_f	Fermi level
Ec	Conduction band
Ev	Valence band
Eg	Gap of energy
ε_r	The constant dielectric of materials
G_m	Transconductance
G_d	The conductor of drain
g_d	The Output conductor
HEMT	High electron mobility Transistor
HMIC	Hybrid microwave integrated circuits
h	Thickness of substrate
InP	Phosphor indium
InAs	Arsenuir indium
InGaAs	Indium gallium arsenide
K	Factor of Rollet
LNA	Low Noise Amplifier
Lg, Ls, Ld	Inductors parasites of gate, source, drain
MBE	Molecular Beam Epitaxy
MESFET	Metal Semi-conductor Field Effect Transistor

MMIC	Microwave Monolithic Integrated Circuit
NF	Noise Figure
NFmin	Noise figure minimal
pHEMT	Pseudomorphique High Electron Mobility Transistor
RF	Radiofrequency
Si	Silicium
S11	The coefficient reflexion input
S12	The coefficient transmitter direct
S21	The coefficient transmitter inverse
S22	The coefficient reflexion output
SKA	Square Kilometre Array
Γ_{opt}	The coefficient reflexion optimal of noise
t	The thickness of conductor
Γ_s	The coefficient reflexion output
Γ_{in}	The coefficient reflexion input
Vp	Tension pincement
Vgs	Tension gate-source
Vds	Tension drain-source
w	Weight, Unit Measures.
WLAN	Wireless Local Area Network.
Y	admittance.
Z_c	Impedance caracteristique.

Abstract

In the last twenty-first century reached to the latest technology innovation in the field of electronics and small size it to farther limits border in designing integrated circuits with transistors high composition by Semiconductors InP and GaAs.

Has been reached transistor design from through a change in its physical by several measurements to input signals are weak and re-measured it in the output.

We was designed two circuits Low noise amplifier by transistor pHEMT_A043_800µm. the first circuit is source common cascode, the result was the high gain of 47dB and noise figure of 0.68 dB. On the other hand the second circuit composed from three stages cascade by 38.5dB and figure noise 0.7dB.

Résumé

Au cours des dernières années, un progrès a été réalisé avec succès dans le domaine de l'électronique, la miniaturisation des composants, la conception et la mise en œuvre MMIC employant les semi-conducteurs composés. Une des applications les plus excitants de cette technologie est le Array (SKA) radiotélescope kilomètre carré. L'objectif principal de ce travail est la conception d'un MMIC InP-pHEMT large bande LNA, dans la bande L avec le niveau de bruit le plus bas possible et que la réponse de gain plat possible.
Dans ce travail, nous discutons de la conception de deux amplificateurs à faible bruit (LNA) sur la base d'un transistor de 1 µm de large de la grille, et de large 200 µm sur InP à l'aide de deux topologies.

Le premier circuit est composé de deux phases (phase de source commune en cascade avec cascode topologie, le résultat a été le gain élevé de 47 dB et figure de bruit de 0,68 dB. D'autre part, le second est un amplificateur en cascade à deux étages avec 38.5dB et la figure 0,7 dB de bruit.

ملخص

في آخر القرن الواحد والعشرين توصلت التكنولوجيا إلى أحدث الابتكارات في مجال الإلكترونيات وتصغير حجمها لأبعد الحدود في تصميم دوائر متكاملة ذات ترانزستورات عالية التركيبة وذلك بأشباه الموصلات InP و GaAs

تم الوصول إلى تصميم ترانزيستور من خلال تغيير في خصائصه الفيزيائية بواسطة عدة قياسات من إدخال إشارات ضعيفة وإعادة قياسها في المخرج.

عملنا دارتين من أجل تقديم مكبر خافض الضجيج وذلك بإستعمال ترانزستور pHEMT_A043_800µm . الدارة الأولى عبارة عن منبعين مشتركين تسلسلا. فكانت النتيجة بأعلى كسب يقدر بـ: 47 ديسيبل وعامل الضجيج 0.68 ديسيبل. أما الدارة الثانية مكونة من ثلاث طوابق فكانت النتيجة بكسب 38.5 ديسيبل وعامل ضجيج 0.7 ديسيبل.

General Introduction

Technological advances in integrated microwave circuits are the key to open and to fully exploit the new market opportunities, as we have seen in the last decade with the explosion of mobile telecommunications like wireless internet networks, Bluetooth and mobile phone. And they have developed through advances in transistors and performance components based III-V Gallium Arsenide (GaAs) or indium phosphide (InP) used because they present better performance in.

The global stress and tension resulted in particular increase the speed of search in semiconductor components or low noise amplifier and the need for supplements minimize its size , allowing the emergence of new systems high-quality and low cost and small size.

It has been reached to use of microwave monolothiques circuits (MMIC), component by High electron mobility transistor (HEMT) and Heterojunction Bipolar Transistor (HBT). These components are the base of MMICs allows applications to very high frequencies.

The transistor HEMT the more sales today in high frequency especially in fabrication, the amplifier low noise, wideband signals, Radar, communications satellite and mobile phone. when the evolution of pseudomorphique (pHEMT) to amplification the power of another area or outstanding performance were obtained, especially at millimeter frequencies.

The work will present a design of a low noise amplifier using heterojunction field effect transistor-type HEMT or pHEMT be one of the assets base of a MMIC for radio astronomy applications.

The terms of this thesis consists of three Chapters:

In the first chapter , the HEMT and pHEMT their operation and structure are studied, and the different noise sources and origins in the semiconductor components.

In the second chapter . we will focus on the design methodology of microwave monolithic integrated circuits and their applications, the advantages and disadvantage of MMICs with the hybrids.

In the last chapter, we designed a work on two amplifiers LNAs exposed the first a cascode cells and other structure in the 0.4-1.9 GHz band, three-stage cascaded topology based on a transistor pHEMT_A043_800µm.

FIRST CHAPTER

THE FIELD EFFECT TRANSISTORS TO HETEROJONCUTION

I.1 Introduction

A large variety of electronic devices (such as diodes, transistors, mixers, attenuators, and photo-detectors, to name a few) are based on the unique electrical conducting properties of semiconductors. Semiconductors are solid-state conductors whose electrical conductivity ranges approximately between 10^{2} and 10^{-9} mho per centimeter (mho/cm) (or its inverse, resistivity between 10^{2} and 10^{-9} ohm-cm) at room temperature. These conductivities are higher than an insulator's but lower than a metal's. Although most pure single-crystal semiconductors are insulators at absolute zero with conductivities less than 10^{-14} mho/cm, it is impurities and imperfections that allow manipulation of semiconductor's device properties. In fact, it is the ability to precisely engineer and finely tune a semiconductor's conductivity at the atomic layer level that is essential to the production of state-of-the-art high electron mobility transistor (HEMT) devices.

Important semiconductors like silicon (Si), germanium (Ge), gallium arsenide (GaAs), indium phosphide (InP) and their ternary derivatives, like aluminum gallium arsenide (AlGaAs), indium gallium arsenide (InGaAs), and indium aluminum arsenide (InAlAs), form a crystalline diamond (or zincblende) lattice structure bonded by covalent forces. Each atom has four nearest neighbors lying at the corners of a tetrahedron, and it shares an electron with each atom. The covalent attractive potential between atoms is created by the shared electron pairs of opposite spin [1].

I.2 Charge carrier and energy band gap

Semiconductors can have two types of charge carriers that contribute to the conductivity, electrons and holes. In pure intrinsic semiconductors at room temperature, thermal energy can free an electron (negative charge) from its bonding or lattice site, leaving behind a vacant positively ionized atom. The vacancy is called a hole, and is equivalent to a charge carrier of positive charge moving in a direction opposite to the electron's motion. Unlike electrons in free space, which have a continuous set of energy states, electrons in a solid have forbidden bands of energy. At low energies electrons in a solid behave much like free, classical electrons. However, as the electron energy increases, they interact with and are

scattered by the lattice, exhibiting their wave nature. This occurs at energies where the electron's de Broglie wavelength,

$$\lambda = h/p \qquad \text{(Equ.I.1)}$$

h: Planck's constant

p: electron momentum

Approaches the inter-atomic spacing, a, producing a band of forbidden energy states. A graphical representation for the electron energy as a function of wave vector ($k = 2\pi/\lambda$) for an ideal one-dimensional solid is shown in Fig I.1.

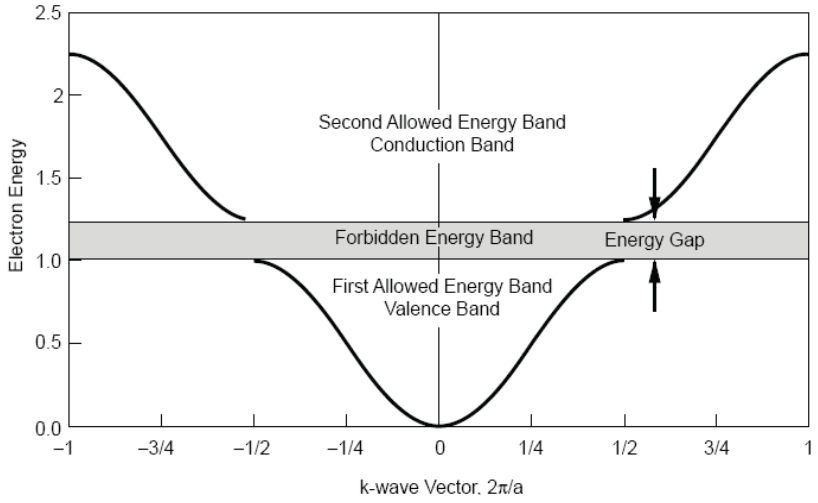

Figure I.1: Electron energy plotted as a function of wave-vector k ($2\pi/a$) for an electron in a one-dimensional solid of lattice constant a showing the energy gap.

$$m^* = h^2 \left(\frac{\partial^2 E}{\partial k^2} \right)^{-1} \qquad \text{(Equ.I.2)}$$

Thus for large values of $\delta^2 E / \delta k^2$, m^* can be much less than the free electron mass. In addition, below room temperature the electron mobility is approximately inversely proportional to the product of the effective mass and physical temperature, that is $\mu e \propto (m^* T)^{-1}$. While the electron velocity is in turn proportional to the product of the electron mobility and applied electric field,

$$\mathbf{v} = \mu_e \varepsilon \qquad \text{(Equ.I.3)}$$

Although silicon is the dominant material in use today for the manufacture of transistors and is the most mature technology, the III–V semiconductor compounds have far superior transport properties, especially at high frequencies and low temperatures. In fact, the m^* of GaAs and InP is less than an order of magnitude smaller than Si's, and their μ_e's are more than two orders of magnitude greater than Si's at liquid nitrogen temperatures (77 K). In fact, the maximum intrinsic frequency of operation for a HEMT device is directly proportional to the electron velocity. Listed in Table I.1 for comparison is the band gap energy (Eg), electron mobility (μ_e), peak velocity (v_p), and lattice constant (a) for a number of important semiconductors [2].

Semiconductor	E_g (eV)	μ_e (cm^2/Vs)	v_p (10^7cm/s)	a (Å)	a (nm)
Ge	0.66	3900	0.6	5.65	0.565
Si	1.12	1500	1.0	5.43	0.543
GaAs	1.42	8500	1.8	5.65	0.565
InP	1.35	4600	2.4	5.87	0.587
$Ga_{0.15}$ $In_{0.85}As$	1.20	9500	2.9	5.85	0.585
$Ga_{0.47}$ $In_{0.53}As$	0.75	15,000	3.4	5.85	0.585
InAs	0.36	33,000	4.4	6.06	0.606
InSb	0.17	80,000	5.0	6.48	0.648

Table I.1: Electronic properties of important semiconductors at room temperature [2].

I.3 Heterojunction HEMT versus MESFET

Until the invention of the HEMT, the most widely used III–V transistor for both microwave and high-speed digital applications was the GaAs metal semiconductor field effect transistor (MESFET). However, since electrons must transit through the doped channel in a MESFET, it does not take full advantage of the high mobilities in GaAs. The result is more than a 50-percent reduction in electron mobility, since ionized dopants scatter electrons. Hence, separation of the dopant channel from the electron transit channel is key to the superior noise, gain and frequency performance of the HEMT. For comparison, the cross sections of a GaAs HEMT and a MESFET are shown in Fig. I.2 and a comparison of their material properties are shown in Table I.2.

The model HEMT structure can be formed of two distinct semiconductor layers. The bandgap difference results in the formation of conduction and valence band discontinuities at the layer interface or heterojunction creating a quantum well in the conduction band. The wider band gap semiconductor is

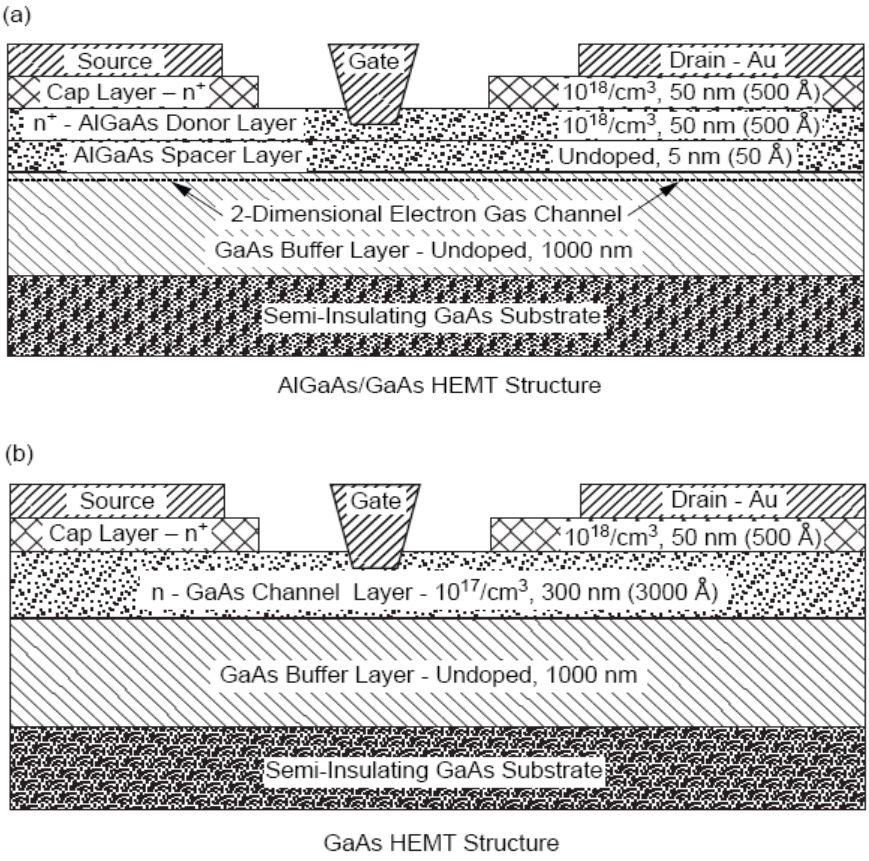

Figure I.2: Cross sectional diagrams comparing structures of an (a) AlGaAs/GaAs HEMT and a (b) GaAs MESFET [2].

Material Properties	HEMT	MESFET
Sheet charge density ($1/cm^3$)	10^{18}	10^{17}
300-K electron mobility ($cm^2/V\text{-}s$)	8,500	4,000
77-K electron mobility ($cm^2/V\text{-}s$)	80,000	6,000

* Assume a spacer thickness of 5 nm (50 Å)

Table I.2: Material properties of conventional HEMT and GaAs MESFET structures.

I.4 HEMT materials evolution—from GaAs to InAs

As previously mentioned, the first successful HEMTs were based on the lattice-matched heterostructure AlGaAs/GaAs. A few years later, In was added to the carrier channel to improve device performance, that is, to increase electron mobility (Γe), increase the frequency of operation and lower the noise.

The InGaAs channel layer inserted between the AlGaAs and GaAs is not lattice matched to either compound, GaAs or AlGaAs, but compressed to match them at their interface; accounting for the device name, pseudomorphic HEMT (PHEMT). The thickness of the InGaAs layer (between 50 to 200 Å [5–20 nm], depending on In concentration) is chosen so that most of the compressional strain is taken up by the InGaAs layer. To further push device performance, the In concentration was increased from the range of 15–20 percent to 65 percent, the spacer material changed to InAlAs, and InP substrates used to accommodate the larger lattice mismatch. Pure InAs as the carrier channel is currently being investigated as the next logical step to produce the ultimate in HEMT device performance. The advantage of this material is the high electron mobility (30,000 cm2/Vs at 300 K) and velocity (4 x 10^7 cm/s) and a large conduction band offset between InAs and AlSb (1.35 eV) Although the layer number, composition, and thickness vary depending on the desired properties, all HEMT layer structures have the same essential feature, a vertical heterojunction. The heterojunction spatially separates charge carriers from donors and confines them to the channel layer where the electron momentum is quantized in the "vertical" direction but is continuous in the horizontal direction. In the following discussion, the design guidelines for an optimal low noise AlGaAs/GaAs HEMT device are given, then a summary and comparison is presented of some of the essential enhancing features of PHEMTs and lattice-matched InP HEMTs [3].

I.5 The GaAs pseudomorphic HEMT—A1GaAs/InGaAs/GaAs PHEMT

In 1986 the GaAs pseudomorphic HEMT was introduced as a high performance alternative to the AlGaAs/GaAs HEMT. Substitution of InGaAs for GaAs as the two-dimensional electron gas channel improves transport properties due to the higher mobility of InGaAs and stronger electron confinement associated with the quantum well at the heterojunction. Thus, injection of electrons back into the AlGaAs from the InGaAs is significantly reduced; thereby improving the transport properties. The larger conduction band discontinuity at the

AlGaAs/InGaAs heterojunction allows a higher sheet charge density and hence a higher current density and transconductance.

Additionally, the electron mobility and peak velocity can be further improved by increasing the indium concentration (Fig.I.3). The room temperature mobility of this type of PHEMT structure is generally 5000 to 7000 cm^2/Vs with a 2-DEG concentration of 1–3 x 10^{12} cm^{-2}. Although InGaAs is not lattice matched to either the AlGaAs donor or the GaAs buffer layers (Fig. I.3), the strain associated with the lattice mismatch can be elastically accommodated within the InGaAs layer. For example, for a PHEMT structure like AlGaAs / $In_xGa_{1-x}As$ / GaAs where x is in the range of 0.15 to 0.20, the InGaAs layer must be smaller than the critical thickness ~150 Å (15 nm) . Above the critical thickness, lattice dislocations form, while for a thickness less than ~ 50 Å

(5 nm), quantum size effects substantially reduce electron confinement and increase electron scattering.

In 1990 the state-of-the-art performance for a 0.1 μm gate length device PHEMT was an f_{max} of 290 GHz, an f_T of 130 GHz, and a minimum noise figure of 2.1 dB with an associated gain of 6.3 dB at 94 GHz.

Pseudomorphic technology is quite mature, and microwave monolithic integrated circuits (MMICs) based on this type of material are common and routinely exceed this performance [6].

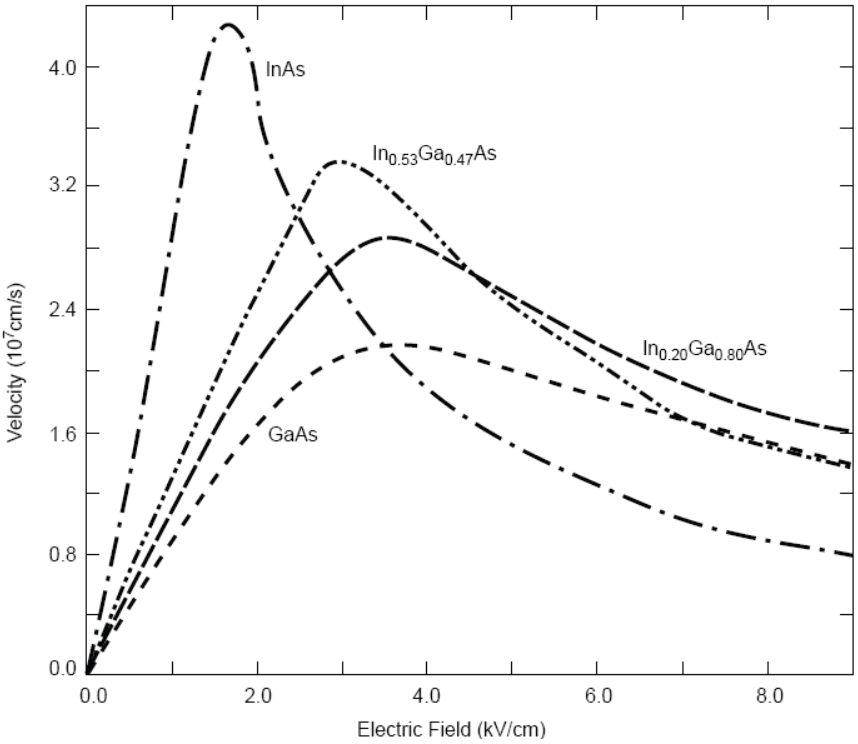

Figure I.3: Electron velocity as a function of electric field for variety of In concentrations of InGaAs.

I.6 Device fabrication

This section outlines the major processing steps in the fabrication of HEMT devices and microwave monolithic integrated circuits (MMICs). These processing steps are mostly based on, and hence quite similar, to GaAs MESFET processing. The major steps following growth of the heterostructure material are surface preparation and cleaning, front-side processing, and backside processing. Front-side processing steps include mesa or device isolation, ohmic contact formation, gate formation, metallization, and device passivation, while back-side processing includes substrate thinning via-hole formation and dicing. The processes are all performed in a clean room environment, varying in grade from Class 10,000 for the least critical steps of wafer preparation to Class 100 for the most critical steps, such as ohmic contact and gate formation [7].

I.6.1 Wafer preparation and cleaning

To maintain optimum fabrication conditions and insure high device yields, cleaning operations are performed before all major steps during device processing. Relatively benign solvents, acids, bases, and rinses are used to remove contaminants such as organic materials, metals, and oxides. For example, organic solvents effectively remove oil, grease, wax, photo resist, and electron-beam resist without affecting the HEMT device and circuit materials.

The most common cleaning method is to immerse and agitate the wafer in the heated solvent. Solvents are then removed with alcohol that is, in turn, rinsed off with filtered, de-ionized water. Acids are used for the wet etch removal of III–V semiconductor material as well as the removal of metal and oxide contaminants. The presence of thin interfacial dielectric layers, such as oxides, cause poor ohmic contact and Schottky barrier formation. These oxides can be dissolved with wet bases or removed with plasma etching techniques. Following cleaning and rinsing, the wafer is carefully dried to avoid leaving solvents or water stains[8].

1.6.2 "Hybrid" Lithography

To achieve high speed, low noise temperature, and high power-added efficiency at high frequencies, HEMTs require very short gate lengths. The intrinsic maximum frequency of operation, $f_{\max}$, is the figure of merit used to evaluate HEMT performance which is given by

$$f_{\max} = \frac{v_e}{2\pi L_g} \qquad \text{(Equ.I.3)}$$

where v_e is the electron velocity and Lg is gate length. Fabricating very short gates is a challenge that requires well-developed lithography and pattern transfer techniques.

Masks for the lithography of HEMTs are fabricated using a combination of electron beam lithography (EBL) and photolithography. Although directwrite EBL is a low throughput exposure process, it facilitates accurate definition and alignment of sub-micron geometries while providing flexibility and fast turnaround for design iterations. EBL is widely and routinely used to produce gate dimensions of less than 0.25 µm. To improve the wafer exposure throughput, optical lithography is used for the coarse features (>1µm or 1000 nm), and the direct EBL is used only for the very short gates. This hybrid lithography has the advantage of both the high throughput of optical lithography and the high resolution and

accuracy of EBL. The hybrid lithography scheme is also used for HEMT-based MMICs requiring sub-micron gates.

1.6.2.1 Frontside processing—device isolation or mesa formation.

The devices are isolated from each other by selective etching of doped layers down to the buffer layer or all the way to the substrate. The isolation process involves a number of steps that include resist deposition, photolithographic exposure, development, semiconductor etching, and resist strip and cleaning. The etching results in formation of isolated islands of conducting epitaxial layers or mesas that are surrounded by semi-insulating buffer or substrate material. Device isolation is checked with a simple direct current measurement.

This process also reduces the parasitic capacitances and back-gating, and it provides an insulating surface for MMIC passive components.

1.6.2.2 Ohmic contact formation

Since HEMTs are large-current and smallvoltage devices, the saturation voltage and transcon-ductance are very sensitive to the contact resistance. It is essential that extremely low contact resistances be formed to the 2-DEG that is situated approximately 300–1000 Å (30–100 nm) below the surface to fully utilize the HEMT's potential.

After mesa formation, the ohmic contact areas are patterned using lithographic techniques and then metallized. Ohmic contact areas are either alloyed or non-alloyed. The goal is to dope the surface of the semiconductor sufficiently high to assure that the dominant conduction mechanism between the contact metal and the semiconductor is field emission.

For non-alloyed contacts, a metal can be deposited directly on the ohmic area. To obtain good non-alloyed ohmic contacts, a very heavily doped Ge layer or low-band-gap material such as InGaAs is usually used for the capping layer.

The most commonly used elements for alloyed contacts are a judicious combination of gold (Au), germanium (Ge), and nickel (Ni). These are evaporated onto the patterned HEMT wafer to form ohmics for the source and drain electrodes. After removing the unwanted metal through a lift-off process (whereby the unwanted metal is lifted off by dissolving the underlying resist), the wafer is then thermally alloyed in an inert nitrogen (N2) atmosphere at a temperature between 320 and 450 deg C to form low-resistance ohmic contacts. A rapid thermal annealing (RTA) or furnace annealing technique is typically used for ohmic alloy.

The optimum ohmic surface morphology depends on the metallization composition, thicknesses, and alloy cycle. A good ohmic morphology also provides clean, sharply defined ohmic contact edges in the device channel so that the gate can be placed close to the source to minimize the source resistance [9].

I.6.2.3 Gate formation

In addition to the short gate length, a small gate resistance is essential to the fabrication of HEMTs for high-gain, low-noise, and high-power applications. The most widely used gate cross-sectional structure is the T-shaped or mushroom-shaped gate formed using a multi-layer resist technique with E-beam lithography. In this structure, the small footprint or bottom of the T defines the gate length, and the wider top of the T provides a low resistance.

A trilayer resist system, PMMA/P(MMA,MAA)/PMMA (PMMA is Poly Methyl Meth Acrylate, and the other materials are copolymers of PMMA) is used to define T-gates. The least sensitive resist is first deposited on the wafer. Then a sensitive resist is deposited, and finally, a thin, relatively insensitive resist is used to define a good lift-off mask. In addition, the trilayer resist system gives good control of the recess slot width.

Following gate lithography and resist development, the exposed HEMT channel area is recessed to achieve the desired channel current and threshold voltage prior to the gate metallization. The recess etching is performed using either a wet chemical etch or a reactive ion etching (RIE) technique. The depth to which the gate is recessed is a critical parameter to the HEMT performance. The etching is discontinued when a target source to drain current is achieved. Figure I.4 shows the T-shaped resist cavity using the trilayer resist system.

After the recess, the wafer is then metallized, and the lift-off process is performed to form the metal gates. The metal used to create a Schottky barrier must adhere to the semiconductor and possess thermal stability. The gate metal is typically composed of several metal layers to decrease resistivity. The most commonly used gate metallization layers are titanium/platinum/gold (Ti/Pt/Au), with titanium/palladium/gold (Ti/Pd/Au), titanium/molybdenum/gold (Ti/Mo/Au) and chromium//palladium/gold (Cr/Pd/Au) as possible alternative compositions. Because the gates are very small, a scanning electron microscope (SEM) is used before and after gate metallization to measure the gate dimension and inspect for defects produced during the gate-formation process.

Submicron T-gates fabricated using this technique have demonstrated excellent mechanical stability, and they also exhibit extremely low gate resistances. However, for 0.15µm or less gates, the T-gate resistance rapidly increases and becomes significant compared to the source resistance. Thus for extremely short gate lengths, a trade-off between the gate resistance and the gate length must be made. An overview of the gate formation process for FETs can be found in Weitzel's review article. Figure I.5 shows the lifted-off Tshaped gate using the PMMA/P(MMA,MAA)/PMMA trilayer resist system.

To increase the contact conductivity, to simplify bonding to the device and to add MMIC components, such as, inductors, capacitors, and transmission lines, it is necessary to add more metal. Addition of thicker metallization and higher levels of metallization requires additional processing steps such as, resist deposition, photolithographic exposure, development, thick metallization evaporation, lift-off,.. etc. Au is usually used because of its good conductivity in combination with another metal like Ti or Cr. The Ti or Cr layer, usually 200– 1000 Å (20–100 nm) thick, is applied first to provide good adhesion to the III-V semiconductor.

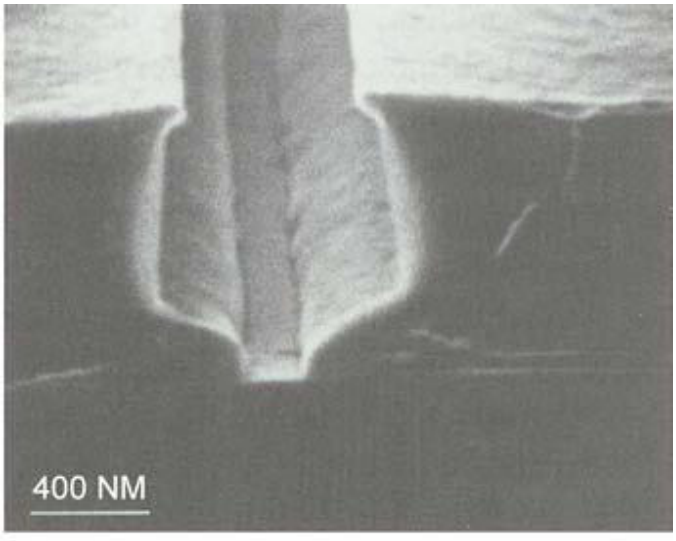

Figure I.4: T-shaped resist cavity using the trilayer resist system.

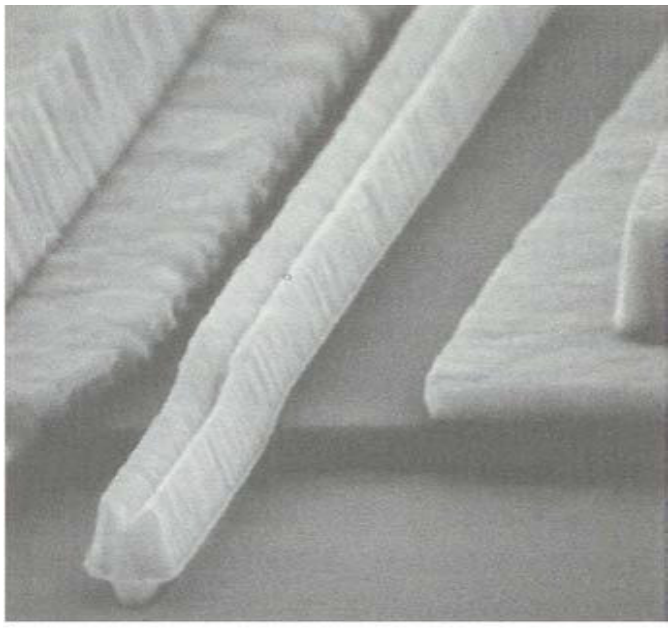

Figure I.5: T-shaped gate structure formed using the trilayer resist system.

I.6.2.4 Dielectric deposition and HEMT passivation

The device channel area is susceptible to surface damage, chemical and mechanical. Long-term degradation can occur through oxidation or particulate contamination and/or damage during handling and probing. Dielectric films such as polyimide, silicon nitride (Si_3N_4) and silicon dioxide (SiO_2) are commonly used to seal and protect the surface, keeping humidity, chemicals, gases, and particles away from sensitive areas of the device. Device protection or passivation (as it is named), requires a continuous, uniform, low-loss dielectric film. The polyimide film can be spun on the wafer, while Si3N4 and SiO_2 can be deposited using plasma-enhanced chemical vapor deposition (CVD).

For capacitors in a HEMT MMIC, a certain dielectric film thickness is needed to achieve the desired capacitance and to improve device and circuit reliability. A thick passivation improves reliability by eliminating pin-holes but reduces device performance by introducing extra parasitic input and feedback capacitance between the gate and drain. A thick passivation degrades the device noise figure, gain, and possibly power-added efficiency, especially at millimeter-wave frequencies. The final dielectric film thickness for HEMTs or MMICs is determined by a trade-off among the device and circuit reliability, performance, and capacitor requirements for the application.

I.6.2.5 Backside processing

The last steps in HEMT fabrication are wafer thinning, via-hole formation, and dicing. The substrate is thinned to reduce its thermal impedance, to improve its mechanical handling, and to facilitate transmission line and via-hole formation. A final substrate thickness of 3 to 4 mils (0.0762–0.1016 mm) is typically used for microwave low-noise HEMTs and MMICs. Uniform wafer thinning is the key to a high-yield via-hole process. Via-holes provide low-inductance source grounding which is critically important for high-frequency power HEMTs and low-noise and power MMICs.

The wafer thinning requires mounting of the wafer, usually with the wax frontside down, on a carrier such as glass, quartz, or silicon. Thinning the wafer is accomplished by mechanically lapping the backside of the wafer with a slurry of water and grit, usually silicon carbide (SiC), between the wafer and a flat plate, usually glass. To obtain a smoother surface, the wafer can either be further lapped with a finer grit or chemically polished.

After the wafer has been thinned and polished, the backside is patterned to open holes corresponding to the desired via locations. The via-hole pattern is defined with photolithography using infrared light for aligning the backside pattern to the frontside pattern. (Most III–V semiconductors are transparent to infrared light.) Via-holes can be formed with a wet-chemical etch or with RIE techniques. Compared to the wet-chemical process, the RIE via-hole process is less sensitive to the uniformity of the final substrate thickness and also provides smaller vias with controlled etch profiles. Figure I.7 shows typical via-holes etched through a 4-mil-thick (10-mm) substrate in a HEMT using the wetchemical approach. After the via-hole formation, the backside of the wafer is metallized. The chips are then separated through a wafer sawing or a scribeand- break technique. Figure I.8 shows a typical HEMT chip after scribe-andbreak. Chips with mechanical damage or surface contamination are screened out using both optical microscope and SEM inspections. The HEMT chips are finally electrically tested for dc and RF performance [10].

To summarize, in order to obtain uniform, high-yield, and reproducible HEMTs, the following are the most critical fabrication issues:

1) Uniform and low-defect density HEMT epilayers.

2) Formation of uniform submicron gates on large-size wafers.

3) Uniformity of the HEMT gate recess etch.

Each of these areas represents a significant technical challenge and requires a substantial investment in equipment and technology development to insure future HEMT device performance improvements.

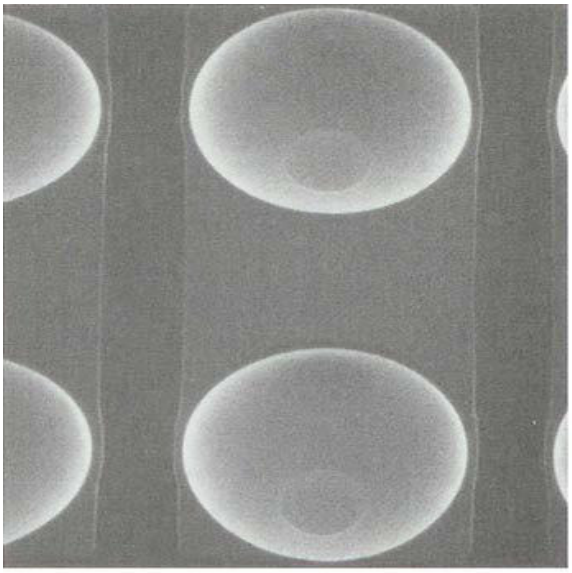

Figure I.7: Via-holes etched through a 4-mil-thick (10µm) GaAs substrate using a wet etch.

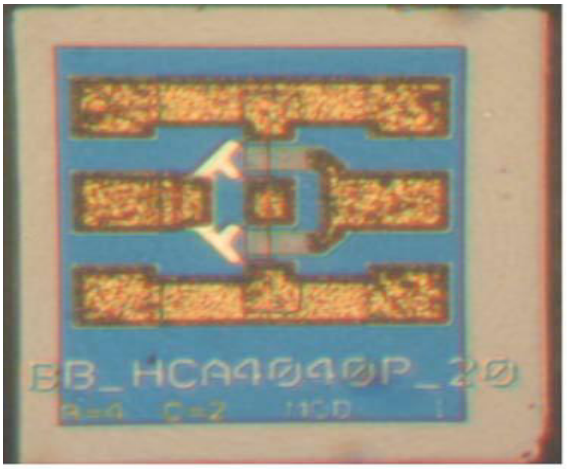

Figure I.8: Typical HEMT chip after scribe and break. (Note: all chips are inscribed with data identifying position on the wafer, gate number, and gate width [3].

I.7 Large Signal Models of HEMT Devices

GaAs MESFET models successfully predict large signal performance by predicting the voltage dependence of device characteristics. Of device's bias dependent nonlinear behavior, the transconductance is the most critical to the accurate prediction of many important large signal effects. The structure of each of the models has the same elements here (figure I.9). They have the same characteristics at low gate voltages. In

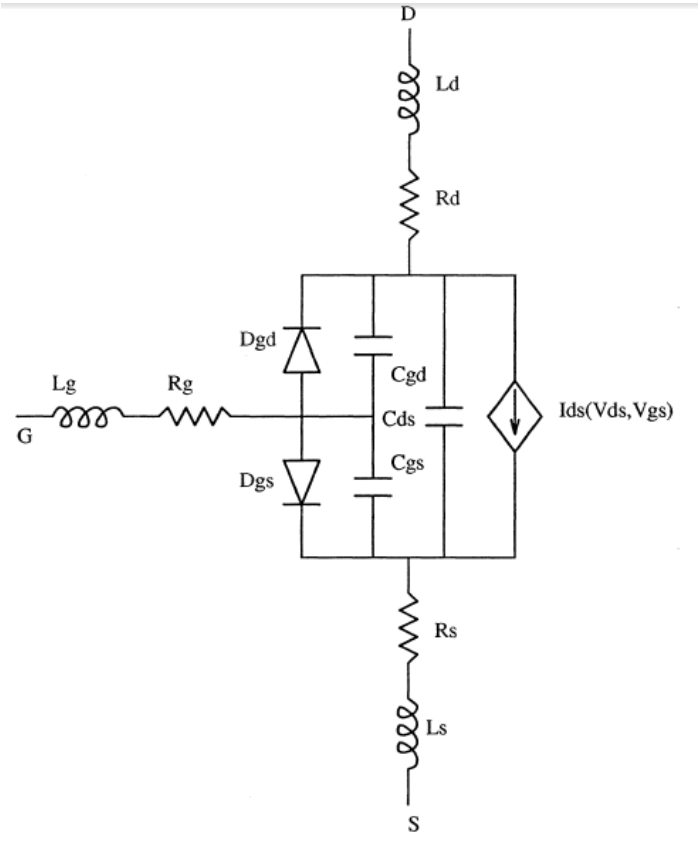

Figure I.9: The large signal model of a HEMT [11].

contrast to a MESFET, however, the HEMT's transconductance begins to decrease rapidly at some gate bias level. Based on this point, the HEMT models can be modified from the MESFET models. In figure I.9, there are three main bias dependent elements (C_{gd}, C_{gs}, and I_{ds}). Among them, drain current is the most important electrical property. The other two nonlinear capacitors do not affect the DC characteristics and will be ignored in the DC analysis[11].

C_{DS} : The intrinsic capacitance between drain and source.

R_{DS} : The intrinsic resistance between drain and source.

C_{GD} : The intrinsic capacitance between gate and drain.

C_{GS} : The intrinsic capacitance between gate and source.

V_{GS} : The gate source voltage.

V_{DS} : The drain source voltage

R_d : The parasitic drain resistance

L_s : The parasitic source inductance

R_s: The parasitic source resistance

I.8 CONCLUSION

In this chapter we recalled the principle of operation of field effect transistors such as HEMT heterojunction and pHEMT and their physical structure. Indeed, the electron mobility strength in this chapter the various parasitic effects and noise that may affect the field effect transistors because they are best suited for low noise enforcement.

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SECOND CHAPTER

MMICs DESIGN METHODOLOGY

II.1 Introduction

Monolithic microwave integrated circuits (MMICs) are microwave circuits in which the active and passive components are fabricated on the same semiconductor substrate. The additional term 'monolithic' is necessary to distinguish them from the established microwave circuits (MICs) which are hybrid microwave circuits consisting of discrete active devices and passive components integrated together onto common substrate using solder or conductive epoxy.

MMICs were born in the 1960s out of design research for military and aerospace applications. Their small size, lower power consumption, high reliability and optimum performance made them very attractive for cutting-edge applications. Over the next several years, MMICs remained confined to aerospace and military applications, and only recently, have they begun to penetrate the commercial high-frequency wireless markets. The demand for high-performance/low-power consumption devices for cell-phones, wireless-Local Area Networks (LAN), Local Multipoint Distribution Systems (LMDS) and the emerging wireless-Wide Area Networks (WAN) has brought MMICs into the commercial market spotlight [1].

MMICs pose a different set of design challenges than those of traditional analog/digital design. At frequencies ranging from 2 to 40 GHz and beyond, physical parasitic effects play a prominent role. This, coupled with other important factors such as the equally important roles of active and passive components, component proximity and inter-connects, high circuit analysis complexity and process variations, presents a tremendous challenge to those seeking top design performance in the microwave frequencies and this means that MMICs have a special range of applications and that MMIC design is very different to conventional VLSI design, in which CAD offers a high degree of layout automation. The important transmission-line nature of interconnections on an MMIC requires far more involvement from the designer in the layout process [2].

II.2 Advantages and disadvantages of MMICs

II.2.1 Cost

The low cost advantages stems from the simple fact that a single wafer can produce upwards of 1000 working circuits, each with very similar performance and requiring no hand tuning and minimal assembly work. This argument holds as long as the circuit is fairly complicated and requires a large number of components. However, in many cases it is possible to use packaged transistors soldered onto a cheap substrate. Then the most expensive components are the transistors; the passive components such as filters and matching networks cost next to nothing, and the assembly is straightforward with packaged transistors.

II.2.2 Performance

Most MMIC devices have to be tailored to volume production and tend not to give state-of-the-art performance. This can be a serious problem for low-noise and high-power amplifier design, where performance is of prime concern. For the very best noise figure and power efficiency it is often necessary to use discrete transistors before and after the MMIC parts. With a hybrid MIC the designer can choose the best transistor for the job, and the transistors may be from different manufacturers. Discrete transistors can use the shortest gate length and optimum active layer structure for their application, regardless of other requirements, because yield is much less important. Using the same fabrication techniques for complex MMIC would result in a very poor yield because of the multiplicative effect of the yields of individual transistors on the same chip. For low-density circuits this is not so much of a problem, and so millimeter-wave circuits using HEMTs should give good performance and yield.

II.2.3 Reliability

MMICs are more reliable than hybrid MIC circuits, as long as the fabrication process is carefully controlled and qualified. In contrast, the mechanical limitations of chip attachment and wire-bonding become all too apparent when a hybrid circuit is subjected to temperature cycling, shock, and vibration.

II.2.4 Size and Mass

MMICs are very compact, and this can be a significant advantage. In many commercial applications there is an increasing need to miniaturize the microwave circuits, with smart cards and radio transceivers for PCMCIA slots (in notebook computers) being good examples. The active phased array antenna is the primary applications where size is very important: since each face of an array may have many hundreds of modules, MMICs are essential in order to minimize the antenna size and mass.

II.2.5 Investment required

Setting up an MMIC fabrication facility for mass production is prohibitively expensive. There was a time when most major microwave companies had their own facilities as a matter of course, in order to demonstrate their capability. When the profitable applications were not forthcoming, there was a period of regrouping and consolidation. There are still many major foundries/suppliers of GaAs and silicon MMICs [3]. A list of MMICs major manufactures can be found in [1]. In contrast, developing hybrid MIC circuits using packaged transistors can be carried out with PC-based packages like Touchstone, and with little more than an etching tank and soldering iron. A simple hybrid MIC circuit can be laid out, constructed, and tested in one day. Because the substrate is cheap and plentiful the designer doesn't need to spend time squeezing the circuit into the smallest possible space. The prototype can be tweaked with a scalpel and conducting paint, and then the final design completed. The capital investment required and development times are both considerably less for MICs, with obvious benefits.

II.3 Types of MMICs

As well as the different device technologies (GaAs, InP, Si.....), in general there are three quite distinct circuit topologies used for MMIC design. The choice of which almost entirely depends on the operating frequency of the circuit. The three techniques can be classified as 'all-transistor', 'lumped elements', and 'distributed' techniques. Fig. II.1 shows the approximate frequency range to which each approach is applicable. There is some overlap of each approach's useful frequency range of application, and the techniques may often be blended together in the same design.

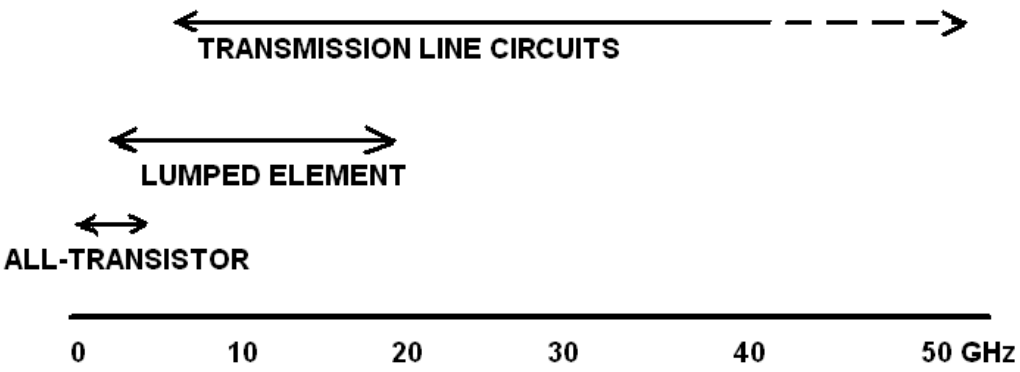

Figure II.1: Typical frequency range of operation for the three approaches of MMIC design.

II.4 MMIC Design

The penetration of commercial radio frequency systems into the microwave and millimeter-wave bands has put increased pressure on reducing MMIC costs at all stages of production and design. In the field of circuit design, the use of CAD simulation and layout tools plays a pivotal role in first-time success and yield of a MMIC design.

II.4.1 Design Flow Productivity

Designing a MMIC involves two critical stages: performance specification, and circuit design and simulation. Other functions such as fabrication and test must also be considered during the design stages to arrive at a manufacturable product with high yield and the desired performance [5]. A typical MMIC design flow chart is shown in Fig.II.2:

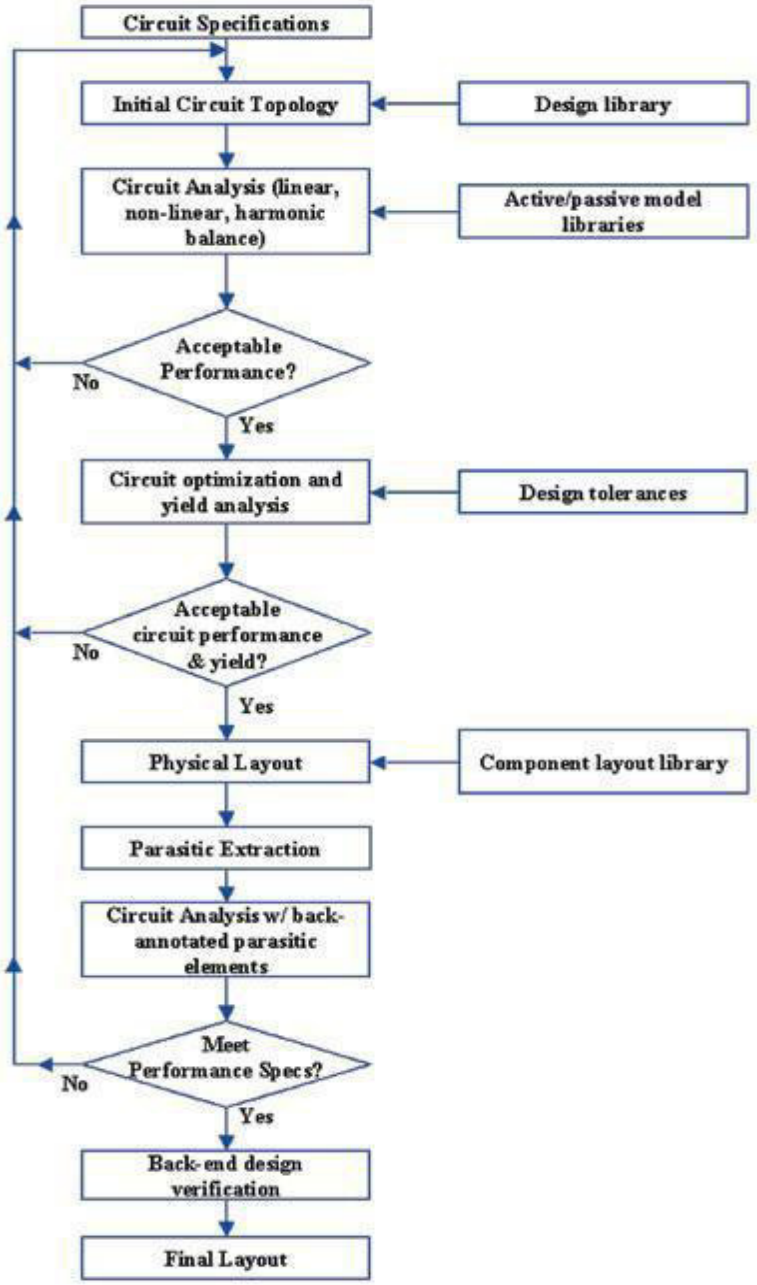

Figure.II.2: Typical MMIC design flow [5]

II.4.2 Design for reliability and manufacturability

Several factors may have a direct or an indirect impact on circuit yield and reliability. Device parameter variations as a result of process limitations or level of control, raw material variations, and EM proximity effects all play roles in determining overall circuit reliability and yield. The approach for achieving a reliable design should take into account the following:

1- Definition of realistic performance requirements.

2- Documentation of design methodology.

3- Material and processing characterization and variation.

4- Understanding of potential failure mechanisms.

5- Use of adequate simulation and test tools.

The definition of realistic and achievable performance requirements is probably the most important initial step in MMIC design. Pushing the design-performance boundaries may result in selection of devices that fall at the edges of the normal Gaussian distribution. This will result in low yield and may have an impact on the reliability of the selected components. Therefore, design-performance requirements should fit very comfortably into the high-yield and assured performance window of a MMIC foundry's process.

A documented design methodology can provide a clear path for device design, simulation, layout, and fabrication. This approach will also allow a smoother design implementation and identification of unacceptable design limits or points of possible yield loss. Figure III.1 shows a typical design flow and the various necessary inputs. The characterization of the processes and materials used throughout the fabrication cycle is also connected to an understanding of the common failure mechanisms and other reliability aspects of device and circuit design. As an example, gate length and placement-variation effects have been shown to be the dominant factors in limiting the yield of semiconductor devices. To meet performance requirements at higher operating frequencies, shorter gate lengths are normally required. However, this results in smaller gate-metal-to semiconductor contact area, which is more critical from the yield and reliability aspect. Another parameter of importance is the chip length-to-width aspect ratio; it should be kept as close to 1:1 as possible to increase overall yield and reduce chip breakage during the dice and sort operations. A maximum chip length-to- width ratio of 3:1 is the normally recommended ratio for MMICs. Layout design rules, derived from empirical and process-variation data can be very valuable in increasing the yield and reliability of a MMIC design. Considerations for circuit element placement, sizing, process variations, and physical tolerances play an important role in determining the reliability, yield, and final cost of the product. Yield analysis techniques are normally practiced to determine the overall yield and identify areas of poor yield performance. Additionally, sensitivity analysis techniques are commonly employed to determine a

design's sensitivity to variations in bias point, device process parameters, tolerances, and thermal conditions. In-process and on-wafer testing of MMIC components can provide valuable information on the performance and yield of the final product. Comparison of these data with those of the process can indicate the manufacturability of the design for a particular foundry.

II.5 Methodologies designing LNA

The project methodology present the implementing process for low noise amplifier. In early stage, the literature review and understanding of theory about the overall procedure in this project will be compared. Figure II.5 shows the flow chart of the project [7].

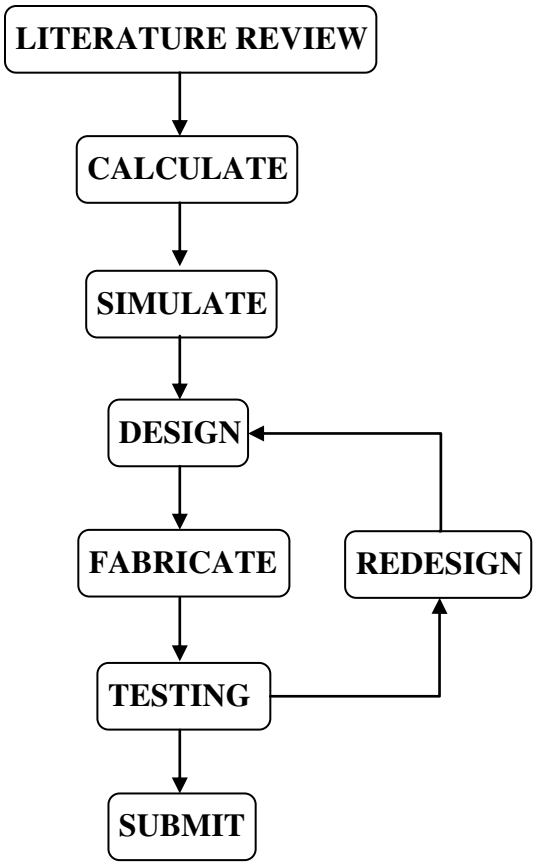

Figure II.3: Flow chart of project [7].

II.5.1 Literature review

The understanding parameter such as **S** parameter, VSWR, noise parameter and etc need to be covered. These parameters can be found from the data sheet of the transistor. Related topics need to be covered such as bias design, circuit stabilization, noise optimization, linearity optimization, load pull for gain and Third-Order Intercept Point **(IP3)** off improvement and complete circuit characterization [2]. The component that will be used in design the low noise amplifier circuit such as transistor, material and type of bias will be identified.

II.5.2 Calculate

All components will be calculated and selected using theoretical analysis.

II.5.3 Design and simulate

The low noise amplifier circuit is adapted into simulation software. The circuit will be simulated and the data will be collected. The important parameter for this low noise amplifier circuit is the gain and the noise figure.

II.5.4 Fabricate and testing

The low noise amplifier circuit will be constructed and fabricated on the microstrip board. The value of the hardware will be measured. It will be tested and analysed in this process.

II.6 Gain and stability of the amplifier

The design method presented in this paper is based on the S parameters of the transistor [6], and can be used with both bipolar and field effect transistors (FET).

A transistor amplifier in the band of microwaves (300 MHz – 300 GHz) can be designed using the circuit shown in (Fig II.2).

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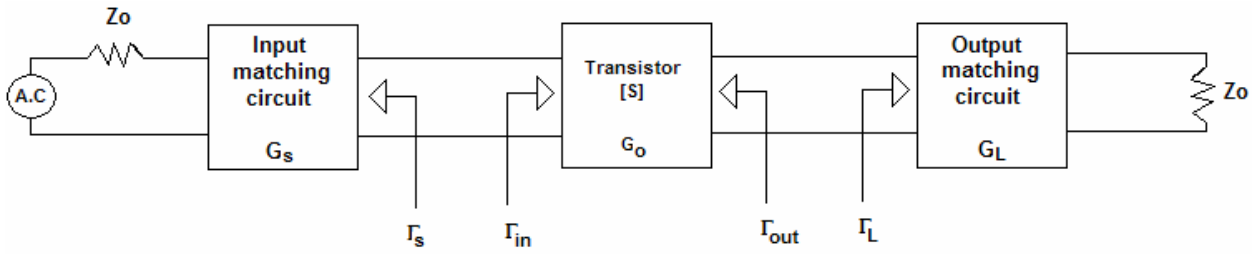

Figure II.4: Amplifier General Circuit.

The reflection coefficients at the input and output of the circuit are defined as follows:

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \qquad \text{(Equ. I.1)}$$

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \qquad \text{(Equ. I.2)}$$

S_{11}, S_{12}, S_{21} and S_{22} are the dispersion parameters of the transistor (S parameters) whereas Γ_S and Γ_L are the reflection coefficients of the source and load respectively.

The gain of the transistor is the ratio between the given power on the load and the available power at the source and it depends on the matching at the input and at the output. In this way it is possible to define effective gain factors for the input matching network (source), the transistor and the output matching network (load) as follows [6]:

$$G_s = \frac{1 - |\Gamma s|^2}{|1 - \Gamma_{in}\Gamma s|^2} \qquad \text{(Equ. II.3)}$$

$$G_o = |S_{21}|^2 \qquad \text{(Equ. II.4)}$$

$$G_L = \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \qquad \text{(Equ. II.5)}$$

Now, the total gain can be defined by: $G_T = G_S\, G_0\, G_L$ (Equ. II.6)

If the transistor is unilateral, $S_{12} = 0$ or it is small as to be ignored, (1) and (2) are reduced to:

$\Gamma_{in} = S_{11}$ $\Gamma_{out} = S_{22}$

Now considering the stability of the amplifier shown in Fig. 2, oscillations may be produced if either input or output impedance has a negative real part. This would imply that $|\Gamma_{in}| > 1$, $|\Gamma_{out}| > 1$. Since Γ_{in} and Γ_{out} depend on the matching network at the source and load, the stability of the transistor will depend on Γ_S and Γ_L. So we define two types of stability:

A. Unconditional stability: The network is unconditionally stable if $\Gamma_{in} < 1$ and $\Gamma_{out} < 1$ for all the passive impedances on the source and on the load.

B. Conditional stability: The network is unconditionally stable if $\Gamma_{in} < 1$ and $\Gamma_{out} < 1$ only for a certain range of passive impedances on the source and on the load. This case is also known as potentially unstable.

A two port network can be considered unconditionally stable if and only if the two following conditions are satisfied:

$K > 1$ and $|\Delta| < 1$, which are described by the following equations.

$$|\Delta| = S_{11}.S_{22} - S_{12}.S_{21} \qquad \text{(Equ. II.7)}$$

$$K = \frac{1+|\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2 \cdot |S_{12} \cdot S_{21}|} \qquad \text{(Equ. II.8)}$$

In an other hand, applying the unconditional stability requirements to (Equ. II.1) and (Equ. II.2), result in conditions for Γ_S and Γ_L in order to be considered unconditionally stable, such conditions are defined as follows:

$$|\Gamma_{in}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \qquad \text{(Equ. I.9)}$$

$$|\Gamma_{out}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \right| < 1 \qquad \text{(Equ. I.10)}$$

Alternatively if the device is unilateral ($S_{12} = 0$), these conditions are reduced to that if

$S_{11} < 1$ and $S_{22} < 1$.

II.7 Noise figure

The minimum and actual noise figure of the LNA was simulated using scattering parameters. Its formula is bellow:

$$NF = NF_{min} + \frac{4R_n|\Gamma_s - \Gamma_{opt}|}{(1-|\Gamma_s|^2)|1+\Gamma_{opt}|^2} \qquad \text{(Equ. I.11)}$$

Γ_s, Γ_{opt} : It is coefficients reflexion of the optimal admittance of respectivement noise.

R_n: The equivalent noise resistance of the transistor.

II.8 Conclusion

In this chapter we presented the design of the low noise amplifier must meet the specification of the specifications (greater than 10dB gain and noise figure is less than 1dB). For this, we opted for the source system topology cascode common among the different configurations previously mentioned. Indeed, the cascode amplifier has a high gain and good insulation and low noise which is almost identical 'to the one transistor connected in a common source. To have a strong gain was two cascaded stages connected in a common source.

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THIRD CHAPTER DESIGN AND SIMULATION OF LNA

III.1 Introduction

State-of-the-art communications and radio astronomy applications demand high-density, small size, and reliable multifunction monolithic microwave integrated circuits (MMICs). MMICs use microstrip or coplanar waveguide as the planar connections between semiconductor devices. These open waveguides contain a significant portion of electromagnetic energy above the circuit substrate. Furthermore, as advanced circuits are made more complex and more compact, inter element coupling begins to affect overall circuit performance. For example, if a transmission line is placed too close to a rectangular spiral inductor that is used in a filter, the parasitic coupling between the two elements could change the value of the inductor and detune the filter. Although MMIC density is still low relative to that of most advanced digital integrated circuits, MMIC designers are faced with competing objectives. A circuit design must simultaneously accommodate the area required by the largest structures in an MMIC (typically inductors or inductive lines), maintain a "reasonable" distance from nearby transmission lines and other elements, and minimize the use of chip real estate. On the other hand, in designing a wide-band LNA, it is always required to obtain low noise, high gain, and low VSWR performances with adequate circuit stability, all over the frequency band of interest. Because of all these aspects, the design of a broadband MMIC LNA, especially in such low frequency range (L-band), is quite challenging [1, 2].

III.2 Active device description

The fabricated high breakdown 1 μm InGaAs-InAlAs-InP pHEMT used in this work is shown in figure 1. Such transistor is suitable for radio-astronomy applications. It uses an advanced MBE (Molecular Beam epitaxy) growth technique and is a four finger device with 200 μm unit gate width and 1 μm gate length. Looking at the structure from bottom to top, a lattice- matched undoped $In_{0.52}Al_{0.48}As$ buffer layer of 4350 °A thickness, is grown on top of an InP semi insulating substrate. A highly strained, undoped $In_{0.7}$ Ga $_{0.3}As$, channel is grown well below the critical thickness of this composition (140 ° A). The spacer is a lattice matched, undoped In0:52Al0:48As layer of 100°A thickness used to spatially separate the

heavily doped delta-region from the active channel. A supply layer $In_{0.52}Al_{0.48}As$ is formed with 300°A thickness to supply electrons into the 2DEG and the 500°A $In_{0.53}Ga_{0.47}As$ cap layer [3,4].

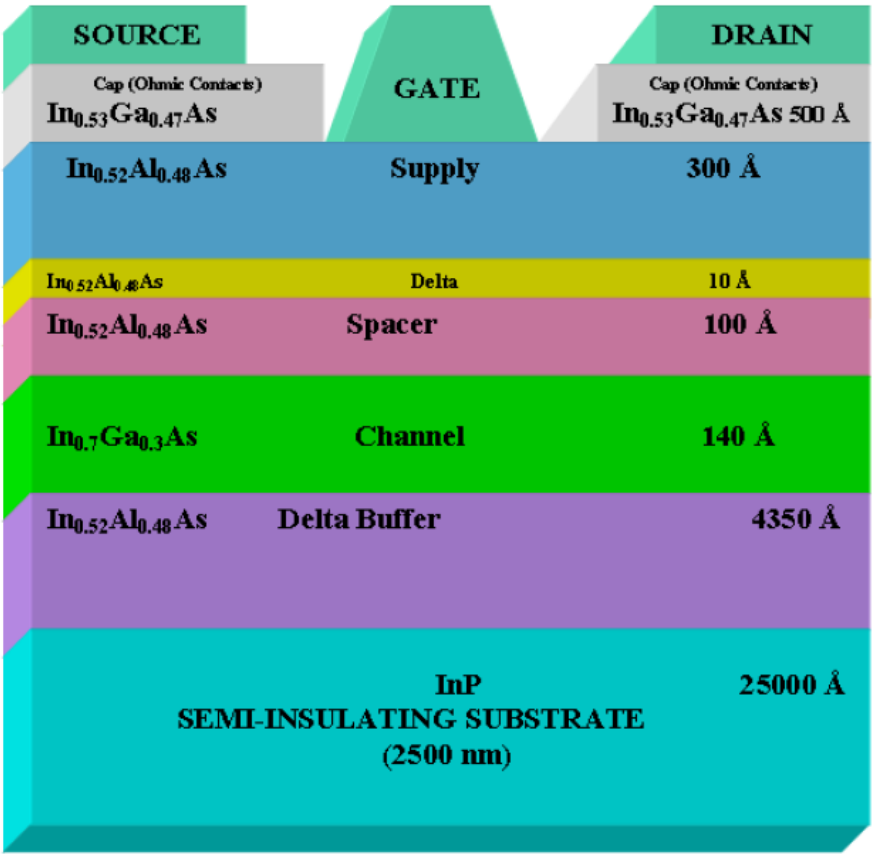


Figure III.1: The epitaxial layer structure of the pHEMT used in this work to design radio frequency LNAs [3].

III.3 State of the art amplifier LNA in astronomy

In reality there are few kinds of different LNA, and regardless of the technology used.

They can be classified into four main types of architectures that are LNA:

- Resistive termination
- Terminated in 1/gm (the inverse of the transconductance)
- To shunt circle

- At inductive degeneration

The main criteria for a low noise amplifier are:

- Operating frequency.

- Factor of noise circuit (dB).

- Gain (dB).

- Linearity.

To answer the specifications of our application charge must also optimize consumption (dissipated power) and clutter. Table III.1 presents a state of the art low noise amplifier application in radio astronomy.

Parameter	Target Goal	Accepted Tolerance	Unite
Frequency	0.5 - 3	--	GHz
Band passant	1	--	GHz
Gain	> 10	± 20%	dB
Noise figure	< 1 (NF_{min} + 0.2)	± 30%	dB
Input Return Loss	<-10	± 20%	dB
Output Return Loss	<-10	± 20%	dB

Table III.1: Specifications list of LNA.

We worked by **Advanced Design System (ADS)** is the world's leading electronic design automation software for RF, microwave, and high speed digital applications. In a powerful and easy-to-use interface, ADS pioneers the most innovative and commercially successful technologies, such as X-parameters and 3D EM simulators, used by leading companies in the wireless communication & networking and aerospace & defense industries. ADS provides full, standards-based design and verification with Wireless Libraries and circuit-system-EM co-simulation in an integrated platform [3].

III.4 The low noise amplifier configurations

III.4.1 A two-stages common sources cascaded

The Fig.III.2 shows the circuit of LNA designed. Used (T1) in structure common source. The addition of a (T2) ensures isolation between the output and the input of the stage and prevents problems of instability.

It is believed that the source impedance is Rs = 50Ω. Among all LNA architectures proposed in the literature, we chose the structure shown Fig III.2.

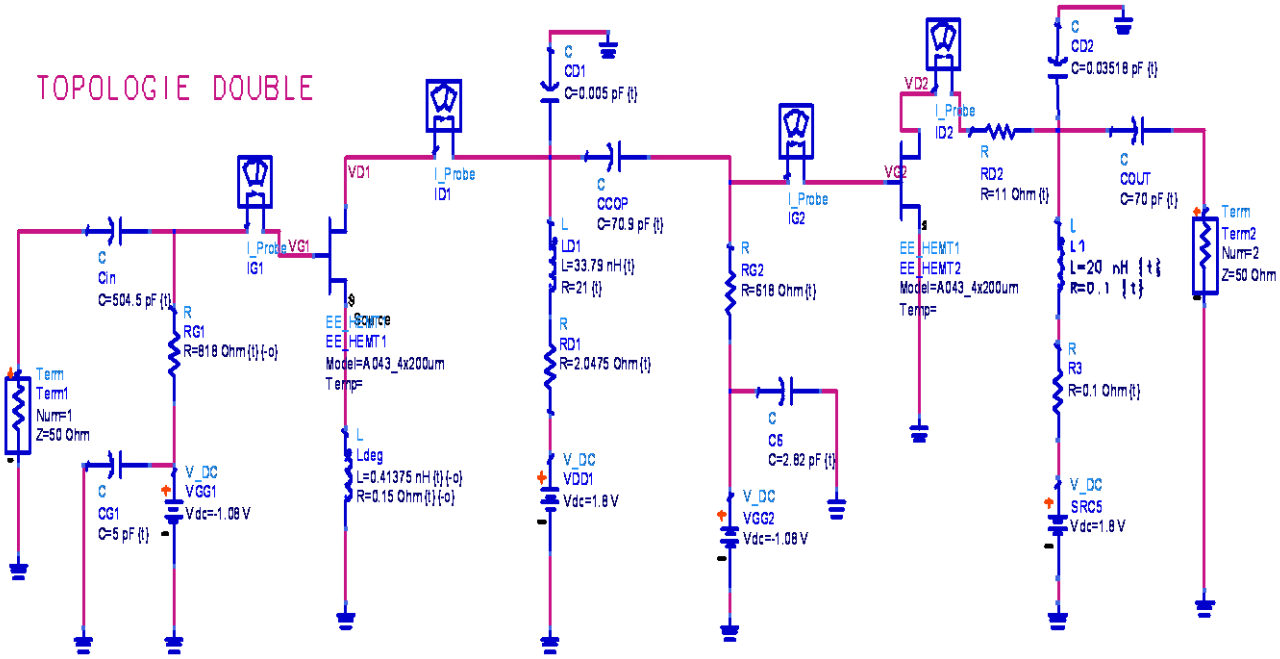


Figure III.2: circuit LNA, double stages common source cascaded.

It circuit comprises a bias stage, a cascade and matching networks at the input and output. The operating point of the transistor is selected in order to give the best noise performance, the conditions of the polarization donner as follows:

- The supply voltage DC=1.8v
- The drain voltage V_{d1}=1.26 v
- The current of drain I_d= 27 mA .
- The supply voltage of gate V_{g1}= -1.08v.

The LNA cascade circuit consists of:

- The resistance R_{D1} and the inductor L constitute the matching network grafted transferring the input impedance in the circuit 50 ohm (1.8v, 27 mA).
- The resistor R cross-adaptation of the circuit.
- The capacitor C_{in} and the inductors L_1, L_{deg} are the output matching network which transfer the output impedance of the circuit in 50 ohm.

Adaptive input and output networks provide both adaptation. and stabilizing the biasing of the transistor. Each amplifier is stabilized in its operating frequency band (0.5 - 2.3 GHz) and unconditionally stable in the band (0.1-30 GHz).

VD1	VD2	VG1	VG2	ID1.i	ID2.i	IG1.i	IG2.i
1.267 V	1.493 V	-1.080 V	-1.080 V	-23.14 mA	-27.37 mA	-414.3 pA	-414.3 pA

Table.III.2: Bias of LNA cascade.

III.4.2 Three-stages common source and cascode configuration

To increase the gain on the band we can to cascade multiple cells common source. This cascade provides a higher gain over a wideband.

We are proposed in this work is a cascaded two-stage structure, in order to improve the performance of LNA and specifications: The minimum noise factor and the gain more than (Top) is 20dB.

The first stage is designed to minimize noise while the second stage to improve the gain and the third the figure noise and gain of the amplifier are then maximized.

The conditions biasing are presented in Table fellow (Tab. III.3):

ID1.i	ID2.i	IG1.i	IG2.i	VD1	VD2	VG1	VG2
-44.12 mA	19.49 mA	-414.3 pA	-414.4 pA	1.230 V	945.9 mV	-980.0 mV	-1.080 V

Table III.3: Bias of LNA three-stages cascode

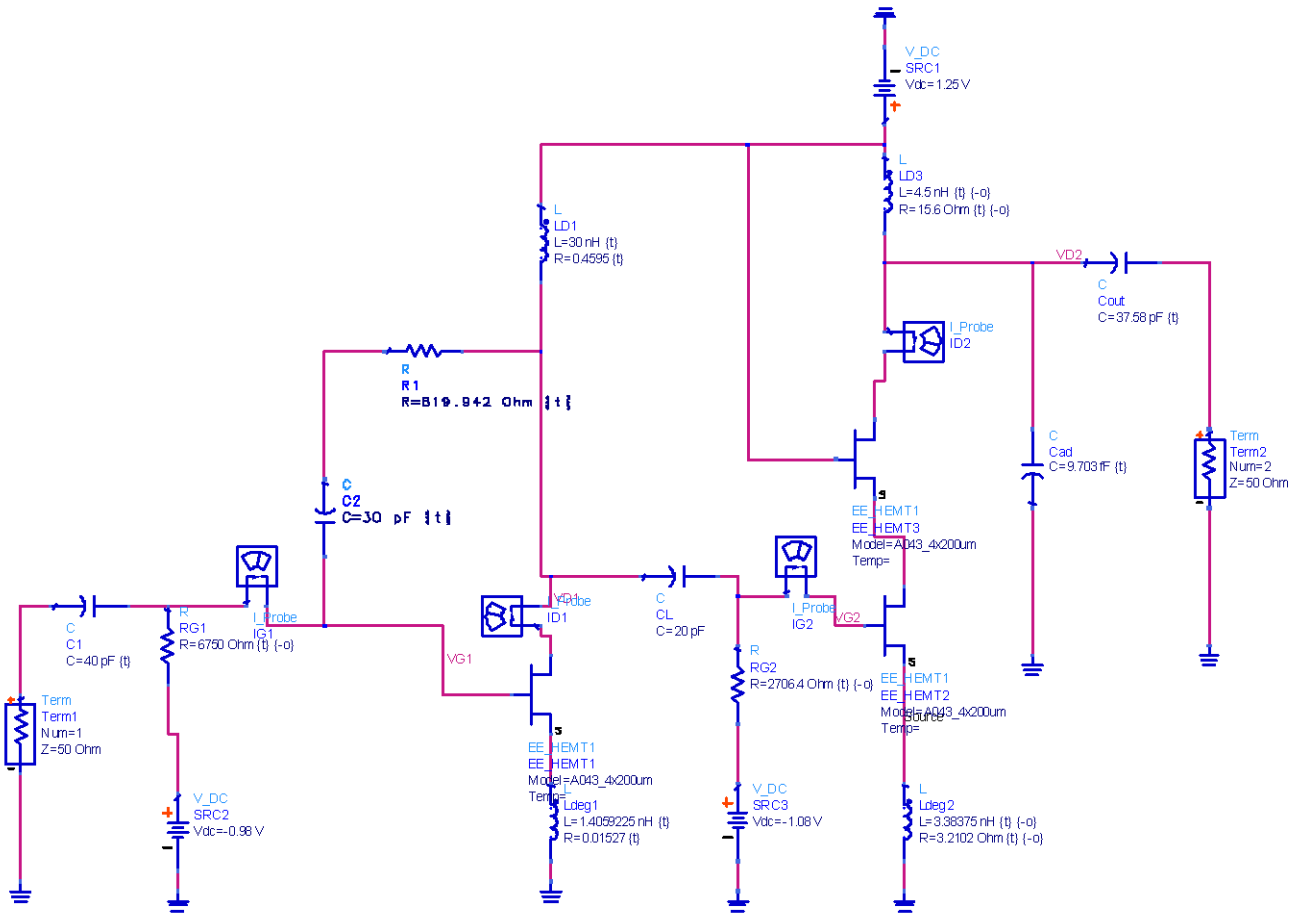


Figure.III.3: The amplifier LNA , Three-stages common source and cascode configuration

III.6 Discussions of Results

We have simulated the performance of circuit (Fig III.3) using optimization and adjustment techniques of ADS to determine the best values of components of the circuit giving a compromise between high gain and low noise value ensuring adaptation and stability of the amplifier. We obtained the following results:

The reflection coefficient S_{11} is strictly less than -20 dB (Fig III.4).

This circuit function in biasing point has been a high gain and noise performances:

V_{DS}= 1.8 V, I_{DS}= 27 mA

III.6.1 The low noise amplifier mounted in common source cascode

By ADS (Advanced design System) simulated this amplifier for calculated the performances:

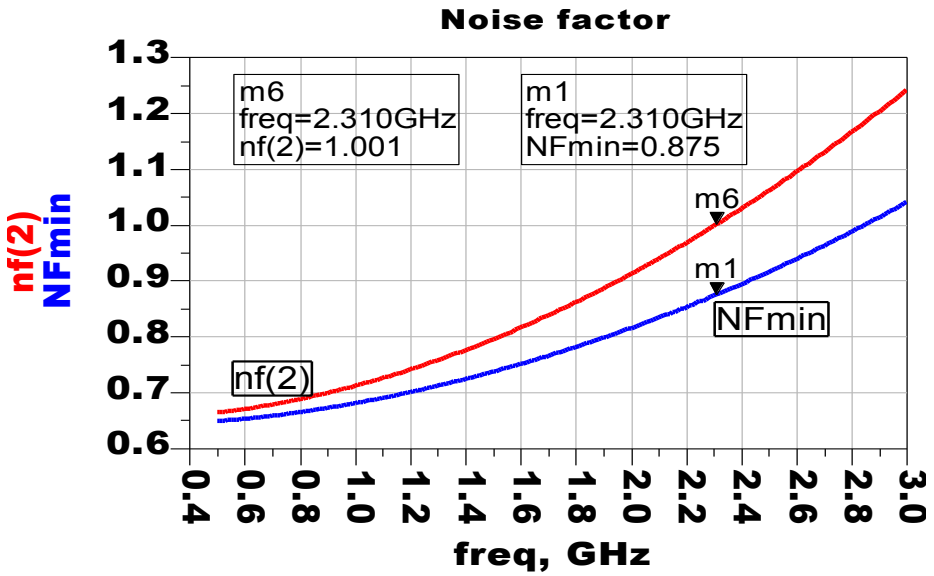
S-parameter and noise factor. Optimization techniques and adjustment of ADS we used to set the best values of the circuit components, giving a compromise between high gain and low noise factor ensuring adaptation and stability circuit input and output.

The results and simulation of circuit LNA as follows:

- The gain more than (>10 dB) it's mean (S_{21}= 38dB in frequency 1GHz).
- The noise factory NF=1 GHz and NF_{min}= 0.875GHz.
- A reflection coefficient at the input and output: S_{11}<-10 dB and S_{22}<-10dB when frequency on 0.65 GHz.
- The associated noise gain >10dB.
- Factor of stability K>1 while 3.0>F>0.5 GHz.
- The impedance of output $Z_{output}\approx 50\Omega$ between 1.6 GHz to 2.08 GHz, and Z_{opt} between 0.97 GHz to 1.27 GHz.

The unconditional stability of the entire band of interest Fig III.4 (b), and also checked on a broadband (0.1-30 GHz), the transistor can be adapted input and output by any impedance.

(a)



(b)

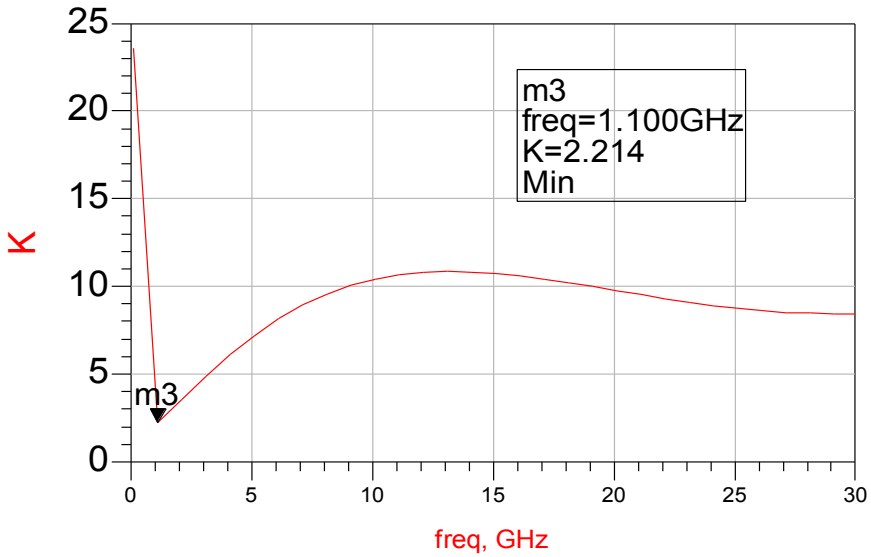


Figure.III.4: (a) Noise factor, (b) Stability of LNA cascade.

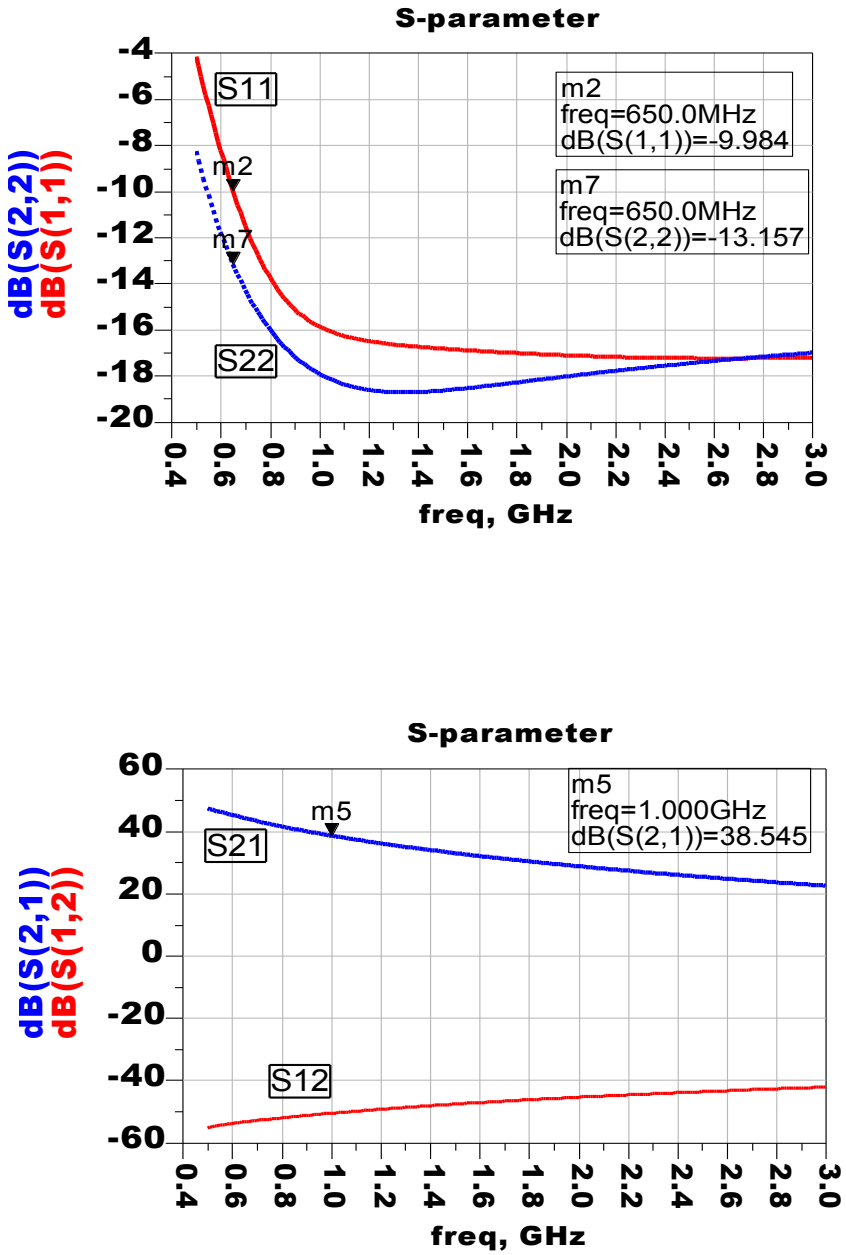


Figure.III.5: The performances of LNA (S-parameter). source common cascade

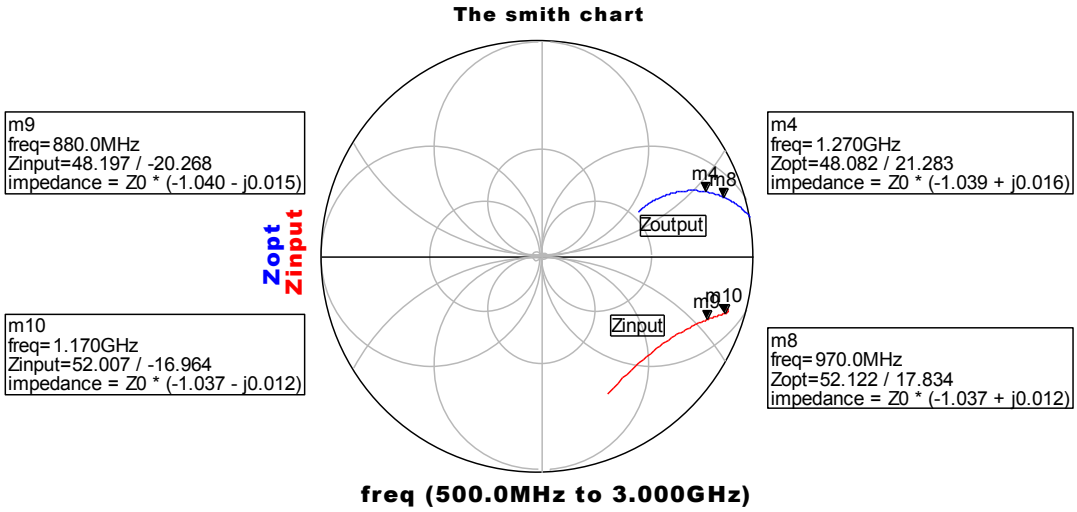


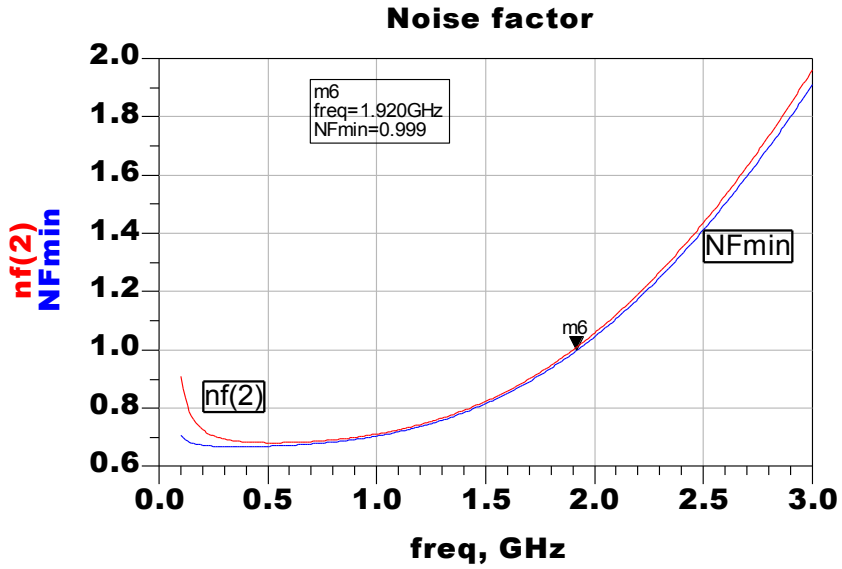
Figure III.6: The Smith chart.

III.6.2 The low noise amplifier mounted in common source Three-stage cascaded

We are doing the same way as the previous system of simulation and these results are better from last circuit and check the specifications Figures (III.6, III.7, III.8) of the performance of the LNA are:

- The gain (S_{21}) more than 20dB when 1.09>F>0.18 GHz.
- A reflection coefficient at the input (S_{12}): 3.5> F >0.59 GHz.
- A reflection coefficient at the output (S_{22}): 0.7> F >1.7 GHz.
- The noise factor: NF< 1dB if the frequency<1.92 GHz.

(a)



(b)

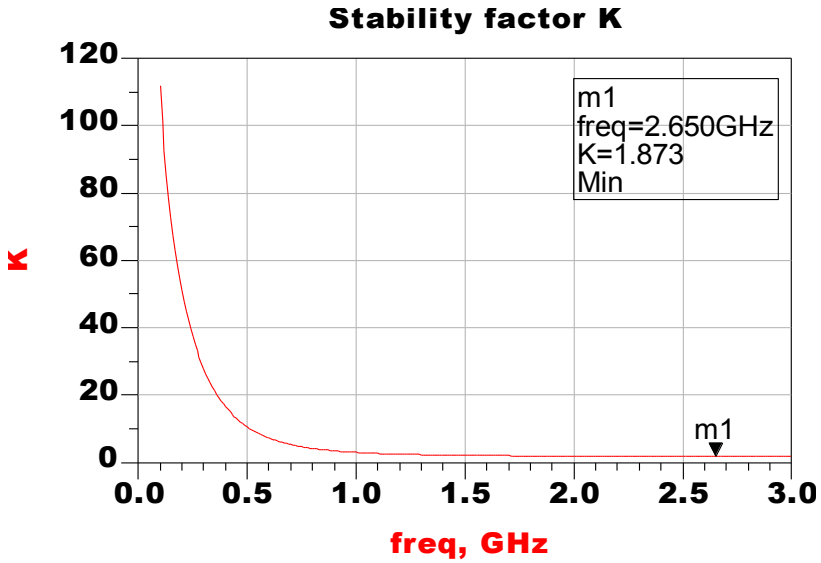


Figure III.7: (a) The stability of LNA cascode, (b) The noise factory.

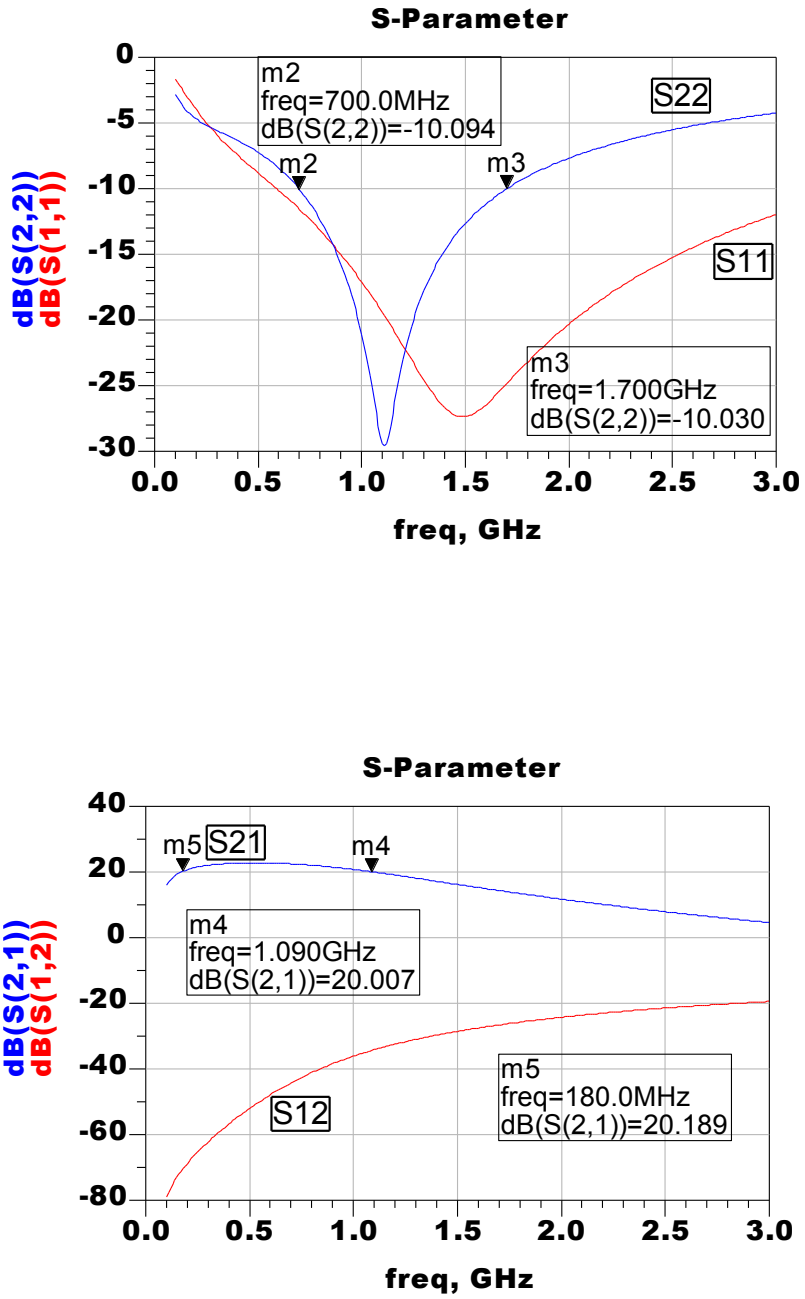


Figure III.8: The performances of LNA (S-parameter). source common three-stages cascode.

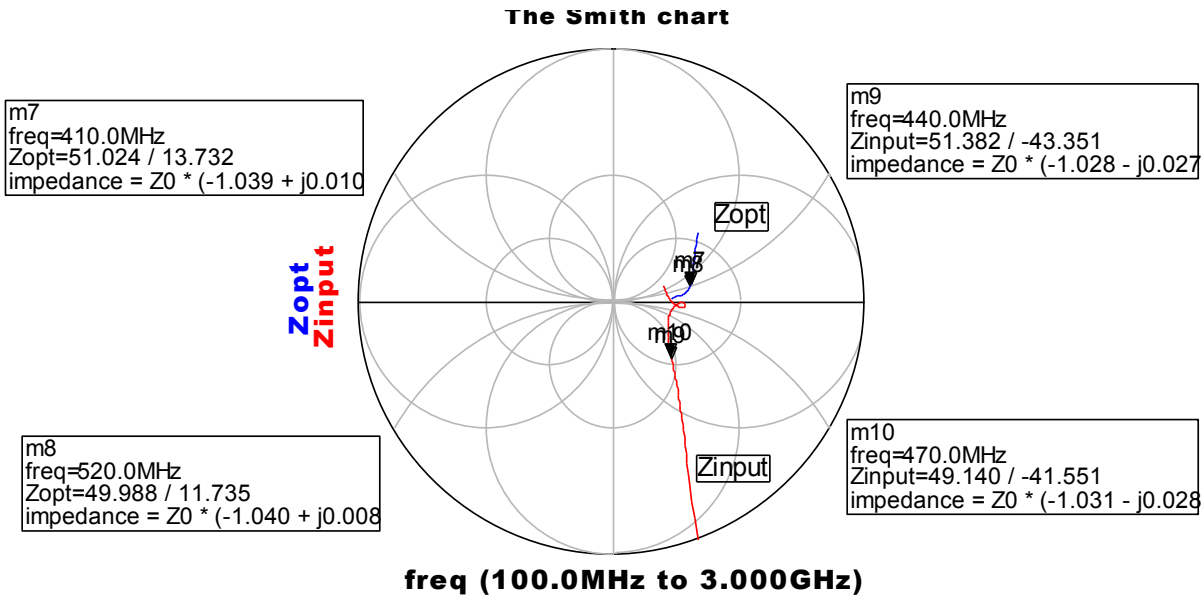


Figure III.9: The Smith chart.

III.7 Conclusion

In final chapter we describe the design of a low noise amplifier at low voltage supply (1 V) and operating in the band (0.4-2.3 GHz). The performances of two LNAs obtained are almost comparable the specifications.

The bias circuit of the transistor A043 is designed to maintain constant working point, to minimize noise and improve stability. The reflection coefficient is satisfactory, with parameter S_{11} and S_{22} below -10dB for the first cascade LNA cell. However, the S_{11} parameter reaches -10 dB from 0.6 GHz. We also note that the S_{22} parameter is slightly better at low frequencies. The S_{21} gain is relatively flat with no ripple in the band of interest. And more than 20dB in three stages cascade.

After optimization for the best possible gain of the LNA, we checked the satisfaction of the

output matching demonstrating that its reflection coefficient S_{22} is minimal for the 0.6 GHz frequency.

Finally, this LNA gave an acceptable gain of 26.5dB, a factor 0.64dB minimum noise and stability in a wide band between 0.1GHz - 30GHz. while the second configuration of the LNA has a gain greater than 27 dB, a lower noise figure and good 0.63dB output matching (S_{22} <-13.15 dB for the frequency> 0.65 GHz).

III.8 References

[1] A. D. Y. a. S. S. Osofsky, "Design and Analysis of a Traveling-Wave MESFET With Enhanced Shielding Capabilities," *IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES*, vol. 42, pp. 1610-1616, 1994.

[2] L. D. a. M. Terrovitis, "A Broadband Low-Noise-Amplifier," Department of Electrical Engineering & Computer Sciences, University of California May, 1999 1999.

[3] Z. Hamaizia, "Conception d'un amplificateur faible bruit LNA à base d'un transistor à effet de champ à hétérojonction pHEMT ", *Thèse de Doctorat Université de Biskra, Février 2011.*

[4] ADS2009, Agilent Technologies, Palo Alto, CA, USA.

General Conclusion

The amplifier design for telecommunications applications, astronomy and radar systems to microwave frequencies require knowledge and a thorough characterization of the components at the heart of these systems, namely transistors. At present, a large technological diversity, both in the choice of semiconductors by the different types of transistors used to offer the designer to achieve this task.

Therefore, the design of amplifiers must go through a judicious between different technologies according to their potential and criteria specified according to the applications referred choice. Criteria relate to constraints of power, performance, and constraints in terms of cost and reliability are of prime importance in the industrial context.

The transistors FETs are the most interesting features for low noise applications. The main objective of this work is to design an amplifier with low broadband noise for astronomy application.

So this work began with a general study of components based on GaAs and InP, after recalling the essential proporiétés material and growth processes, the study is geared more towards the characteristics of heterojunction transistors HEMT and family as pseudomorphic viewpoint of its heterojunction.

To meet the specifications, two a mplifier circuits using the transistor pHEMT summers are developed for various constraints that the stability of the transistor, minimizing the overall noise, maximum gain and bias of the transistor.

In the second chapter, in the first place, we introduced the definitions of performance criteria of a microwave amplifier as gain, noise figure, stability and S-parameters Then we presented the diff-erent blocks matching circuits in the input and output of the transistor pHEMT thus constituting the body of the LNA. It detailed in designing methodology of MMICs.

Finally, we introduced two low noise amplifiers based on two different architectures, first mounting cascode common source circuit. perfectly adapted to the constraints of low power consumption, they offer outstanding features in terms of their power gain exceeding 10 dB gain for the first circuit and 38.5dB for the Second Circuit.

For the design of low-noise amplifiers, were answered specification of specifications (greater than 10 dB gain and NF less than 1dB). For this, so opted for the topology of common source cascode circuits and three cascaded common source-stage. Indeed, the cascode amplifier has a high gain and good insulation as a low noise figure is almost identical to that of a single transistor connected in a common source. On the second circuit, it is designed to provide enough gain (greater than 38.5dB).

These two topologies using the LNA transistor pHEMT_A043_800µm were designed for the requirements and specifications of SKA. We can say that these two architectures designed almost met most requirements of the specifications by providing a noise near NFmin and sufficient gain. Overall, we can say that this work has to come up with acceptable results vis-a-vis those found in the literature.

Perspectives:

The two circuits Will Be Realized later designed and integrated in radio astronomy and wireless telecommunication system using the transistor fabricated. Developed essential points:

- Use of new pseudophormique InP transistors to high electron mobility Improved noise.
- Extend the band of interest: design of UWB systems.
- Use other LNA Circuit topologies broadband or ultra-wideband.

APPENDIX 1

Review of S-parameter

- Relationship of b_i and a_i: $b_i = \Gamma_i a_i$

- Expressions for b_1 and b_2 at reference planes:

$$b_1 = S_{11}a_1 + S_{12}a_2$$
$$b_2 = S_{21}a_1 + S_{22}a_2$$

- Definitions of S_{ii}:

$S_{11} = \frac{b_1}{a_1}$ for $a_2 = 0$, i.e., input Γ for output terminated in Z_o.

$S_{21} = \frac{b_2}{a_1}$ for $a_2 = 0$, i.e., forward transmission ratio with Z_o load.

$S_{22} = \frac{b_2}{a_2}$ for $a_1 = 0$, i.e., output Γ for input terminated in Z_o.

$S_{21} = \frac{b_1}{a_2}$ for $a_1 = 0$, i.e., reverse transmission ratio with Z_o source.

- Definitions of Γ_L, Γ_s, Γ_{in} and Γ_{out}:

$\Gamma_L = \frac{Z_L - Z_o}{Z_L + Z_o}$, the reflection coefficient of the load

$\Gamma_s = \frac{Z_s - Z_o}{Z_s + Z_o}$, the reflection coefficient of the source

$\Gamma_{in} = \frac{Z_{in} - Z_o}{Z_{in} + Z_o} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}$, the input reflection coefficient

$\Gamma_{out} = \frac{Z_{out} - Z_o}{Z_{out} + Z_o} = S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s}$, the output reflection coefficient

APPENDIX 2

Principal of heterojunction

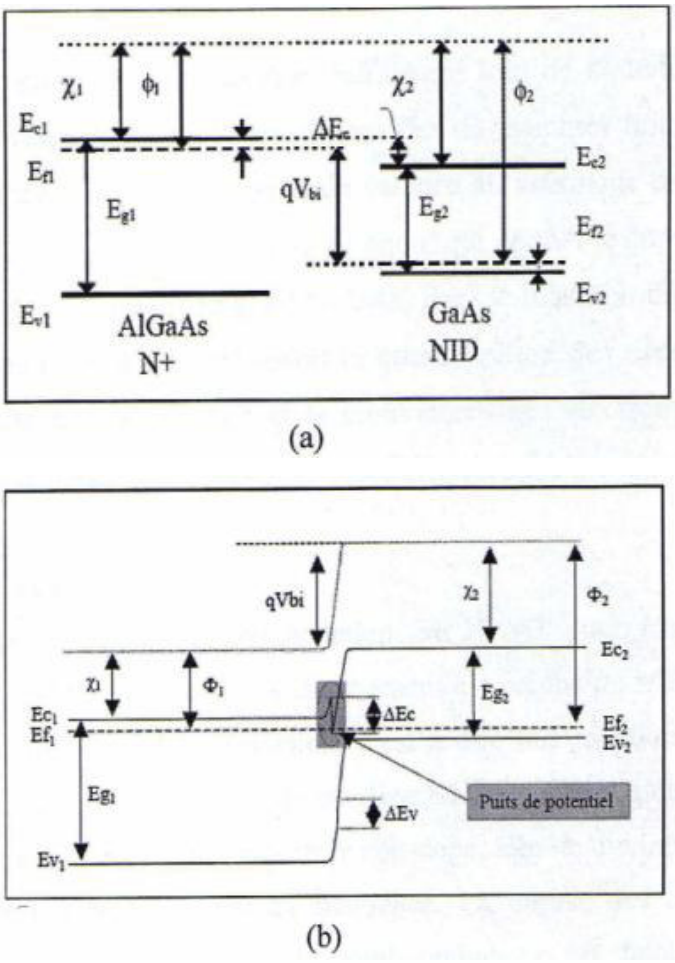


Figure A1.1: Diagramme band of heterojunction GaAs-Al_xGa_{1-x} As

APPENDIX 3