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Présentée par :

MEGHERBI MOHAMED LARBI

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Devant le jury composé de :

Dr. Sengouga Noureddine	**Professeur**	**Président**	**Université de Biskra**
Dr. Dehimi Lakhdar	**Professeur**	**Rapporteur**	**Université de Batna**
Dr. Mimi Malika	**Professeur**	**Examinateur**	**Université de Mostaganem**
Dr. Athmena Noureddine	**Maitre de Conférences 'A'**	**Examinateur**	**Université de Batna**
Dr. Saadoune Achour	**Maitre de Conférences 'A'**	**Examinateur**	**Université de Biskra**

Abstract

In this work, different experimental current-voltage behaviours of several Al implanted 4H-SiC p-i-n diodes are investigated by means of numerical simulations in a wide range of currents and temperatures. Some devices for which recombination and tunnelling are the dominant current processes at all biases are classified as “leaky” diodes. The well-behaved diodes, instead, show good rectifying characteristics with a current conduction due to tunnelling below 1.7 V, recombination between 1.7 V and 2.5 V, and diffusion processes above 2.5 V. At higher current regimes, a series resistance in excess of $1 m\Omega cm^2$ becomes the main current limiting factor. Depending on the relative weight between the contact resistances and the internal diode resistance, different temperature dependencies of the current are obtained. A good agreement between numerical and measured data is achieved employing temperature-dependent carrier lifetime and mobility as fitting parameters.

Silicon carbide (SiC) provides an alternate solution as a radiation hard material, because of its wide bandgap and higher atomic displacement energies, for devices intended for radiation environment applications. However, the radiation tolerance and reliability of SiC-based devices needs to be understood by testing devices under controlled radiation environments. These kinds of studies have been previously performed on diodes and MESFETs, but multilayer devices such as bipolar modulated field effect transistors (BMFET) have not yet been studied. The implantation of defects on BMFET in the bulk of devices show that the degradation in device performance produced by high concentrations of traps, also, higher capture cross section has an effect on the output characteristics. Defects induced damage at the drift layer has also been examined in this thesis. It is found that damaging of the canal by ionizing radiation (induced defects) reduces the current gain as well.

Additionally, measurements has been performed on fabricated 4H-SiC PiN concern optical performance, such as dark current, photocurrent and spectral response. The performance was improved regarding the signal to noise ratio, which is the same as photocurrent to dark current ratio in this case.

Keywords: p-i-n diode, silicon carbide, device simulation, carrier lifetime, 4H-SiC, defects, BMFET, photocurrent.

Résume

Dans ce travail, différents mécanismes de transport ont été étudié. Des mesures expérimentales pour plusieurs diodes à base de 4H-SiC ont été utilisées avec implantation d'Aluminium. Ces derniers sont étudiés aussi au moyen de simulations numériques dans une large gamme de courants et de températures. Les diodes pour lesquels les courants de recombinaison et de tunnels sont les plus dominants sont classées comme " diodes de fuites ". Par contre les diodes " bien comportés ", montrant des bonnes caractéristiques de redressement avec un courant de conduction en raison d'un courant de tunnel au-dessous de 1,7 V, recombinaison entre 1,7 V et 2,5 V, et les processus de diffusion supérieure à 2,5 V. Aux régimes ou le courant est plus élevées, une résistance série de plus de $1m\Omega cm^2$ devient le principal facteur de limitation de courant. En fonction du poids relatif entre les résistances de contact et la résistance interne de la diode, on obtient différentes dépendances de température du courant. Un bon accord entre les données numériques et mesurées est atteint par la dépendance entre la température et la durée de vie d'une part et la mobilité d'autre part des porteurs de charge comme paramètres d'ajustement.

Le carbure de silicium (SiC) fournit une solution de remplacement en tant que matériau résistant au rayonnement, en raison de sa large bande interdite et des énergies de déplacement atomiques plus élevé, des composants à base de SiC seront conçues pour des applications dans des environnements de rayonnement. Toutefois, la tolérance de rayonnement et la fiabilité de ces composants doit être compris par des essais dans des environnements de rayonnement contrôlées. Ces types d'études ont déjà été étudiés sur des diodes et des MESFETs, mais des composants multicouches tels que des transistors à effet de champ bipolaires modulé (BMFET) ne sont pas encore été étudiés. A cet effet l'implantation de certains défauts dans le substrat du BMFET montre que la dégradation des performances du composant produit par des concentrations élevées de défauts ainsi des sections de capture plus élevée a un effet négatif sur les caractéristiques de sortie. Les défauts induits par radiation à la couche active (canal) ont également été examinée dans cette thèse. Il a été montré aussi que le canal est endommagé par les radiations (défauts provoqués) ionisants provoque une réduction du gain en courant.

En outre, des mesures ont été effectuées sur des diodes à base de 4H-SiC pour étudier les performances optiques, tel que le courant d'obscurité, la réponse spectrale et photocourant. La performance a été améliorée en ce qui concerne le rapport signal à bruit, qui est le même dans le cas du rapport courant photoélectrique à d'obscurité.

Mots clés : p-i-n diode, Shunt, carbure de silicium, simulation, durée de vie, 4H-SiC, défaut, photocourant.

Dedicated to My Beloved Mother,

&

All My Family

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LIST OF SYMBOLS

A	Device area, diode area
c_n,c_p	capture rate for electrons, for holes
D	diffusion coefficient
D_n, D_p	diffusion coefficient for electrons and holes
e	electron charge
e_n, e_p	emission rate for electrons, for holes
E	energy
E_A, E_D	acceptor energy level, donor energy level
E_a	activation energy
Ec	critical electric field
Eg	indirect bandgap
E_C	conduction band energy
E_F	Fermi energy
E_i	intrinsic Fermi energy
E_V	valence band energy
$\Delta E_{D;A}$	donor, acceptor ionization energy
G	generation rate
h	Planck constant
k	Boltzmann factor
J	electric current density
κ	thermal conductivity
m^*_v	electron, hole effective mass
μ	carrier mobility
n_i	intrinsic density
$N_{C;V}$	effective density of states
N_t	trap density
n	electron density
p	hole density
$\mathcal{R}$	recombination rate
R	resistance
R_{on}	specific on-resistance
R_{sh}	sheet resistance
T	temperature

T_0	reference temperature (300K)
$\tau_{R\text{-}G}$	effective lifetime of recombination or generation process
τ_v	effective electron, hole minority carrier lifetime
V	voltage
V_{bi}	built-in voltage
V_B	breakdown voltage
W	depletion region width
ΔE_g	bandgap narrowing
L_a	ambipolar diffusion length
D_a	ambipolar diffusion coefficient
τ_{HL}	high level lifetime
τ_{SC}	space charge lifetime
s_g	surface generation velocity
$s_{n,p}$	surface recombination velocity
Q	stored charge
N_t	trap density
σ_n	electron trap capture cross-section
σ_p	hole trap capture cross-section

LIST OF FIGURES

LIST OF TABLES

Contents

Introduction

Silicon carbide (SiC) is a wide band-gap semiconductor with interesting physical properties in order to realize electronic devices well suited to operate under high temperature, high-power, and/or high-radiation conditions. The potentialities of the 4H-SiC polytype, in particular, are expected to enable significant improvements to a far ranging variety of applications and systems [1-5]. However, since this is a relatively new technology, intensive efforts are still necessary to ascertain the detailed physics and the real design benefits that can be obtained by developing even simple SiC-based devices.

In short, SiC has been notoriously difficult to grow as pure and defect free as silicon. As time marches on, there are more and more breakthroughs in growing high quality SiC. However, there are still many problems in growing homoepitaxial, defect-free SiC. These defects are known to negatively affect devices that are fabricated on or near them. Micropipes, comets, and carrots are all defects that have been shown to negatively affect devices. Additional SiC morphology problems appear in the form of surface states on the substrate. These electrically active states can increase reverse leakage current. Better devices could be created if these states were eliminated. Thus, the study of SiC epitaxy and devices remains prudent to this day.

To this extent, in this thesis different forward I-V behaviours of several Al implanted 4H-SiC vertical p-i-n diodes are investigated by means of measurements and numerical simulations in a wide range of currents and temperatures. In details, diode experimental data and results of proprietary simulation software [6] are combined to extract key physical parameters, including temperature dependent carrier lifetime and mobility, which aid to differentiate the current transport mechanisms at different biases. This study could also turn useful in the design of more complex 4H-SiC power devices, such as the various JFET-based devices recently presented in literature [7-10], where p-i-n diodes are the embedded structures determining the device on and off-state characteristics. The effect of ion implantation or irradiation in SiC material has been extensively studied both electrically and structurally. However, studies for SiC devices, subjected to ion implantation or irradiation, are also needed to understand the mechanisms involved in the degradation of the electrical performance. Such studies provide information on device tolerance and threshold radiation doses, and they are important for rating devices and to improve the device design for specific applications.

In the present thesis, the effects of ionizing radiation on SiC based BMFETs have been studied. A theoretical investigation is conducted to quantify the effect of traps located at drift region in a SiC BMFET by the implantation of multiple traps with densities and cross section in a controlled region. Chapter 1 gives a background to silicon carbide and why its material properties give outstanding device performance for power devices compared to other semiconductor materials. Chapter 2 presents an overview of the PiN device. The important models and parameters used for simulation for the total forward drop of the device are presented in chapter 3. Electrical characterization and discussion are found in Chapter 4. Finally, this thesis work is concluded.

Chapter 1

Material Properties and Technology

Silicon carbide is a wide bandgap semiconductor, which has many advantages compared to the conventional semiconductors. In this chapter, the material properties of SiC is focused and show the advantages of using SiC over other semiconductor.

1.1 Historical Background

SiC was first observed in 1824 by Jacob Berzelius [11]. The properties and potential of the material were not understood at that time. The growth of polycrystalline SiC with an electric founding furnace was introduced by Eugene Acheson in 1886. He was also the first to recognize it as a silicide of carbon and gave it the chemical formula SiC. Later on, he used carbon and sand in a melting process that is still used today in an improved way known as the Acheson method.

With its polycrystalline forms, silicon carbide has long been a well-proven material in high temperature, high-strength and abrasion resistant applications. In 1955[12], Jan Antony Lely proposed a new method for growing high quality crystals witch still bears his name. The interest in SiC as an electronic material began to increase slowly from this point on. The first SiC conference was held in Boston in 1958.During the 60’s and 70’s SiC was mainly studied in the former Soviet Union.

In the year 1978 the development of SiC saw a major step; the use of seeded sublimation growth technique also known as the modified the modified Lely technique [13]. This breakthrough led to the possibility for true bulk crystal growth. In 1987, Cree Research Inc., the first commercial supplier of SiC substrates, was founded [14]. In the 1990s, the semiconductor industry concentrated strongly on the realization of unipolar devices in SiC, especially Schottky diodes. Since then, device fabrication in SiC is rapidly growing. Today many types of devices, such as blue LED’s, MOSFET’s, MESFET’s, Schottky barrier diodes, bipolar transistors, thyristors, radiation detector and temperature sensors are possible.

1.2. Crystal Structure

Silicon carbide is a wide bandgap semiconductor, which has many advantages compared to the conventional semiconductors. In this section, the material properties of SiC are focused. Some of the important parameters for device simulation and calculation are also presented with useful values, which are based on the recent literature and commercially available simulators.

1.2.1 Crystal structure

The common semiconductors occur in the diamond crystal structure (Si and Ge), the zinc blende crystal structure and the wurtzite crystal structure (for example, GaAs and other III-V compound semiconductors) even though there is a large number of different crystal structures possible in nature [15]. Silicon carbide has several stable Crystal structures.

1.2.2 Polytypism of SiC

SiC has equal parts silicon and carbon, both of which are group IV elements. The distance between neighboring silicon (a) or carbon atom is approximately 3.08 Å for all polytypes. Crystals can have many different structures; the most common are cubic and hexagonal. The carbon atom is situated at the center of mass of the tetragonal structure outlined by the four neighboring Si atoms Figure 1.1.1 The distance between the C atom and each of the Si atoms is approximately 2.52 Å. The height of the unit cell, called c, varies between the different polytypes. Therefore, the ratio of c/a differs from polytype to polytype. This ratio is 1.641, 3.271, and 4.908 for the 2H, 4H, and 6H-SiC polytypes, respectively. The polytype is a variation of crystalline material in which the stacking order of planes in the unit cell is different.

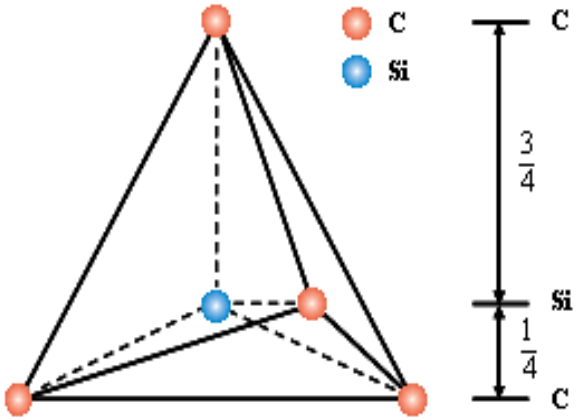


Figure 1.1.1: The tetragonal bonding of a Carbon atom with the four nearest silicon**.**

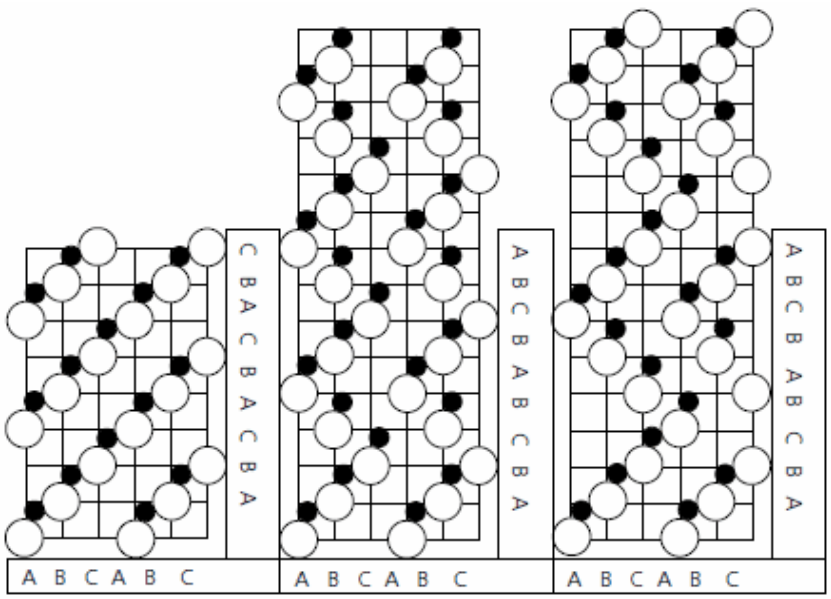


Figure 1.1.2: Stacking sequences of the crystal structure of (a) 3C SiC (b) 4H SiC, and (c) 6H SiC [16].

1.3 Production and doping of SiC single crystals

The availability of high purity and defect free on large area wafers is of vital importance for industrial development. The feasibility to produce low cost, high volume large area SiC wafers has been one of the main reasons of his success and domination in microelectronic applications. Currently SiC has not reached yet the performance of Si in terms of material quality but recent breakthrough should be a step forward allowing the fully industrialization of SiC devices and systems.

1.3.1 Bulk growth of SiC

The production of large-area defect-free single crystalline SiC substrates, i.e. bulk crystals, with well-controlled doping concentrations is one of the essential parts of realizing the full potential of SiC electronic applications. On such substrates, it is possible to grow so called epitaxial layers with uniform thicknesses and homogeneous doping over large areas.

For SiC the dominating bulk growth technique is the so-called seeded sublimation growth, i.e. the modified Lely technique. Here in a closed system, a solid source consisting of SiC powder is used and a temperature gradient transports material from the source to the seed. The growth temperatures are very high, 2000 – 2500^0 C. The size of commercially available wafers increase continually and in year 2005 wafers with a diameter of 4 inch are already on the market, however, the production of larger wafers has been also reported. In case of seeded sublimation growth the use of a solid source and the closed system makes it sensitive to depletion of the source, specifically for the Si component.

To overcome this problem the high temperature chemical vapor deposition (HTCVD) technique was developed [17]. Here gases, typically silane (SiH_4) and ethylene (C_2H_4), containing Si and C are fed into the susceptor, then decompose as they are heated and form solid particles as a mixture of Si and C. As they are heated further they sublime in a similar manner as in the sublimation growth and are transported to the seed. Since here the purification of gases is easier, the benefit of HTCVD technique is the production of high-purity material for specific applications.

1.3.2 Epitaxial growth of SiC

Bulk crystals of SiC are several cm thick thus here a trade-off between the growth rate and crystal quality must be done. The quality obtained is not good enough to be used as an active layer in a device. To solve this problem, thin layers in the 1-300 μm range are grown on top of the substrates by epitaxial growth. For this purpose, vapor phase epitaxy (VPE) is the only considered technique for SiC. This is commonly realized in a CVD reactor where the substrate is placed and source gases (SiH_4, and C_3H_8 or C_2H_4), containing Si and C are fed through [18]. An off-orientation of the surface normal of the substrate to the c-axis is preferred towards the <11-20> direction to be able to replicate the polytype [19]. An angle of 3.5^0 is employed for 6H-SiC, while 8^0 off-angle is needed for 4H-SiC. The lower requirement on growth rate allows the epitaxial growth to occur at a lower temperature of 1450–1650^0C and closer to equilibrium, leading to a higher crystalline quality [20] suitable for active layer fabrication in devices.

Note that in principle, a perfect crystal is impossible to manufacture. Even if it does not contain any impurities as extrinsic defects, some amount of intrinsic crystal defects is always present to maintain the thermodynamic equilibrium. Generally, a major distinction is made between point defects and extended defects. In SiC the most important extended defects are dislocations, stacking faults and the so-called micropipes. These kinds of defects are discussed in part two of this chapter.

1.3.3 Growth of different polytypes

Even though there exist more than 200 different polytypes of SiC, they are not equally easy to grow. The seeded sublimation growth technique is primarily suitable for the production of 4H and 6H-SiC. The largest bandgap in a thermally stable polytype is 3.26 eV in 4H-SiC.

The saturation drift velocity of carriers is higher in 4H than in 6H-SiC, making the propagation of electronic signals faster in 4H-SiC. Therefore, there is a strong emphasis on studying the properties of the 4H polytype. The technology for growing large pieces of 4H for substrate production is also favorable, although the 6H polytype is easier to grow.

3C-SiC allows highest saturation drift velocity and mobility, making it most suitable especially for fast switching power devices. Some efforts have been made to produce bulk crystals of 3C-SiC, but for

a long time no breakthrough has been achieved. This might be due to comparatively high temperatures needed for the sublimation, and that the 3C polytype is thermodynamically stable at lower temperatures. However, recently the production of 4-inch diameter, 200 μm thick 3C bulk layers with good crystalline quality was reported [21]. The layers were deposited by CVD on Si substrates at relatively low temperature ($T < 1450^0C$), below the melting point of Si.

2H-SiC is not thermally stable at common growth temperature [22] and cannot be grown in large-area stable pieces, therefore it could be only of scientific interest. Another frequently referred polytype is 15R-SiC which usually appears in common growth conditions, but is not exposed to a great attention.

This thesis deals with the 4H polytype, which are seem to be the most promising candidates for future applications.

1.3.4 Doping of SiC

When doping a semiconductor material during the crystal growth, large-area homogeneously doped wafers can be obtained with well-controlled doping concentration. However, in planar device structures a lateral separation between different parts has to be achieved. The dopants introduced during *in situ* SiC PVT epitaxial growth are aluminium and boron for p-type and nitrogen and phosphorus for n-type; with trimethylalminum ($(CH_3)_3Al$); diborate (B_2H_3), nitrogen gas N_2 and phosphine (PH_3), as the most common dopant precursors. In semiconductor processing ion implantation is the key technology for doping, besides crystal growth and thermal diffusion. Ion implantation means that electrically accelerated energetic ions are shooted into the crystal. The ion energy is usually in the range 100keV–1MeV. Implantation, as a thermally non-equilibrium process has the advantage that basically all stable elements of the periodic table can be implanted.

Therefore, in case of SiC this is the only technique suitable for selective doping with N, Al, B or P. In addition, doping concentrations and doping profiles can be adjusted reproducibly and varied over a wide range. However, as a disadvantage, ion implantation causes damage to the crystal structure, depending on the ion mass, ion energy, the implanted fluence and the fluence rate (the number of implanted ions per unit area and unit time, ions $cm^{-2}s^{-1}$). To reduce the induced damage and to electrically activate the implanted dopant species, usually high-temperature post-irradiation annealing has to be performed. The high temperature stability of SiC is a disadvantage in this case since implantation also produces some high temperature stable defects. These will be very difficult to remove, by annealing, once they are created.

As p-type dopant, aluminium is the most frequently used. It has a low diffusity in SiC over the temperature of interest; high incorporation efficiency and, compared to boron, lower acceptor ionisation energy (see Tab 1.1).The incorporation is almost linear to the flow of trimethylalminum and a maximum

doping level of about $2x10^{20}cm^{-3}$ can be reached. Boron is less used, partly due to its higher acceptor ionisation energy and lower solubility in SiC. Boron has a higher diffusity than aluminium, and a tendency to stick to the reactor walls, and subsequently evaporate. Both of these effects lead to non-abrupt doping profiles.

Type	Dopant	Ionisation energy (meV)	
		4H-SiC	6H-SiC
n	N	42(hex) 82(cub)	82(hex) 137(cub)
	P	53(hex) 93(cub)	82(hex) 115(cub)
p	B	300	310
	Al	190	225
	Ga	281	290

Table 1.1: Ionisation energies of the most common impurities in 4H-and 6H-SiC.

As n-type dopant, nitrogen is preferred to phosphorus, even though the acceptor ionisation energy is practically the same for both. The dopant incorporation is proportional to the N_2 flow, and saturates at around $1x10^{20}cm^{-3}$.

The dopants are incorporated into Si or C lattice site. A large dopant atom will preferably replace the larger Si atom in order not to distort the lattice. Aluminium and phosphorus, both with an equivalent radius comparable to that of silicon are hence regularly incorporated into Si sites.

As it can be seen from the previous sections, SiC research and processing is a complex field with many open questions. Every problem mentioned above – even more or less significant – has to be solved in order to be able to fabricate continuously operating, non-deteriorate and reliable structures. To accomplish this purpose a very important obstacle to be eliminated is to understand the structure and properties of point defects and to tailor the depth distribution of dopants and ion irradiation-induced damage in the material. Now we turn to the main scope of this thesis and first give a short introduction to the nature of point defects and defect creation mechanisms taking place during electron irradiation into SiC.

1.4 Contact creation

One of the key technical issues for a semiconductor device is the metal semiconductor (MS) contact. An ideal MS contact can either be a rectifying (Schottky) or non-rectifying (ohmic). Metal-semiconductor combinations generally upon preparation are rectifying due to the Schottky barrier at the metal-

semiconductor interface. Schottky contacts are essential for current switching and rectification. Ohmic contacts may be considered a limiting case of Schottky contacts with a modified Schottky barrier. A good ohmic contact, usually formed by depositing a metal on the semiconductor, does not perturb device characteristics and is stable both electrically and mechanically. Based on the Schottky-Moll theory of metal-semiconductor contacts the Schottky barrier high of a certain metal or its ohmic nature depends exclusively on its work function, once it is brought into intimate contact with SiC (deposited onto that). Based on the previous theory one may think that is possible to class the elemental metal layers into two groups: good ohmic or good Schottky contacts. However, the Schottky-Mott model needed a significant modification, what was done by Bardeen later by introducing the concept of surface states. It is not possible to sort the metallic contacts as Schottky or ohmic as their basic electrical behaviour depends not only on the work function of the metal, but also on several parameters, even on alloying temperature of the contacts. For example, Ni contacts on n type SiC annealed up to 600°C are Schottky contacts, however, the same contacts annealed at 900°C became ohmic [23].

N-type SiC ohmic contacts have been developed to the point where specific contact resistances on heavily doped material is now available and that processes involving silicide formation using metals such as Ni appear to lead to lowered Schottky barrier heights at the metal-semiconductor interface. N-type contacts submitted to ageing at high temperatures for long times and then characterized at room temperature indicate good thermal stability [24]. Most of the elemental metal layers deposited on n-type SiC exhibit a Schottky contact at room temperature with high barrier height [25].

P-type ohmic contacts are not as well developed or understood as n-type contacts. The very large Schottky barrier height that exists at the metal-p-type SiC interface has led to the need for extremely heavy surface doping since sufficient barrier lowering to enable ohmic contacts formation has not been achieved. Enhanced doping for the formation of p-type ohmic contacts has been achieved either during epitaxial growth, by ion implantation, or it is generally believed, by contact processes using Al and Al based alloys. On that substrate Al/Ti contacts are commonly used for ohmic contacts deposited either subsequently (Al/Ti, Al layer over the Ti layer) or simultaneously (Al-Ti) [26-28]. For Schottky contact purposes on p-type SiC, tungsten is a promising candidate [29]. Table 1.2 Reports some selected results on ohmic contacts on n-type and p-type 4H-SiC material from literature.

n-type or p-type	Metal ref	Doping(cm^{-3})	Contact resistance ρ_c (Ωcm^2)	Annealing
n-type p-type	TiC [30]	$1.3x10^{19}$	$4x10^{-5}$	950°C
	TiC	$> 10^{20}$	$6x10^{-4}$	950°C
	Ti	$> 10^{20}$	$8x10^{-4}$	950°C
n-type p-type	Ni [31]	$1x10^{19}$	$6x10^{-6}$	1050°C 10min
	Ni	$1x10^{21}$	$1.5x10^{-4}$	1050°C 10min
n-type	Ni	$1x10^{19}$	$7x10^{-6}$	950°C 30min
	[32] TiW	$1x10^{19}$	$3x10^{-5}$	950°C 30min
p-type	TiW	$6x10^{18}$	$1x10^{-4}$	950°C 30min
p-type	Ni/Al [33]	$3\text{-}9x10^{18}$	$5x10^{-3}$	800°C 2min
	Ni/Ti/Al	$3\text{-}9x10^{18}$	$6x10^{-5}$	800°C 2min
p-type	Ge/Ti/Al [34]	$4x10^{18}$	$1x10^{-4}$	600°C 30min
p-type	Al-Ti [29]	$5x10^{18}$	$2x10^{-4}$	1000°C 2min
n-type	Ni/C [35]	$3x10^{19}$	$1x10^{-6}$	700°C 2h
	Ni/C	$1x10^{17}$	$8x10^{-5}$	900°C 2h

Table1.2: Specific contact resistance measurements on 4H-SiC from literature.

1.5 Oxidation

As with the Si technology, SiC can be obtained in different ways such as thermal oxidation and CVD. SiC surfaces can be thermally oxidized using dry and wet oxygen at around 1000°C in the same way as Si. It has been also found that the oxidation of all SiC polytypes is much lower than that of Si. It normally takes a much longer time to get the same thickness on SiC than Si under the same conditions. Another unique characteristic in the oxidation rates are different between the silicon face and the carbon face .i.e. the

oxidation depend on the crystal orientation of SiC, thus SiC shows an anisotropic oxidation [36]. The SiO_2 /Si interface plays a crucial role in the development of MOS devices. To build high performance MOS devices in SiC, The SiO_2/Si needs to be improved. For years, the progress has been hampered by problems with the gate oxide, reflecting in very poor channel-carrier mobility and oxide reliability. A lot of research effort have been poured into the improvement of quality SiO_2/Si interface in SiC. A figure of merit in MOS devices can be described in terms of their interface state and fixed charge densities. Dynamic improvement have recently been reported with nitrided SiO_2-SiC interfaces [37,38], leading to improved reliability and to recently reported values for inversion-layer mobility in 4H-SiC of about 50cm^2/vs [39].

2. Major defects in SiC

Ever since large electronic grade SiC substrates became available they have been plagued with persistent defects which limit performance or reliability and which have been difficult to remove. This includes both structural defects such as stacking faults, dislocations and micropipes, electrically active point defects and a poor quality of the interface between SiC and SiO2 and other candidate dielectrics for MOS devices. A steady improvement in the defect density control has been observed in the recent years, and nowadays wafers with diameters up to 3" or even 4" are commonly available from different suppliers, with a very low defect density in comparison with the first attempts to grow wafers with the same diameter.

2.1 Crystal Imperfections

2.1.1 Bulk defects

2.1.1.1 Micropipe

Micropipe defects are the major obstacles to the production of high performance SiC devices. Micropipes are defects unique to the growth of SiC. They are physical holes that penetrate through the entire crystal and replicate into the epitaxial layer. They become “killer defects” if they are found on the active region of the device [40]. Fig 1.2.1 is a picture of a micropipe defect, which was obtained using a Nikon AFX-II microscope with a 1000x lens [41].

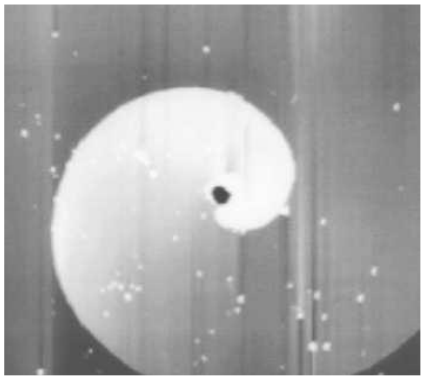


Figure 1.2.1: Micropipe defect [41]

2.1.1.2 Dislocations

Dislocations are one-dimensional line defects and they extend through the entire lattice. There are two main types of dislocations, with screw and edge character. The specification depends on the mechanism of their formation and the so-called Burgers vector **b**. The dislocation is a local distortion of the crystal and due to stress. It is required to move by one lattice constant. An edge dislocation is formed by removing from the crystal a half of atoms plane terminating on the dislocation line and then joining the two planes in the way to restore order in the crystal, see Fig1.2.2.

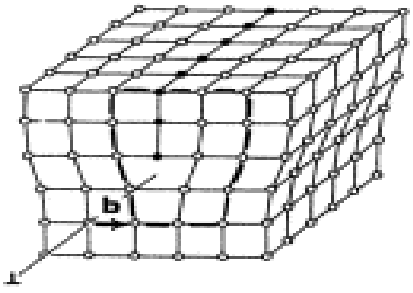


Figure1.2.2: Edge dislocation

A screw dislocation can be explained in the following manner. The crystal has been slipped above the dislocation line by a lattice vector parallel to the line and then rejoined to the part below the dislocation line to restore crystalline order, see Fig1..2.3.

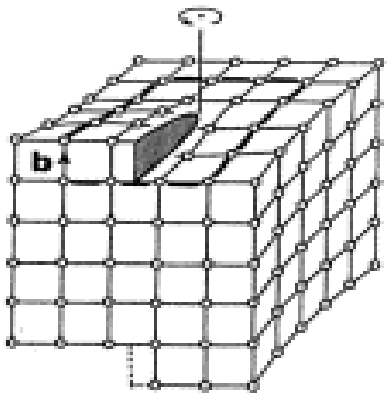


Figure1.2.3: Screw dislocation

2.1.1.3 Stacking faults

Stacking faults (SFs) are planar defects and they mostly exist in the primary slip plane, which, for SiC is {0001}.In principle, three types of SFs can exist in hexagonal system.

2.1.1.4 Low angle grain boundaries

Low-angle boundaries near the crystal periphery tend to form with the growth of large-diameter crystals grown under non optimized process conditions. In SiC substrates, low-angle boundaries are visible between the magnitude of this burgers as void-like linear crystallographic features extending radially inward from the wafer edge and generally following low-index planes. They can sometimes extend through the entire thickness of the wafer. Recent work has resulted in a dramatic reduction in these defects, current research and development substrates up to diameters of 100 mm are now produced without these low angle grain boundary defects.

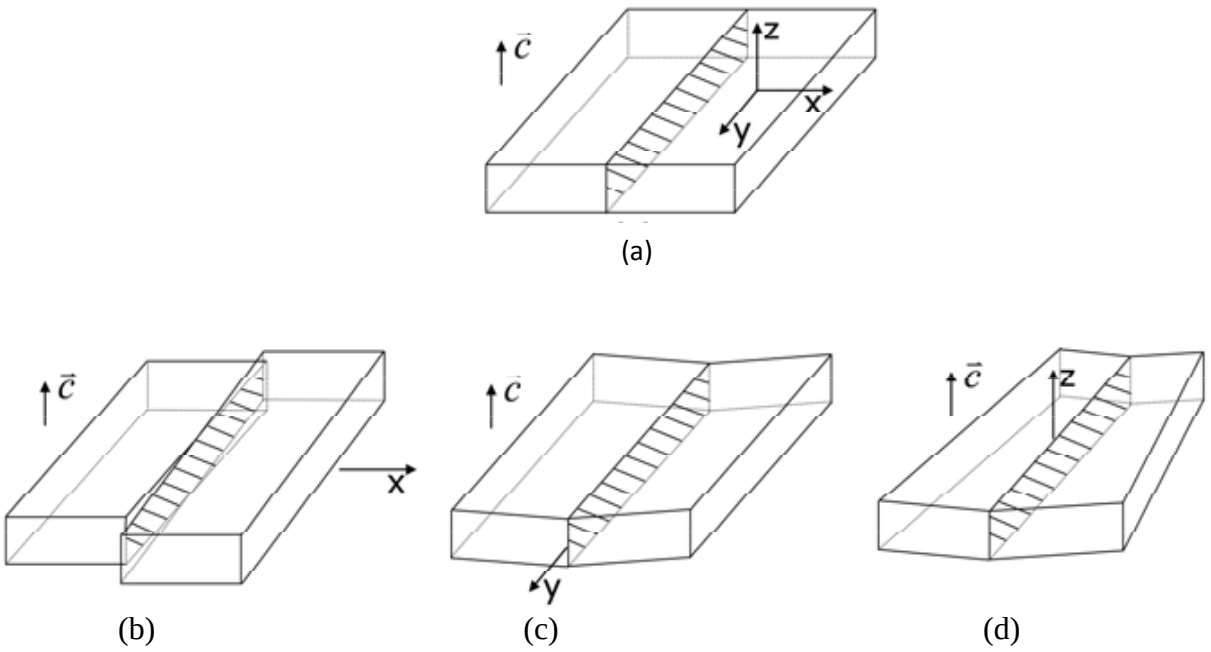


Figure 1.2.4: Schematic diagram showing three types of domain misorientation. (a) Perfect crystal; (b) twisted grain boundary; (c) basal plane tilt boundary, (d) prismatic plane tilt boundary.

2.1.1.5 Other planar defects

Defects with a triangular or hexagonal shape that can be created by inclusions of foreign polytype. They can be easily identified with an optical inspection because they show well– defined boundaries and color changes. Inclusions of the same polytype but with different orientation of the crystallographic axes have been reported [42, 43].

2.2 Epitaxial defects

A detailed study has been performed on SiC epilayer, with optical microscope investigation and spectroscopic techniques, in a way similar to that followed for the bulk analysis. Two types of defect were identified: etch pits and comets.

2.2.1 Etch pits

Etch pits can be generated during the epitaxial growth by means of an H_2 etching on the surface. They generally appear like holes, with a hemispherical depression on the surface. Etch pits have a diameter comprised between 1 and 10 micrometers, and the thickness is on the order of a few hundred nanometers. They can show a lighter color than micropipes, when observed by an optical microscope.

Wafers purchased recently from different suppliers are free from etch pits on the surface. A more refined polishing of the surface is generally the main reason of this improvement in the wafer's quality.

2.2.2 Comets (or carrots)

This defect is like a comet constituted by a "head" and a "tail". Comets are passing through the entire epilayer in a transversal direction.

This defect can be originated during the growth by an aggregation of micropipes, or merely by micro particle detachments from the reactor walls, with their subsequent interaction with the growing surface.

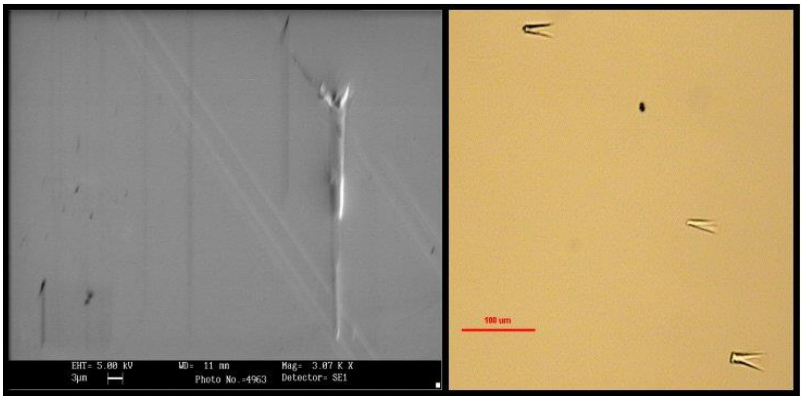


Figure.1.2.5: S.E.M and optical images of a group of comets. [44]

2.3 Point Defects

Three kinds of point defects can form in SiC, which are vacancies, interstitials and antisites. A vacancy is an unoccupied site for an atom or ion in a crystal [45], as shown in Figure 1.2.6. In 4H-SiC, both Si and C-vacancies may form in different charged states (charge states of the atoms surrounding the unoccupied site) depending on whether the SiC is *n*–type or *p*-type.

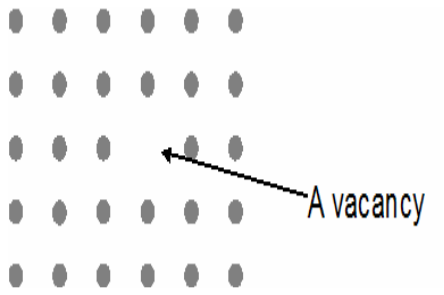


Figure 1.2.6: Schematic of a vacancy in a crystal.

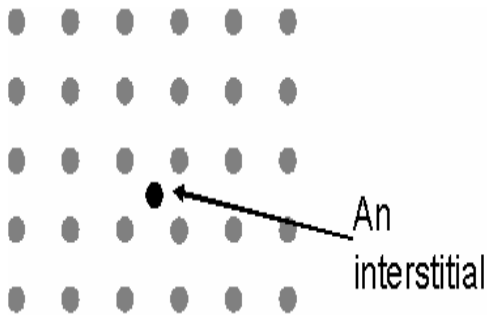


Figure 1.2.7: Schematic of an interstitial in a 2-D 2-D crystal.

A crystal lattice can be modeled by spherical atoms or ions between which there is empty space [46]. An interstitial might be an impurity or self-interstitial, i.e. a C or Si interstitial in the SiC crystal, as shown in Figure1.2.7. An interstitial might be an impurity or self-interstitial, i.e. a C or Si interstitial in the SiC crystal.

An antisite is a defect where, for a binary compound, a crystal site is occupied by the wrong species (Figure1.2.8). For instance, if in SiC, a C lattice site is occupied by a Si atom, then this is called a Si antisite, and if in SiC, a Si lattice site is occupied by a C atom, and then this is called a C antisite.

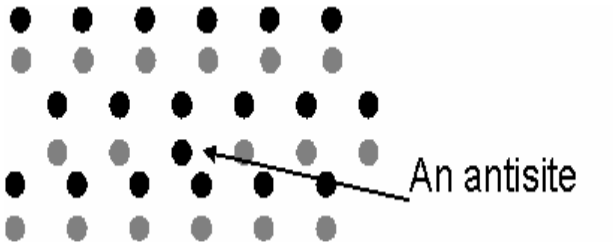


Figure 1.2.8: Schematic of an antisite in a 2-D crystal.

2.4 Shallow and deep levels

In addition to the classifications above, it is common to group defects according to the localized bandgap states they give rise too. States that have energies close to either the valence (E_V) or conduction band edges (E_C) are usually called shallow levels, whereas states with energies that are far from both the bands are called deep levels.

The classical examples of shallow defects are impurities with (shallow) donor or (shallow) acceptor states, due to the loosely bound electron or hole around them.

2.5 Defect charge states and formation energies

Let us consider a deep center, with the energy level E_T located in the bandgap and with a uniform concentration of N_T defects cm^{-3} over the semiconductor material (see Fig.2.4). There are four processes describing the dynamic behavior of the deep state, namely the individual capture and emission processes of both electrons and holes, with corresponding emission and capture coefficients (probability per unit time) of e_n, e_p, c_n, and c_p (see Fig. 2.9).

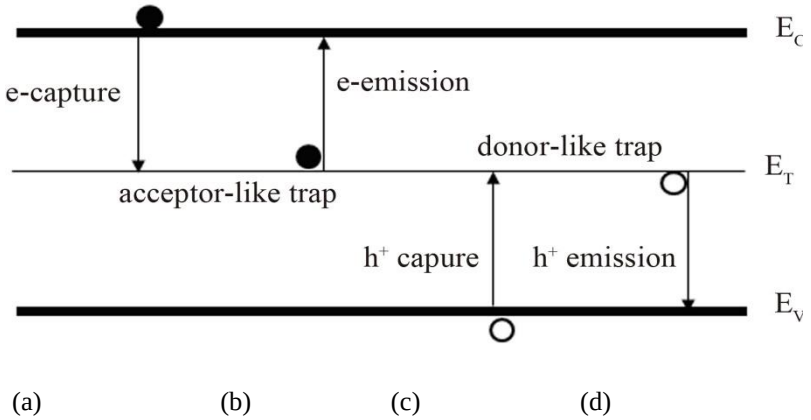


Figure 1.2.9: Emission and capture processes to and from a deep level located in the bandgap of a semiconductor.

Let us mark the capture of an electron from E_C to E_T as event (a) and the emission of an electron from E_T to E_C as event (b). Similarly, the capture of a hole from E_V to E_T is event (c) and the emission of a hole from E_T to E_V is event (d). Now four different processes can be considered (see Fig.1. 2.9):

1. Recombination: event (a) is followed by event (c)
2. Generation: event (b) is followed by event (d)
3. Trapping electrons: event (a) is followed by event (b)
4. Trapping holes: event (c) is followed by event (d)

The occupancy of the state E_T is determined by competing emission and capture processes. Electrons can be emitted and holes can be captured at the n_T states occupied by electrons and holes can be emitted and electrons can be captured at the (N_T-n_T) states occupied by holes. If the trap has a degeneracy factor g_0 when empty and g_1 when occupied by one electron, it can be shown that in thermal equilibrium the electron and hole emission is written as [47]:

$$\frac{e_n}{c_n} = \frac{g_0}{g_1}\exp\left(\frac{E_T - E_F}{KT}\right) \quad and \quad \frac{e_p}{c_p} = \frac{g_1}{g_0}\exp\left(\frac{E_F - E_T}{KT}\right) \tag{2.1}$$

Where E_F is the Fermi level in the material and g_0 and g_1 are degeneresance factor. Roughly speaking, if $E_F > E_T$, $c_n > e_n$ and $e_p > c_p$ so that the state is occupied by electrons, whereas when $E_F < E_T$ the state is empty.

Many defects can introduce more than one deep level in the bandgap. These are usually denoted +/++, 0/+, -/0, --/-, etc., where the first symbol represents the charge state of the defect when an electron is bound to it, and the second one is the charge state of the empty level.

The important property of deep levels is the ability to influence carrier lifetime significantly even at low concentrations. According to Shockley-Reed-Hall [48, 49] statistics, the minority carrier lifetime (for a single deep trap) is given by:

$$\tau = \frac{c_p(p_0+p_1)+(n_0+n_1)}{c_n c_p N_T(n_0+p_0)} \qquad (2.2)$$

Here n_0 and p_0 are the electron and hole densities at thermal equilibrium, and n_1 and p_1 are the electron and hole densities for the case that the Fermi level E_F is at the energy position E_T of the deep level.

It can be shown [50] that τ depends sensitively on the position E_T of the deep level in the bandgap. If we consider two defect centers with energy level difference of 0.4 eV, the lifetime at room temperature will be determined by the deeper level even if its concentration is six orders of magnitude lower than the concentration of the shallower level. This is mainly due to the exponentially decreasing probability of thermal reemission from the defect for deeper levels.

2.6 The role of deep levels

Presence of deep-level defects as efficient carrier traps can seriously affect the performance of some semiconductor devices, which depend on long minority carrier lifetimes.

2.7 Prominent 4H-SiC intrinsic defect centers

2.7.1 Z1/2

The so called Z1/2 center is, associated to EH6/7, the only deep level found in significant concentration in n-type as-grown 4H-SiC [51–53,54].. The concentrations of these two centers are both inversely related to the minority carrier lifetime, as well as the nitrogen donor concentration, and for a while it was uncertain which defect center was the dominant in limiting the lifetime [55,56]. Klein et al. performed DLTS and lifetime measurements on a series of 4H-SiC epitaxial layers of increasing thickness, and observed that the Z1/2 concentration was very strongly correlated with the inverse effective lifetime [57]. Moreover, this center has large, almost equal capture cross sections for both electrons and holes in the low 10^{-14} cm^2 range making it an efficient recombination center. In contrast, the concentration of the EH6/7

center showed no such correlation. The lifetime is no longer limited by the Z1/2 center below a concentration of $1-2\times10^{13}cm^{-3}$ [58], and it has been speculated that structural defects or surface recombination may dominate in this regime.

The Z1/2 center actually gives rise to two different centers and each yields two different DLTS peaks corresponding to two charge state transitions with closely spaced energy levels [59]. Due to their negative-U property only a direct transition from the neutral to the doubly defect(s) is then believed to migrate out from the irradiated spot and leave behind Z1/2 and other defects in a radial lateral distribution. During such experiments employing a low energy (< 300 Kev) electron beam, Steeds et al. [60] observed that photo luminescence lines corresponding to silicon vacancies stayed within the irradiated area, while interstitial-related centres were observed to migrate outside the directly irradiated area. This, coupled with the low energy, which should only generate damage on the C-sublattice, points to the carbon vacancies as the migrating defect, in contradiction to that concluded in the context of oxidation enhanced annealing of Z1/2.

2.7.2 EH6/7

The EH6/7 levels, like theZ1/2 level, are typically found in as-grown material at concentrations of around $10^{12} - 10^{13}$ cm^{-3}, which further increases greatly due to electron and proton irradiation, and ion implantation [51–53].They are positioned quite deeply in the band gap, about 1.65 eV below the conduction band edge, and have large electron capture cross sections estimated to approx. $10^{-13} - 10^{-14}$ cm^2 extrapolated from an Arrhenius plot, and larger than 5×10^{-15} cm^2 when measured by varying the filling pulse width during DLTS measurements [61]. The EH6/7 levels have been argued to be acceptor-like due to the lack of observed temperature shift of the DLTS peak with different applied electric field [62,63], and a recent study has unambiguously shown that Z1/2 is a double acceptor level while EH6/7, or EH7, is donor-like [68].

The DLTS peak is rather broad and consists of two closely overlapping levels, EH6 and EH7. Because of this, and since they usually appear together, these overlapping levels are sometimes treated together, despite having different behavior, e.g. mainly EH7 is generated by low-energy (80-300 Kev) electron irradiation, while both are generated at higher energies, indicating that EH7 is most likely due to an elementary carbon-related point defect while EH6 is due to a more complex cluster [65]. In fact, the EH7 and Z1/2 levels are now considered to be different charge states of the carbon vacancy, from a comparison of the energy levels of VC, Z 1/2 and EH7, and the fact that both VC and Z1/2 exhibit negative-U behavior [64].

The evidence for the involvement of carbon in this level is compelling and mostly based on the same arguments as for Z1/2; its formation is suppressed by increasing the C/Si ratio during CVD growth [56], EH7 is observed after electron irradiation at energies below the threshold for damaging the Si sublattice [65, 66] and both EH6 and EH7 exhibit highly enhanced annealing following either carbon implantation [67] or thermal oxidation [63, 68, 69]. These results indeed support the involvement of VC in the EH6/7 level.

Some studies have also reported that the concentration of Z1/2 and EH6/7 increases with increasing C/Si ratio, and with increasing nitrogen content [70, 71], although most growth studies seem to agree on the opposite dependence on the C/Si ratio.

As already mentioned, the EH6/7 levels are generated in similar concentrations (about 1:2) as the Z1/2 center by radiation, and their annealing behavior is also very similar [65, 72]. Both have very high thermal stabilities, persisting up to 2000 ◦C, and anneal out in multiple stages. The final dissociation energy for EH6/7 has been estimated as at least 7.5 eV [72]. Although the EH6/7 levels are known to be intrinsic, they have also been observed to exhibit electric field assisted annealing following MeV ion implantation with either N or C, where the annealing changes character depending on the implanted species [73]. This manifests itself as an instability in the EH7 level when subjected to reverse bias at 700 K, e.g. during high-temperature DLTS measurements. EH7 irreversibly decreases in N-implanted and increases in C-implanted material, while little change is observed for the EH6 level. The EH6/7 levels have also been observed long distances from a point irradiation performed with protons, just like the Z1/2 and S1/S2.

2.7.4 S1/S2

The S1/S2 levels consist of the S1 level at Ec-0.45 eV and the S2 level at Ec-0.71 eV, with capture cross sections 8×10^{-17} and 3×10^{-15} cm^2, respectively, measured by pulse width variation [16,19,20,62] [51,74,72,75]. David et al. found that they appear in a nearly 1:1 relationship following both low and high energy electron and proton irradiation, after a post-irradiation anneal at about 200°C, both with formation energies established as about 1 eV [75]. Their decaying amplitudes also closely match during annealing, with an activation energy for the decay Ea =1.8 eV and a prefactor c_0 =1×10^{11} s^{-1}. No electric field dependence on the DLTS peak positions have been found, possibly indicating that the levels are acceptor-like. Due to the 1:1 correspondence both in as-irradiated material and after annealing, David et al. argued that these levels most likely correspond to different charge states of the same defect center. This is further supported by the much smaller electron capture cross section for S1, which could indicate that the center is acceptor-like and capable of capturing two electrons since a capture of the first electron leads to a negatively charged center and therefore a much lower capture rate of the second electron due to columbic repulsion.

It has also been shown that these levels appear after annealing at room temperature for several months, and that the annealing is accelerated both by an applied reverse bias [74] and recombination enhanced during hole-injection either through a p+/n-junction or by illumination with above-band gap light [76].

The recombination enhanced annealing is not entirely a thermal, as the annealing rate decreased with decreasing temperature below room temperature. The fact that both the S1 and S2 levels display these relatively rare properties was regarded as further evidence that they do correspond to different charge states of the same defect center. The levels start to anneal out at temperatures above 250 ˚C.

Upon performing low-energy focused beam electron irradiation, Alfieri et al. observed the S1/S2 levels, along with Z1/2, up to distances of several hundred μm away from the directly irradiated area [77].

Chapter 2

Physics and basic equations of PiN-Diodes

Most power diodes are pin-diodes, i.e. they possess a middle region with a much lower doping concentration than the outer p- and n-layers enclosing it. Compared with unipolar devices, pin-diodes have the advantage that the on resistance is strongly reduced by high-level injection in the base region, which is known as conductivity modulation. Hence pin-diodes can be used up to very high blocking voltages. The base region is not intrinsic, as suggested by the name. The intrinsic case – doping in the range of $< 10^{10}$ cm^{-3} – would not only be difficult to attain by technology, extremely low doping would cause essential disadvantages in the turn-off behavior and other properties. Power diodes usually have a p+n−n+ structure, hence the so-called i-layer is actually an n−layer. Since it is several orders of magnitude lower than the doping of the outer layers, the name pin-diode has become the usual denotation in almost every case.

From the viewpoint of application, power diodes can be distinguished into two main types:
Rectifier diodes for grid frequency of 50 or 60 Hz: the switching losses play a subordinate role, and there is a high carrier lifetime in the middle layer.
Fast recovery diodes that work as freewheeling diodes for a switching device or that are in the output rectifier after a high-frequency transformer. They have to be generally capable of switching frequencies of up to 20 kHz and in switch-mode power supplies of 50–100 kHz and more. In fast diodes manufactured from silicon, the charge carrier lifetime in the middle low-doped layer has to be reduced to a defined low value.

2.1 Structure of the pin-Diode

With respect to structure and technology, pin-diodes can be classified into two types. For pin-diodes using epitaxial technology (epitaxial diodes, Fig. 2.1a), first, an n−-layer is deposited by epitaxy on a highly doped n+-substrate. Then, the p-layer is diffused. With this process a very small base width w_B down to some micrometres can be created, whereby the silicon wafer is thick enough by the substrate to allow production with low wafer breaking and at high yield. By implementing recombination centers – in most cases by gold diffusion – very fast diodes can be realized. Since w_B is kept very small, the voltage drop across the middle layer is low. Epitaxial (epi-) diodes are mainly applied for blocking voltages of between 100 and 600 V; however, some manufacturers also produce 1200 V with epi-diodes.

Because the costs of the epitaxy process are notable, diodes for higher blocking voltages – usually

1200 V and above – are fabricated by diffusion. For a diffused pin-diode (Fig. 2.1b), one starts with a low-doped wafer in which the p+-layer and the n+-layer are created by diffusion. The thickness of the wafer now is determined by the thickness w_B of the middle n−-layer and the depths of the diffusion profiles. The required w_B is small for lower voltages. With deep n+-and p+-layers the wafer thickness can be increased again, but deep p-layers have disadvantages regarding the reverse recovery behavior. The processing of such thin wafers is challenging. Infineon has introduced a technology for handling very thin wafers, down to a thickness of 80 μm in the manufacturing process. With this technology, also freewheeling diodes for 600 V with shallow p- and n+-border layers can be fabricated as diffused diodes.

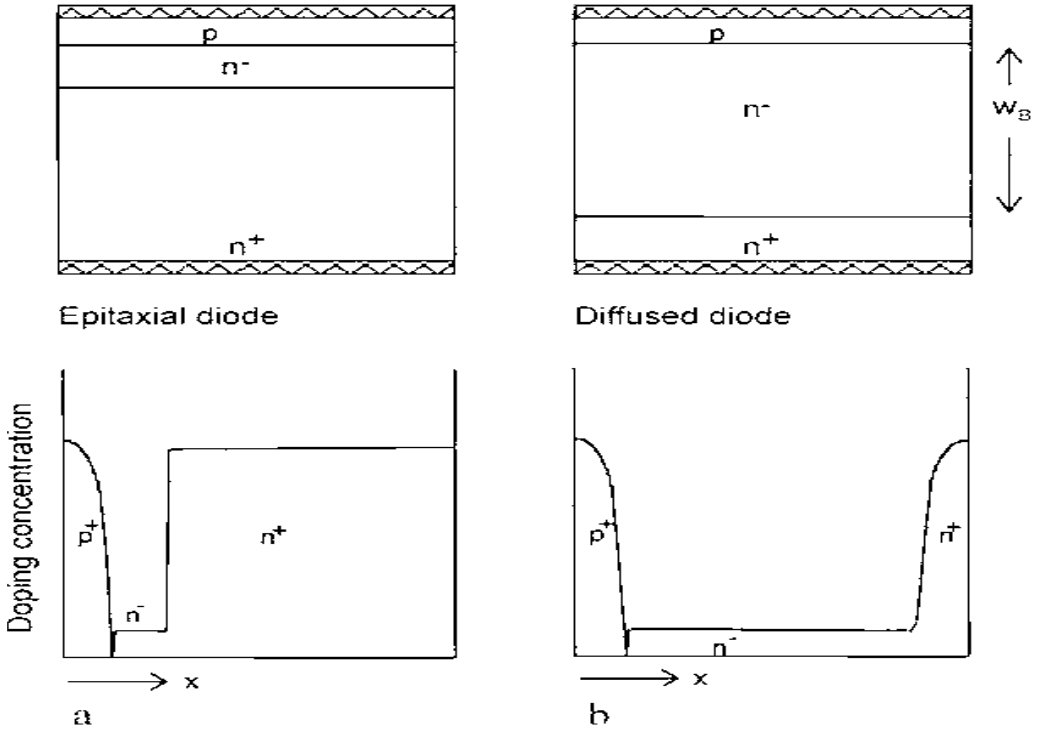


Figure 2.1: Structure of pin power diodes. (a) Epitaxial diode. (b) Diffused diode

2.2 Forward Conduction Behavior

The basic one-dimensional PiN rectifier structure is illustrated in Fig. 2.2 together with the electric field profile when reverse biased and the carrier distribution profile when it is forward biased. A punch-through i-region design is favored for PiN rectifiers due to the conductivity modulation of the drift region in the on-state. The breakdown voltage for such regions is provided in reference [78]. When this junction is forward-biased by the application of a negative bias to the N-region, holes and electrons are injected into the drift-region as illustrated in Fig. 2.2. The carrier distribution n(x) can be obtained by solving the continuity

equation for the N-region:

$$\frac{dn}{dt} = 0 = -\frac{n}{\tau_{HL}} + D_a \frac{d^2 n}{dx^2} \tag{2.1}$$

Where D_a is the ambipolar diffusion coefficient and τ_{HL} is the high level lifetime in the drift region.

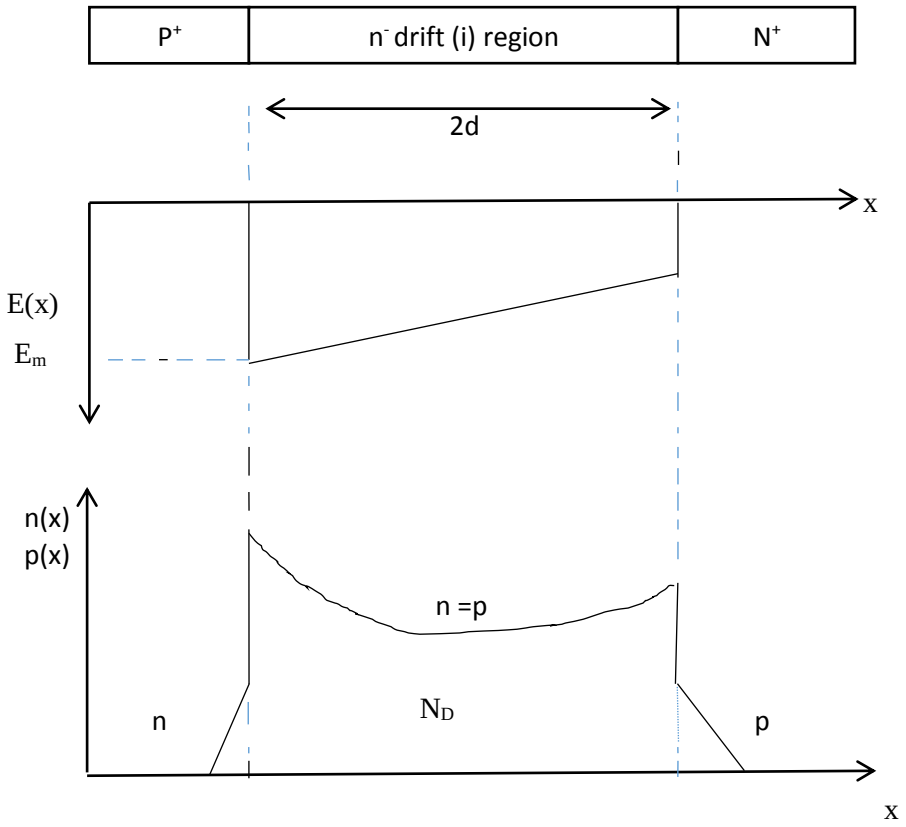


Figure 2.2: Electric Field and Carrier Distribution for a PiN Rectifier.

The solution for this equation using appropriate boundary conditions [78] yields:

$$n(x) = p(x) = \frac{\tau_{HL} J_F}{2 q L_a} \left[\frac{\cosh(\frac{x}{L_a})}{\sinh(\frac{d}{L_a})} - \frac{\sinh(\frac{x}{L_a})}{2\cosh(\frac{d}{L_a})} \right] \tag{2.2}$$

The catenary carrier distribution described by this equation is illustrated in the figure 2.2. In this expression, the ambipolar diffusion length is given by:

$$L_a = \sqrt{D_a \tau_{HL}} \qquad (2.3)$$

The forward current density J_F can be related to the on-state voltage drop V_F after taking into account voltage drops in the middle (i) region and the two junctions.

The forward voltage drop of a pin junction rectifier consists of the drop across the middle region (V_m) and the drops across the two end junctions according to

$$V_F = V_{P+/i} + V_m + Vi/_{N+} \qquad (2.4)$$

Where $V_{P+/i}$ and $Vi/_{N+}$ are the voltage drops across the anode and cathode junctions respectively and their sum can be expressed [79] as

$$V_{P+/i} + Vi/_{N+} = (kT/q) \ln (n(-d)\, n(+d) / n_i^2) \qquad (2.5)$$

Where n (-d) and n (+d) are the electron concentrations at the anode and cathode junctions respectively. The mid-region drop, V_m, depends strongly on carrier recombination lifetimes and can be expressed as transcendental functions of d/L_a [79], approximately,

$$Vm = (3kT/q)\,(d/L_a)^2 \qquad \text{for } d < L_a \qquad (2.6.a)$$

$$Vm = (3\pi kT/8q) \exp (d/L_a) \qquad \text{for } d \geq L_a \qquad (2.6.b)$$

Where 2d is the middle drift layer width and L_a is the ambipolar diffusion length.
Combining Eqs. (2.5) and (2.6), we can get [79]

$$J_F = (2\, q\, D_a\, n_i / d)\, F (d/L_a) \exp (q\, V / 2\, k\, T) \qquad (2.7)$$

Where F (d/L_a) is a function of d/L_a and V_m but not a function of the current density [80], and no end recombination is assumed. We can observe that Eq. (2.7) has a strikingly resemble to the I-V relation of a conventional pn junction under high-level injection.

The off-state leakage current of a silicon junction rectifier is dominated by the space-charge generation current, which is

$$J_{gen} = qn_iW / \tau_{eff} \propto n_i \sqrt{V} / \tau_{eff} \quad (2.8)$$

Where the effective generation lifetime τ_{eff} contains both bulk space-charge generation lifetime, τ_{SC}, and surface generation velocity, s_g. Also, W becomes constant once the mid-region is completely depleted. The switching of the junction rectifier can be modeled with a charge-control model and unlike the low voltage diodes; the switching from the forward to reverse conditions usually goes through a constant di/dt ramp [80].

2.3 Emitter Recombination and Effective Carrier Lifetime

To calculate the influence of emitter recombination on the forward characteristics of a pin-diode, we introduce an effective carrier lifetime τ_{eff} by [81]

$$\int_{-\infty}^{\infty} \frac{\Delta p}{\tau_{eff}} dx = \int_{-\infty}^{\infty} \frac{\Delta p}{\tau_p} dx \quad (2.9)$$

By this definition, τ_{eff} is a mean carrier lifetime of the structure including the emitter recombination. The integration extends from a point deep in the p+-region ($x = -\infty$) over the base to a point deep in the n+-layer ($x=\infty$). In the base where the injection level is high, the excess hole concentration Δp is equal to $p = n$, and in the p+-region the recombination rate $\Delta p/\tau_p$ can be equated to the minority recombination rate $\Delta n/\tau_n(n+) \approx n/\tau_p$. To realize the importance of the effective lifetime for device characteristics, we use the continuity equation which in one-dimensional form can be written as

$$-\frac{\delta j_p}{\delta x} = q.\frac{\Delta p}{\tau_p} + q.\frac{\delta \Delta p}{\delta t} \quad (2.10)$$

Since the hole current deep in the p+-region equals the total current ($j_p(-\infty) = j$), and deep in the n+-region is zero ($j_p(\infty) = 0$), the integration of Eq. (2.10) yields

$$j = q.\int_{-\infty}^{\infty} \frac{\Delta p}{\tau_p} dx + q.\frac{d}{dt}\int_{-\infty}^{\infty} \Delta p.dx \quad (2.11)$$

Inserting Eq. (2.9) and multiplying with the area, one obtains

$$I = \frac{Q}{\tau_{eff}} + \frac{dq}{dt} \tag{2.12}$$

Where I denotes the current and Q the stored charge of excess carriers: $Q \equiv qA \int \Delta p dx$. Equation (2.12) is a generally valid equation of charge dynamics. For a stationary forward current I_F, it takes the form:

$$Q_F = I_F \,.\, \tau_{eff} \tag{2.13}$$

Where QF is the stored charge for this special case. According to Eq. (2.13), the effective lifetime can be directly determined by measuring Q_F for a given forward current I_F.
We evaluate the effective lifetime now in dependence on device parameters and on the stored charge or the mean concentration $.p$ in the base region. By splitting up the integration interval on the right-hand side of Eq. (2.9) into the three neutral regions with constant lifetime one obtains into the three neutral regions with constant lifetime one obtains (see Fig. 2.3)

$$\frac{1}{\tau_{eff}} \int_{-\infty}^{\infty} \Delta p dx = \frac{1}{\tau_n} \int_{-\infty}^{x_p} n dx + \frac{1}{\tau_{HL}} \int_{L}^{R} p dx + \frac{1}{\tau_p} \int_{x_p}^{\infty} p dx \tag{2.14}$$

The equilibrium minority carrier concentrations and likewise the contributions of the space charge layers from x_p to L and from R to x_n are neglected on the right-hand side. Since the integrals are proportional to the respective stored charges, Eq. (2.14) can be written as

$$\frac{Q}{\tau_{eff}} = \frac{Q_n(p^+)}{\tau_n(p^+)} + \frac{Q_B}{\tau_{HL}} + \frac{Q_p(n^+)}{\tau_p(n^+)} \tag{2.15}$$

where Q_B denotes the stored charge in the base, $Q_n(p^+)$, $Q_p(n^+)$ are the stored charges of minority carriers in the p+- and n+-regions, respectively, and $Q = Q_B + Q_n(p^+) + Q_p(n^+)$ denotes the total stored charge. Because of the low injection in the end regions and the relative small minority carrier diffusion length, the stored charges $Q_n(p^+)$,$Q_p(n^+)$ are small compared with the stored charge $Q_B = q \,.w_B.\bar{p}$, if the base width is not too small and the injection level not extremely high.

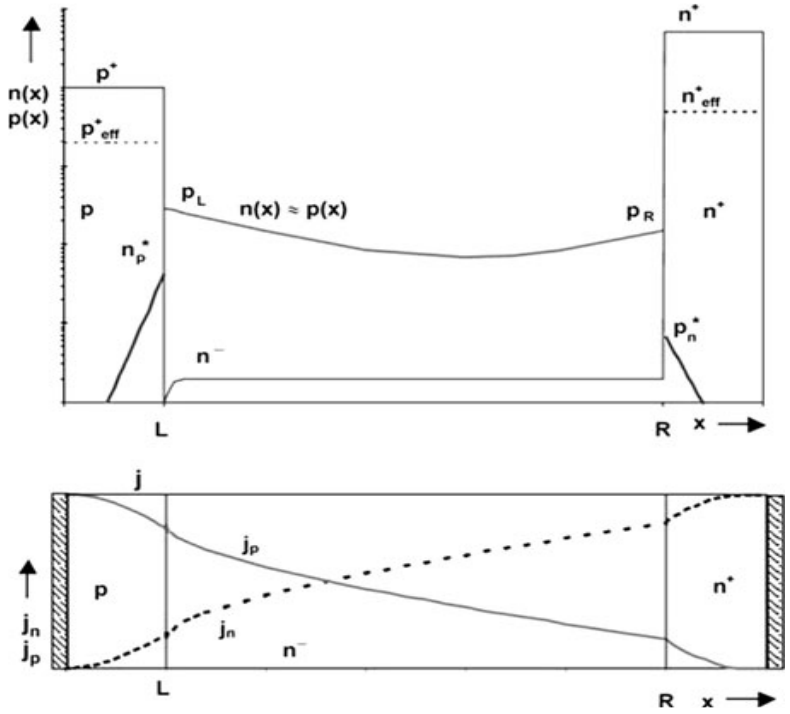


Figure 2.3: pin-Diode with consideration of recombination in the border regions

Equation (2.15) shows that in spite of the small stored charges $Q_n(p^+)$,$Q_p(n^+)$, the recombination in the end regions can be significant if the lifetimes $\tau_{n}(p^+)$, $\tau_{p}(n^+)$ are correspondingly smaller than $\tau_{HL.}$ The latter can be caused by Auger recombination, a high density of recombination centers in the outer layers or by a design of the end regions leading to high surface recombination [82, 83].Insertion of the exponential minority carrier distribution in the first and third integrals on the right side of Eq. (2.14) yields the connection with the emitter parameters (see [84], Eqs. (3.43), (3.100) and (3.101)) and neglecting the equilibrium density p_{n0}:

$$\frac{1}{\tau_p}\int_{x_n}^{\infty} p\,dx = \frac{L_p}{\tau_p}(n^+).p_n^* = \frac{L_P}{\tau_p}\frac{P_R}{n^+}e^{-\Delta E_g/KT} = h_n.P_R^2 \qquad (2.16)$$

The bandgap narrowing ΔEg results in an enhancement of the minority carrier concentration p_{n}^* and hence of the emitter parameter h_n. The analogous equation holds for the recombination integral over the p+-region (first term on the right-hand side of Eq. (2.14)):

$$\frac{1}{\tau_n}\int_{-\infty}^{L} n dx = \frac{L_n(p)}{\tau_n(p)}.n_p^* = \frac{L_n}{\tau_n}\frac{P_L^2}{p^+}e^{\Delta E_g/KT} = h_p.P_L^2 \qquad (2.17)$$

If the integral on the left side in Eq. (2.14) is approximated by $w_B . \bar{p}$, neglecting the stored minority carrier charges in the end regions, one obtains from Eq. (2.14)

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{HL}} + h_p\frac{p_L^2}{w_B\bar{p}} + h_n\frac{p_R^2}{w_B\bar{p}} \qquad (2.18)$$

To correlate the mean concentration $\bar{p}$ with the concentrations p_L and p_R at the boundaries, the carrier distribution is used in the form:

$$\bar{n} = \bar{p} = \frac{1}{w_B}\int_{-\frac{w_B}{2}}^{\frac{w_B}{2}} p dx = \frac{j.\tau_{HL}}{q.w_B} \qquad (2.19)$$

One obtains

$$\bar{p} = \frac{1}{w_B}\int_{L}^{R} p dx = \frac{L_A}{w_B}.\tanh\left(\frac{d}{L_A}\right).(P_L + P_R) \qquad (2.20)$$

For simpler writing, we use again the letter d for $w_B/2$. Using Eq. (2.20), Eq. (2.18) can be written as

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{HL}} + \frac{H}{d}\left(\frac{\frac{d}{L_A}}{tanh\left(\frac{d}{L_A}\right)}\right)^2.\bar{p} \qquad (2.21)$$

Where

$$H = 2.\frac{\eta^2.h_p + h_n}{(\eta+1)^2} \qquad (2.22)$$

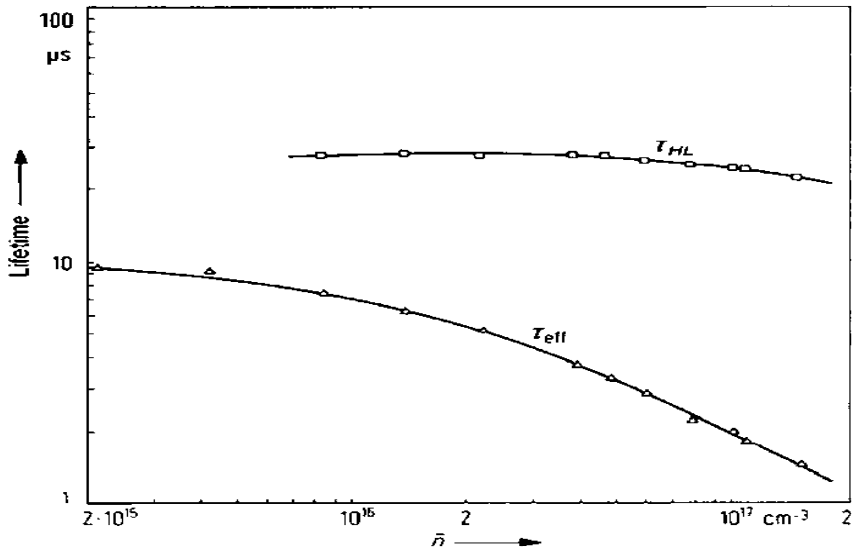


Figure 2.4: Effective lifetime τ_{eff} of a forward-biased pin-diode and lifetime τ_{HL} in the base region as functions of the mean carrier concentration in the base [85].

With $\eta = \frac{p_L}{p_R}$. The quantity *H* corresponds to a first approximation often independent of $\bar{p}$.

2.4 Reverse Blocking

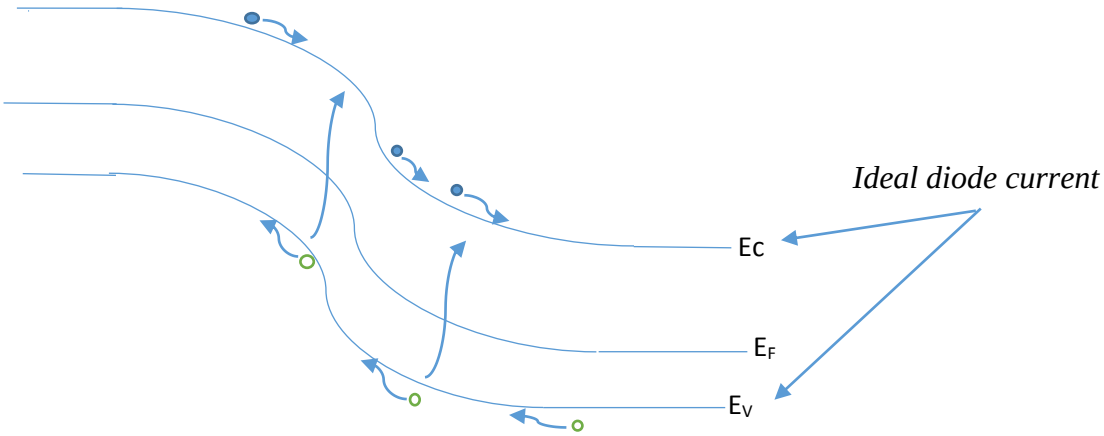


Figure 2.5: Band diagram of p-n junction under reverse bias condition

The PiN diode is designed to be used in high voltage rating application. The capability of voltage blocking depends on the doping profile and the thickness of the drift region. Differ from the Schottky diodes, PiN diodes offer much lower reverse leakage current. As illustrated from Figure 2.4, there are mainly two types of leakage current: depletion region thermal R-G current given by [87]

$$I_{R-G} = \frac{qAn_i}{2\tau_{SC}}(W - W_0) \tag{2.23}$$

Where

$$W = \sqrt{\frac{2\varepsilon(V_b - V_a)}{qN_D}} \tag{2.24}$$

And ideal diffusion current given by [86]

$$I_0 = q.A.\frac{D}{L}\frac{n_i^2}{N_D} \tag{2.25}$$

Where D is the diffusivity, L is the diffusion length.

The leakage current caused by the above two mechanism is much smaller than the one caused by the thermionic emission current across the barrier height in Schottky diode.

2.5 Transient Characteristics

When the diode is forward biased the excess carrier concentration builds up. Hence, when the device is turned off, the excess carrier must be removed before the junction goes to the blocking mode. The process of removing excess charge from the base and the resulting ability of the diode to block voltage is known as the reverse recovery phenomenon. The process consists of the sweeping out of stored charge due to the electric field, the diffusion of stored charge out of the base, and the recombination of stored charge. Once the junction can block voltage, the voltage begins to rise across the diode as the remaining stored charge decays.

2.5.1 Forward recovery

The lightly doped epilayer allows PiN diodes to support large reverse voltages, and has an important role during commutation between conducting state and blocking state, and vice-versa. It was shown in section 2.2 that the presence of epilayer during forward conduction increases on-state voltage drop with respect to signal diodes, since the epilayer behaves such as a variable series resistance connected to the diode. This resistance increases with the current density, considering the phenomena described in the last section, such as end region recombination, and so the voltage drop on the epilayer. The voltage drop due to the epilayer region is more or less in the range from 0.1 V to 1 V. Anyway, the presence of the carriers in the epilayer is the main reason that makes possible to the PiN diodes conducting high current densities.

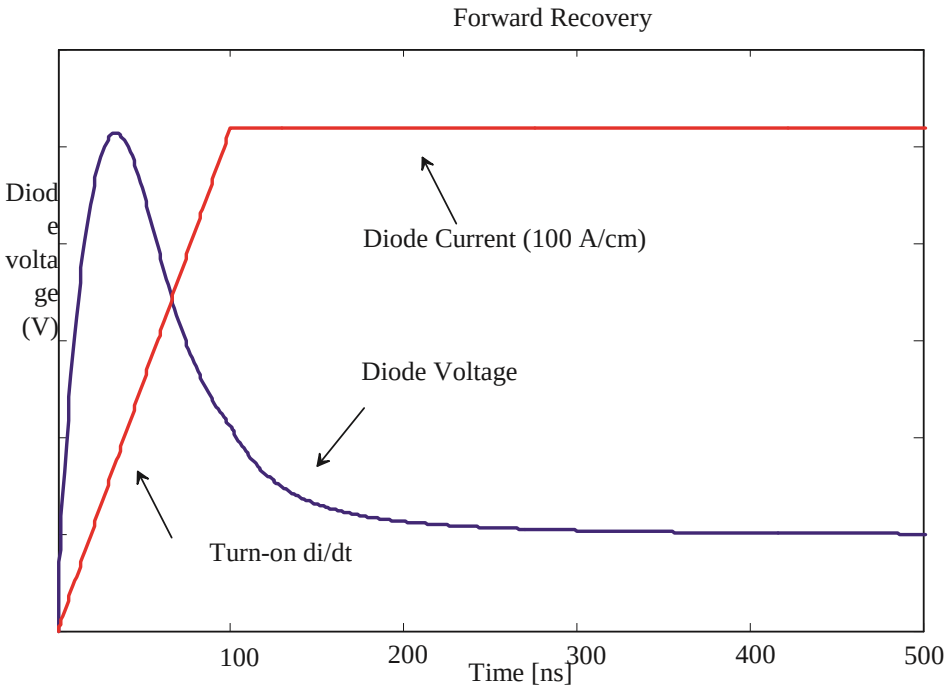


Figure 2.6: PiN diode forward recovery

For the sake of illustrating what would happen if the epilayer was unmodulated, the resistance of the epilayer is evaluated without the carriers injected in the same:

$$R_{epi} = \frac{W}{q\,\mu_n N_D} \tag{2.26}$$

Where W is the width of the epilayer, and N_D is the epilayer doping. In order to clarify the order of the unmodulated region resistance, let us consider a general diode with an epilayer 50 μm wide and with doping $N_D = 10^{14}\,\mathrm{cm}^{-3}$. One finds that its resistance is of the order of $10^{-1}\,\Omega \cdot \mathrm{cm}^2$, which means that for forward density currents equal to 100 A/cm^2, the voltage drop in the unmodulated epilayer should be in the order of 10^1 V.

This example makes clear that if a PiN diode is forced in the conducting state with a high *di/dt*, meaning that the current is increasing in a faster rate than the rate of carriers being injected into the epilayer, transient voltage drop will be much greater than steady stage voltage drop. This is due to the fact that during the first instants, when the epilayer is not modulated, its resistance is very high.

This voltage overshoot due to the fast switch from the blocking state to the conduction state through the forcing of a direct current, is called forward recovery. The voltage peak increases with increasing *di/dt*, and its value depends on how high the current has risen before conductivity modulation is fully effective.

In Fig. 2.6 an example of PiN diode forward recovery is shown, which the simulated diode is the same used for generating Fig. 2.7. It can be observed that diode voltage reaches about 5 V while steady state on-state voltage drop is about 1 V. Fig. 2.7 shows the behavior of excess carriers in the epilayer when the diode is turned on from zero current. It can be observed that excess carriers are initially injected into the regions closest to the P^+N^- and N^-N^+ junctions. From there, they diffuse into the center of the epilayer, and its resistance diminishes to its steady state value.

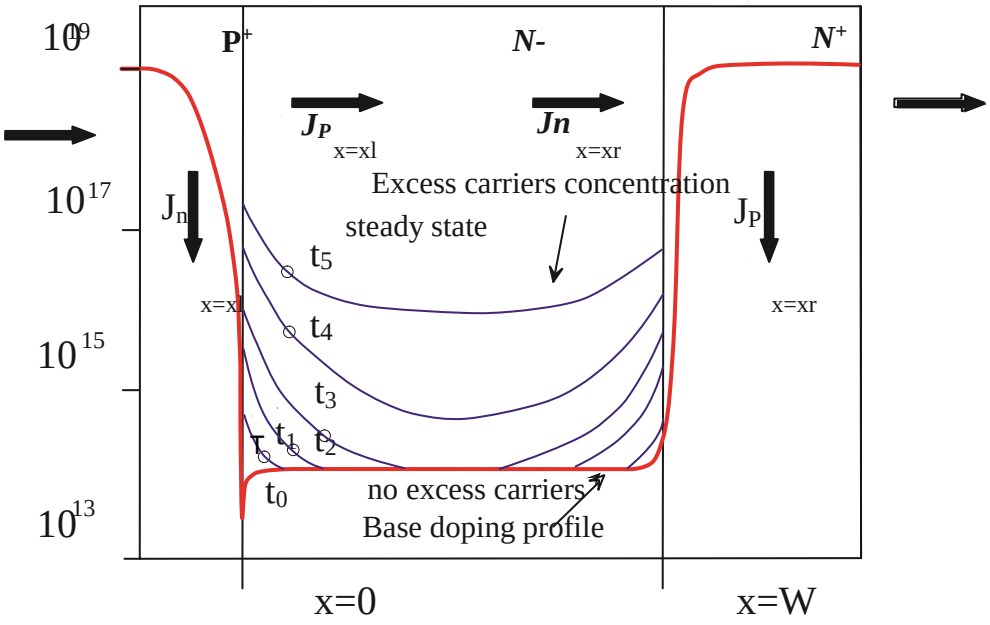


Figure 2.7: Excess carrier concentration profiles during the turn on process in PiN diode

2.5.2 Reverse recovery

A major limitation to the performance of PiN diodes at high frequencies is the loss that occurs during switching from the on-state to the off-state, which have a significant effect on the maximum operating frequency. During the reverse recovery, the charge stored in the epilayer during forward conduction must be removed. As can be seen in Fig. 1.10a, a large reverse transient current occurs in PiN diodes during reverse recovery. Since the voltage across the diode is also large following the peak in the reverse current, a large power dissipation occurs in the diode. In addition, the peak reverse current adds to the average current flowing through the switches that are controlling the current flow in the circuit. This not only produces an increase in the power dissipation in the switches, but also creates a high internal stress degrading their reliability. Moreover, reverse recovery also causes EMI phenomena.

In the following the different phases of the reverse recovery are described, regarding Fig. 2.8. The widely used diode test circuit in Fig. 2.9 is used for a better understanding of the switching process, where DUT is the diode under test, L_{DUT} is the parasitic inductance of the diode, L is the inductance of the circuit that can be considered as a constant current source, S_1 is the switch, and V_S is the supply voltage.

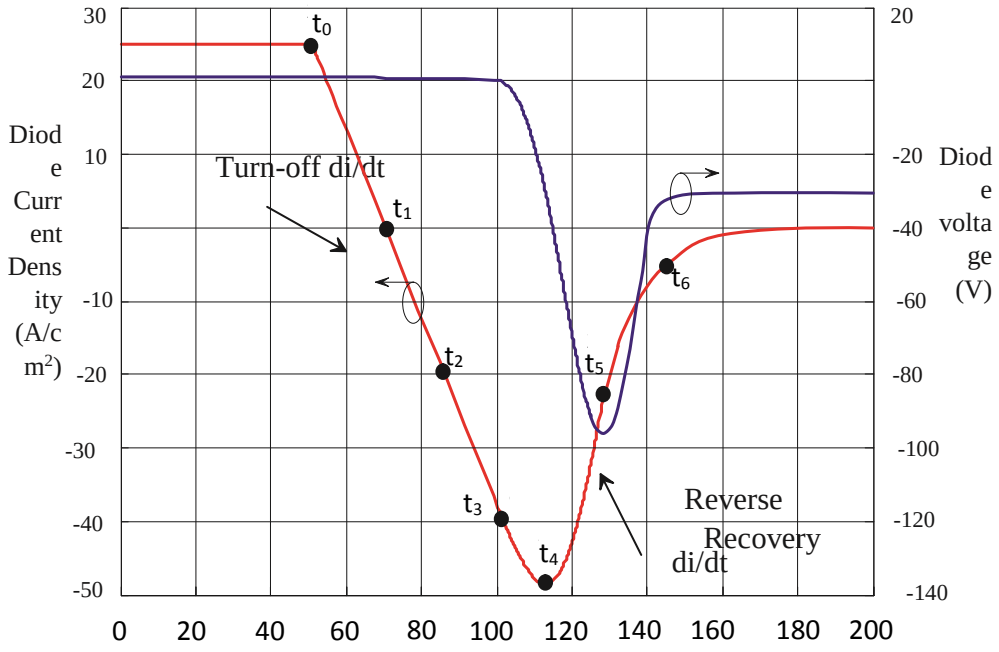


Figure 2.8: PiN diode reverse recovery: Reverse recovery current waveform

During the first phase (0, t_0) the switch in the circuit is open. The diode is in the forward conduction state, and the injected carriers are almost symmetrically distributed along the epilayer (see Fig. 2.8b, sample time t_0).

The voltage drop on the diode has its steady state value corresponding to the conduction current density through the diode.

At the time instant t_0 the switch in the circuit is closed, and the reverse recovery takes place. From t_0 until t_3 the current through the diode is determined by the external circuit conditions and decreases with a constant *di/dt*, the so called turn-off *di/dt*. Hence, the charge profile in the

epilayer during this phase is such that it is able to support an increase in current, in the reverse direction. As far as the diode is able to support this increasing current at a certain *di/dt*, there will be just a small forward voltage drop across the diode, which is determined primarily by the charge profile within the epilayer. The diode is still forward biased. During this second phase (t_0, t_3) the injected carriers in the epilayer are extracted from the diode, by diffusion and recombination, and there is a change in the slope of the injected carrier profile near the two junctions. This slope changes its sign due to the reversal in the current direction, as can be observed by time samples t_1, t_2 and t_3 in Fig. 2.9

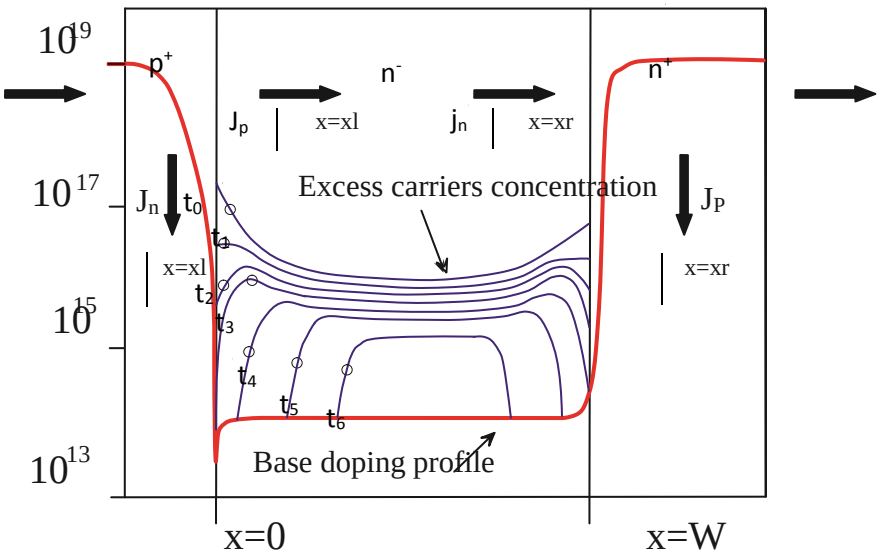


Figure 2.9: PiN diode reverse recovery: Dynamics of carrier concentration in the epilayer during reverse recovery

At the time instant t_3, when sufficient charge has recombined, or has diffused out as reverse current, the carrier's concentration at the P^+N^- junction reaches the levels of thermodynamic equilibrium, allowing the formation of a space charge region. Therefore, the voltage drop on the diode becomes negative and starts to increase. This is the beginning of the third phase (t_3,t_4), which lasts until the instant time when current through the diode reaches its peak negative value. Because of the depleting charge profile, after t_3 the diode will be unable to support an increase

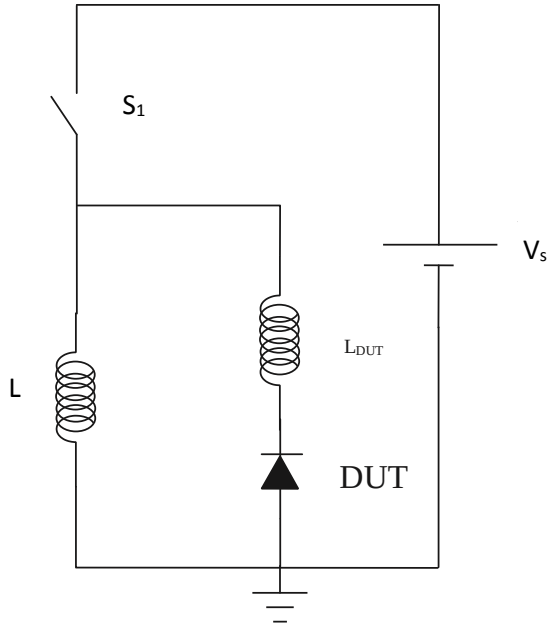


Figure 2.10:Circuit used to emulate diode switching

-in the current as determined by the circuit *di/dt*. However, it must be recognized that the diode may be able to support an increase in the current if the magnitude of the *di/dt* is reduced. At time t_3, the diode starts determining the circuit boundary conditions, being controlled by the diffusion and recombination processes in the epilayer, and it is the voltage across the diode, rather than the current that is determined by the external circuit [86], [87]. The actual time difference between the voltage becoming negative and the diode current reaching its peak negative value, that is the duration of the third phase, depends very much on the circuit conditions as well as on the diode characteristics. It can also be deduced that the diode current waveform will become more rounded near its peak negative value, because *di/dt* through the diode will first decrease and then change sign, at time t_4, when the charge carrier profile in the diode is no longer able to support any further increase in the current in the reverse direction.

During the fourth phase (t_4,t_5), after the *di/dt* has changed its sign, the depletion regions are advancing from both borders of the epilayer and the resulting reduced charge profile is just able to support lower currents. The reverse recovery *di/dt* during this phase induces an overshoot of the reverse voltage as the energy stored in the parasitic inductance L_{DUT}, always present in practical circuits, is transferred into the diode (see Fig. 2.9). This is undesirable, and good circuit designers must minimize parasitic inductances. This phase lasts until time t_5, when the diode is blocking the whole applied reverse voltage, and the reverse diode voltage reaches its peak value. If the turn on of S_1 is controlled so that the current rises gradually, initially taking over the L inductor current and then drawing reverse current out of the diode, as the space charge layer is established in the diode the reverse voltage settles at the supply voltage with no significant overshoot. We call the attention to the fact that the reverse diode current adds to the total current carried by S_1 and causes a transient peak, as already mentioned.

The last phase of the recovery starts at time t_5 and lasts until the moment in which the current reaches its saturation value. If there is a residual amount of excess charge present in the epilayer from this instant time recombination dominates the excess carrier absorption, resulting in a slow tail in the current waveform (see current waveform and excess charge during time sample t_6 in Fig. 2.9). This last phase of the recovery is very critical, and some considerations must be done. The first consideration is with respect to the applied reverse voltage. If the applied reverse bias voltage is small, the space charge region will extend only slightly inside the epilayer. As a result, there will still be a lot of excess carriers remaining in the epilayer. These excess carriers can be removed only through recombination. Hence, if the applied reverse bias voltage is less than a second one operating in the same conditions, the recombination dominated regime will be quite prominent causing a significant tail near the end of the reverse recovery process [87]. This kind of recovery is the so called soft recovery, and a behavior like this is desirable for power electronics applications.

The second and more serious consideration regards to the fact that at time instant t_5, it is possible that the depletion regions can advance through the whole epilayer and the current that is still through the diode cannot be supported by any excess charge. This is the classic snappy recovery. Depending on the rate that excess carriers are extracted from the epilayer, the current goes rapidly to zero with very high reverse recovery *di/dt* because a stronger depletion from both sides happens before the current is ceased, resulting in oscillation. The snappy recovery is detrimental to the diode, as it increases the chance of its destruction due to the excessive electric field strength. Furthermore, the large-amplitude high-frequency oscillations cause excessive amounts of electromagnetic interference (EMI).

When the switching frequency of a power circuit increases, the turn-off *di/dt* must be increased. It has been found that this causes an increase in both the peak reverse recovery current and the ensuing *di/dt*, which in turn results in less recovery time.

If the reverse recovery *di/dt* is large, an increase in the breakdown voltage of all the circuit components becomes essential, since the reverse recovery *di/dt* flows through parasitic inductances in the circuit causing the already mentioned voltage overshoot on the diode. Raising the breakdown voltage capability causes an increase in the forward voltage drop of power switches, which degrades circuit efficiency. Consequently, much of the recent work on PiN diodes has been focused upon improving the reverse recovery characteristics.

However, a trade-off between the switching speed and the forward voltage drop is essential during PiN design. This trade-off is dependent upon a number of factors such as the epilayer width, the recombination center position in the energy gap, the distribution of the deep level impurities, and the doping profile. In section 2.3 it was found that end region recombination results in an increase of voltage drop and it could be assumed that a careful design should reduce this effect (increasing the emitter efficiency, that is reducing h_p and h_n). It would assure that also under high current conditions, end region recombination is small with respect to epilayer recombination. This assumption is not correct. Actual devices tend to increase end region recombination effects, that is, to reduce end region emitter efficiency (increasing h_p and/or h_n), since the increase of end region recombination results in an improvement of dynamic behavior [86], [88], [89]. This improvement is due to the fact that the reduced carrier's concentration in the epilayer (see Fig. 2.8) takes to a faster extraction of the carriers during reverse recovery, considering the same operation conditions, resulting in less reverse current peak and faster reverse recovery, which is desirable in order to reduce switching power losses. It can be achieved through techniques like the lifetime control techniques described in section 2.3. From eq. 2.16 and eq. 2.17 it can be observed that in order to increase h_p and h_n, that is to reduce the emitters efficiency, there are two other design techniques: the reduction of end region doping (increase of minority carrier equilibrium concentration p^+_{N0} and n^+_{P0}) [86], [88], [89], and the reduction of end region thickness (W_P+, W_N+).

It can be noticed that the reduction of end region doping is always effective, as the case of the weak anode diode ,while the reduction of end region thickness has a relevant effect only if W_P+, W_N+ are smaller than minority carrier diffusion length (L_{nP+}, L_{pN+}).

Chapter 3

Modeling of 4H-SiC material properties

This chapter will describe the specific properties of device materials enter the model equations (3.1-3.5), in the form of physical parameters such as the effective intrinsic density, the transport coefficients, the electric permittivity, the heat capacity, and all the parameters appearing in (Generation-Recombination) models of SiC. Each of these parameters may depend on the state variables as well as external parameters. A widely favored pragmatic approach is to rely on phenomenological material parameter models which after careful calibration to experimental data makes it possible combine physically based predictive simulation with numerical practicability.

3.1 Introduction

Numerical device modeling and simulation are essential for analyzing and developing semiconductor device. The help a design engineer, not only gain an increased understanding of the device operation, but also provide the ability to predict electrical characteristics, behavior, and parameter-effects influence of the device. With this knowledge and abilities, the designer can design a better structure.

The increasing complexity of the structure models demonstrates that more accurate modeling generally leads to increased computational difficulties. To consider additional features that important in device design (such as non-uniform doping profiles), numerical approach simulation with the help of computers is almost a necessity. Even with these added complications, computer aided simulation is especially helpful for the analysis of a device in which two-and three-dimensional effects can have practical significance. The increased availability of low-cost, high performance computing has made device simulation widely accessible e.g. ATLAS [90]**,** MEDICI [91]**,** PSCES [92]**.**

As any device simulator, any quantitative, or even qualitative, simulation of a device relies heavily on applicable device models and their parameter values. Although several models with their default parameters are available in many commercial simulators, some of their default parameters do not provide realistic characteristics of some semiconductor materials especially in SiC material, which exists in a host of polytypes.

It is the aim of this chapter to analyze the applicability of 4H-SiC material parameters from literature and to implement them into two-dimensional program ATLAS (Silvaco) as a way to calibrate the simulation process with the real device characteristics.

It starts with a brief introduction of Atlas, followed by reviewers of recently published material concerning bulk parameters of 4H-SiC that are applicable to ATLAS. Regardless which iteration method used, the solutions are carried out over the entire grid until a self-consistent potential (ψ) and free-carrier concentrations (n, p) are obtained. Once the potential (ψ) and free-carrier concentrations (n, p) have been calculated at a given bias, it is possible to determine the quasi-Fermi levels (Φ).

3.2 Atlas device simulator

ATLAS is a two-dimensional device simulator, which solves numerically the following five basic semiconductor device equations:

The Poisson equation;

$$\varepsilon\nabla^2\psi = -q(p - n + N_D^+ - N_A^-) - \rho_s \tag{3.1}$$

The electron and hole continuity equations;

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla.J_n - U_n \tag{3.2}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q}\nabla.J_p - U_p \tag{3.3}$$

And the electron and hole current equations;

$$J_n = -q\mu_n.n.\nabla\Phi_n \tag{3.4}$$

$$J_p = -q\mu_p.p.\nabla\Phi_p \tag{3.5}$$

Where ε is the dielectric permittivity, ψ is the electrostatic potential, n and p are electron and hole concentrations, N_D^+ and N_A^- are the ionized donor and acceptor impurity concentrations, ρ_s is the surface charge density which may be present due to the fixed charge in insulting materials or charge interface;

J_n and J_p are vectors of the electron and hole current density, U_n *and* U_p are the electron and hole recombination rates, μ_n and μ_p are the electron and hole mobility's; and Φ_n and Φ_p are the quasi- Fermi potentials.

The numerical algorithms used in Atlas to solve the five basic device equations are based on the finite element method, which discretized these equations on a simulation grid. This discretization process yields a set of coupled non-linear algebraic equations that represent a number of grid points, for the unknown potentials and free-carrier concentrations. This set of coupled nonlinear algebraic equations in return must be solved by a nonlinear iteration method. Two iteration approaches, Gummel's and Newton's method are available (Appendix C and D) in ATLAS. Regardless which iteration method used, the solutions are carried out over the entire grid until a self-consistent potential (ψ) and free-carrier concentrations (n, p) have been calculated at a given bias, it is possible to determine the quasi-Fermi levels (ϕ) and the hole and electron currents (J_n and J_p) from equations 3.4-3.5.

The results of device simulations depend critically on the physical models and parameters used. A number of physical models are incorporated in ATLAS for accurate simulation, including models for recombination, impact ionization, energy gap narrowing, band-to-band tunneling, mobility and lifetime [90].

3.3 4H-SiC Bulk parameters

The following sub-sections described the important bulk models and parameters of 4H-SiC in unipolar, devices: intrinsic carrier, energy gap narrowing, impact ionization, incomplete ionization and carrier mobility.

3.3.1 Energy gap and intrinsic Carrier Concentration

The intrinsic carrier concentration n_i in a semiconductor is a fundamental parameter and high operating temperature limit. The relationship between n_i, temperature, and energy band gap is given by [90].

$$n_i = \sqrt{N_C.N_V}\exp(-\frac{E_g}{2KT}) \tag{3.6}$$

Where N_C and N_V is the effective density of states in the conduction and the valence band states, respectively given by

$$N_C = 2\left(\frac{2m_e^*.K.T}{\hbar^2}\right)^{\frac{3}{2}} = \left(\frac{T}{300}\right)^{\frac{3}{2}} N_C(300) \tag{3.7}$$

$$N_V = 2\left(\frac{2m_h^*.K.T}{\hbar^2}\right)^{\frac{3}{2}} = \left(\frac{T}{300}\right)^{\frac{3}{2}} N_V(300) \quad (3.8)$$

Where m_e^* and m_h^* is 0.76 m_0 and 1.20 m_0 respectively [94]. . Using equations 3.6 and 3.8 respectively, the N_C and N_V for 4H-SiC equal 1.66x10^{19} cm^{-3} and 3.19x10^{19} cm^{-3}, respectively at room temperature (300K).The temperature dependent energy band gap is given by

$$E_g = E_g(300) + \alpha\left[\frac{300^2}{300+\beta} - \frac{T^2}{T+\beta}\right] \quad (3.9)$$

Where α and β are fitting parameters.The effective density of states in the conduction and valence band as well as the energy bandgap at room temperature is summarized in table 3.1[95].

	4H-SiC	Si	Ge	GaAs
$N_C(300)cm^{-3}$	1.66x10^{19}	2.89x10^{19}	1.04x10^{18}	4.7x10^{17}
$N_V(300)cm^{-3}$	3.19x10^{19}	1.04x10^{19}	6.00x10^{18}	7.0x10^{18}
E_g eV	3.26	1.08	0.66	1.42
α	3.3x10^{-4}	4.73x10^{-4}	4.77x10^{-4}	5.41x10^{-4}
β	0	636	239	204

Table 3.1: Calculated parameters for different semiconductors at 300K.

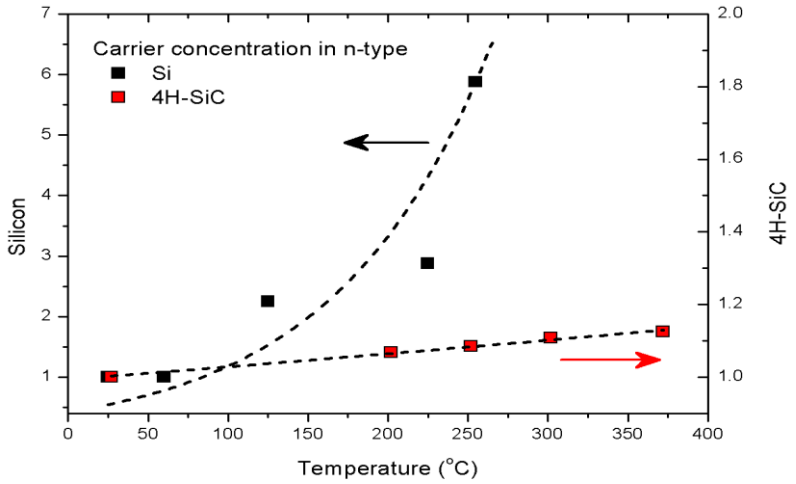


Figure 3.1: Intrinsic concentrations for Si and 4H-SiC semiconductors as a function of the temperature.

From equations 3.6, 3.7, 3.8 and 3.9, the intrinsic carrier concentration as a function of the temperature for different semiconductors having a different energy bandgap based on the calculation (see Table 3.1) was plotted in Figure 3.1. For room temperature (300K), n_i is equal to be approximately 7×10^{-7} cm^{-3} for 4H-SiC. As shown in Figure 3.1, the wider bandgap and thereby lower intrinsic carrier concentration allows SiC to maintain semiconducting behavior at much higher temperature than conventional Si and Ge semiconductors.

3.2.2 Bandgap narrowing

The modification of the density of states by heavy doping leads to an additional influence which is generally modelled by rigid shifts of the band edges, the so called "bandgap narrowing". Theoretical models for doping-induced band edge displacements and bandgap narrowing in both n-type and p-type 4H-SiC were presented by lindelfelt [96]. The model takes into account the three different electron effective mass components associated with hexagonal lattices (instead of two as in Si and Ge).The results for the band edge displacements are expressed in simple analytical form as function of doping concentration.

The band edge displacements for n-type semiconductors can be summarized with the formulas

$$\Delta E_C = A_{nc}\left(\frac{N_D^+}{10^{18}}\right)^{\frac{1}{3}} + B_{nc}\left(\frac{N_D^+}{10^{18}}\right)^{\frac{1}{2}} \qquad (3.10\ a)$$

$$\Delta E_V = A_{nv}\left(\frac{N_D^+}{10^{18}}\right)^{\frac{1}{4}} + B_{nv}\left(\frac{N_D^+}{10^{18}}\right)^{\frac{1}{2}} \qquad (3.10\ a)$$

For p-type semiconductor we get

$$\Delta E_C = A_{pc}\left(\frac{N_A^-}{10^{18}}\right)^{\frac{1}{4}} + B_{pc}\left(\frac{N_A^-}{10^{18}}\right)^{\frac{1}{2}} \quad (3.11\ a)$$

$$\Delta E_V = A_{pv}\left(\frac{N_A^-}{10^{18}}\right)^{\frac{1}{3}} + B_{pv}\left(\frac{N_A^-}{10^{18}}\right)^{\frac{1}{2}} \quad (3.11\ b)$$

The resulting bandgap narrowing ΔE_g then becomes

$$\Delta E_g = \Delta E_V - \Delta E_C \quad (3.12)$$

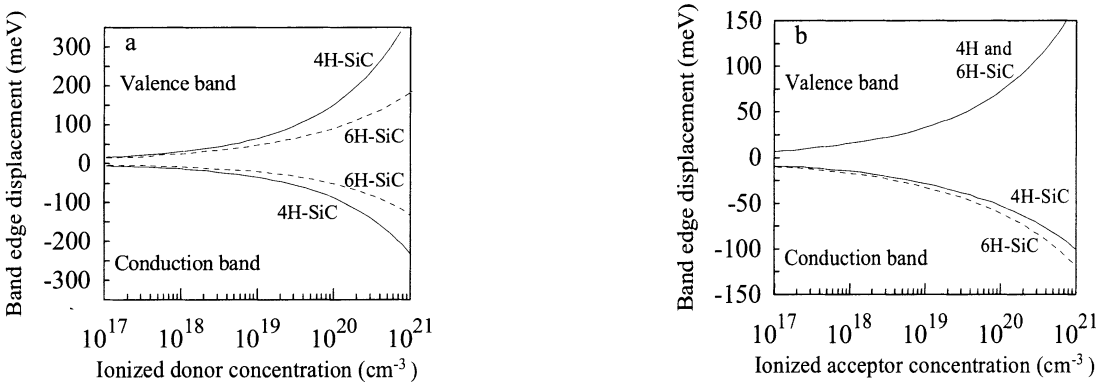
In agreement with the convention used in device modelling, the bandgap narrowing defined here is a positive quantity.

The coefficients A_{nc}, A_{pc}, B_{nc}, B_{pc}, A_{nv}, A_{pv}, B_{nv}, and B_{pv} can be adjusted in the device simulator model by introducing their values for the specific material. For 4H-SiC Lindefelt reported the values [96]:

4H-SiC n-type A_{nc}=-1.51x10^{-2}; B_{nc} = -2.9x10^{-3}; A_{nv}= 1.9x10^{-2}; B_{nv}= 8.7x10^{-3}

4H-SiC p-type A_{pc} =-1.6x10^{-2}; B_{pc}=-3.9x10^{-4} ; A_{pv}=1.3x10^{-2}; B_{pv}= 1.1x10^{-3}

Giving the band edge displacements in eV.



(a) (b)

Figure 3.2: Conduction band displacements and valence band displacements for 4H-SiC vs ionized concentration, (a) donor (b) acceptor.

Equation 3.10 and 3.11 with the parameter values given above, have been plotted in Fig 3.2.The bandgap narrowing is obtained as the energy distance between the balance band and the conduction band shifts.

3.2.3 Incomplete ionization of dopants

The controlled incorporation of shallow impurity levels acting as donors or acceptors is one of the key processes of semiconductor device technology and the resulting n-doped and p-doped regions are the basic functional components of semiconductor devices. One of the disadvantages with wide-bandgap semiconductors is that the dopant ionization levels are quite deep. Hence, the dopants are not fully ionized even at higher temperature.

The most important dopant centers for 4H-SiC have been so far nitrogen (N) acting as donor as well as aluminum (Al) and boron (B) acting as acceptors. N and other donor impurities are assumed to occupy the carbon sites, Al atoms substitute only on the Si sublattice, whereas B may substitute on both sites [94]. The carrier concentration $N^{+}_{D,\,A}$ (i.e. the number of ionized donors or acceptors) can be calculated with the following equations [97, 98]:

$$N^{+}_{D,A} = N_{D,A}\left(\frac{-1+\left(1+4g_C\left(\frac{N_{D,A}}{N_{C,V}}\right)exp\left(\frac{E_{D,A}}{KT}\right)\right)}{2g_C\frac{N_{D,A}}{N_{C,V}}Exp\left(\frac{E_{D,A}}{KT}\right)}\right) \tag{3.13}$$

$$N_{C,V} = 2.513\text{x}10^{19}.\left(\frac{T}{300.K}\right)^{\frac{3}{2}}\left(\frac{m_c}{m_v}\right)^{\frac{3}{2}} \tag{3.14}$$

Where g_C is the spin degeneracy (in this case 2 for donors and 4 for acceptors), N_C (N_V) is the density of states given by equation 3.14 with the effective density of states masses m_c or m_v $(=1\text{x}\ m_0)$ for electrons and holes, respectively, and E_D and E_A are the donors and acceptors levels m_c or m_v $(=1\text{x}\ m_0)$ for electrons and holes, respectively, and E_D and E_A are the donors and acceptors levels.

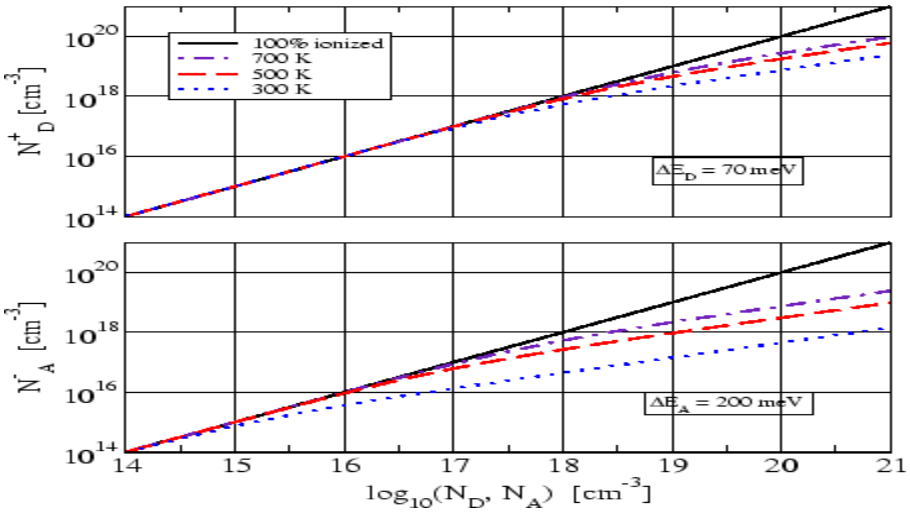


Figure 3.3: Ionization level of the donor (N) and acceptor (Al) as a function of doping concentration in 4H-SiC for different temperatures.

Using equations 3.13 and 2.14, the calculated ionization aluminum and nitrogen in 4H-SiC at 300K and 700K is shown in Figure 3.3. According to the calculation, a doping concentration of 10^{20} cm^{-3} for aluminum at 300K would only result in a carrier concentration of 5× 10^{17} cm^{-3}. Concentration 1% of the atoms have been replaced, and the bands are degenerate, resulting in much higher free carrier concentration. Therefore, the equations 3.12 and 3.14 are not quite valid for higher doping concentration than about 10^{19}cm^{-3}.

3.2.4 Recombination Models

3.2.4.1 Shockley -Read-Hall (SRH) Recombination

The recombination through defects in the bandgap is a process, which is the dominant recombination mechanism in semiconductors with indirect forbidden bandgap, such as Silicon and Silicon Carbide. It results explicitly dependent on the number of imperfections in the crystal, caused by impurities or by crystallographic defects, such as vacancies and dislocations. These imperfections originate intermediate states (see Fig.3.4) within the bandgap that act as recombination centers, or traps, for the free carriers. The theory for recombination through these localized traps was for the first time analyzed by Shockley and Read [96] and then by Hall. Their analytical model which describes the recombination rate (SRH-rate) is given by [99]:

$$R^{SRH} = \frac{np - n_i^2}{\tau_n\left[p + n_i\left(\frac{E_i - E_t}{KT}\right)\right] + \tau_p\left[n + n_i\left(\frac{E_i - E_t}{KT}\right)\right]} \quad (3.12)$$

$$\tau_n = \frac{1}{N_t v_{th} \sigma_n} \quad (3.13)$$

$$\tau_p = \frac{1}{N_t v_{th} \sigma_p} \quad (3.14)$$

Where N_t is the density of state, v_{th} is the electron thermal velocity, σ_n is called the capture cross section describing the effectiveness of the localized state in capturing an electron, σ_p is the capture cross section for holes. τ_n and τ_p are the lifetime of electrons and holes, respectively.

For conventional semiconductors, the SRH carrier lifetimes in the above equations are modelled as functions of doping and temperature by the following [100]:

$$\tau_{n,p}^{SRH} = \frac{\tau_{n_0,p_0}\left(\frac{T}{300}\right)^{\gamma_{n,p}}}{1 + \left(\frac{N}{N_{n,p}^{SRH}}\right)^{\alpha_{n,p}}} \quad (3.15)$$

Where τ_{no} and τ_{po} are the intrinsic minority carrier lifetimes, $\gamma_{n,p}$, $\alpha_{n,p}$ and $N_{n,p}^{SRH}$ are empirical modelling parameters.

At the present, poor contributes are avoidable in literature focused on the estimations of these values for Silicon Carbide, particularly for the 4H-SiC polytype. However, although for the intrinsic carrier lifetimes τ_{n_0,p_0} there is not a convergence of opinions, for the $N_{n,p}^{SRH}$ parameter it is typically used the extracted value for Silicon [101], i.e. $N_{n,p}^{SRH}$=5x10^{16} cm^{-3}.

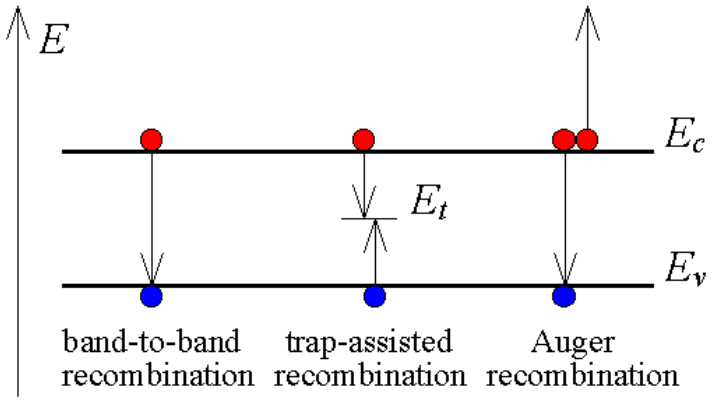


Figure 3.4: SRH recombination process.

3.2.4.2 Surface Recombination

Surface recombination can be modeled in two different ways:

- By specifying the *surface recombination velocity* parameter at the SiC/SiO2 interface (see Eq. 3.15), and then in a way similar to Shockley-Read-Hall (SRH) recombination.
- By specifying the trap distribution in the SiC bandgap at the SiC/SiO2 interface

Although the result is similar because the surface SRH model depends on the traps implicitly, the second method actually models the traps and consider the occupation and the space charge stored. If the first method is chosen, the following expression is implemented at the interface:

$$R_{surf}^{SRH} = \frac{np - n_{i,eff}^2}{(n+n_1)/S_n + (p+p_1)/S_p} \tag{3.15}$$

Where $s_{n,p}$ represents the *surface recombination velocity*, which depends on the traps implicitly.
If the second method is chosen, the following trap types can be implemented:
• *Fixed charge*, which are always completely occupied.
• *Acceptor*, which are negatively charged when occupied and neutral when unoccupied.
• *Donor*, which are positively charged when occupied and neutral when unoccupied.

In addition, the trap distribution and concentration, and its capture-cross section can be defined.
For a trap concentration N_t energetically localized at E_{trap}, the recombination rate can be expressed as:

$$R_{net} = \frac{N_t v_{th}^n v_{th}^p \sigma_n \sigma_p (np - n_{i,eff}^2)}{v_{th}^n \sigma_n (n+n_1/g_n) + v_{th}^p \sigma_p (p+p_1)/g_p} \tag{3.16}$$

In Eq. 3.16, $v_{th}^{n,p}$ are the thermal velocities, $\sigma_{n,p}$ are the capture-cross sections, $g_{n,p}$ are the degeneracy factors that are usually equal to one, and n_1 and p_1 can be expressed as:

$$n_1 = n_i \exp\left(\frac{E_{trap}}{KT}\right)$$

$$p_2 = n_i \exp\left(-\frac{E_{trap}}{KT}\right)$$

3.2.4.3 Auger Recombination

Auger recombination describes the direct recombination process of electrons and holes [102]. When excess carriers recombine in a region that has a high doping concentration the probability of direct recombination between holes and electrons may not be negligible compared to the probability of recombination through traps (SHR recombination).

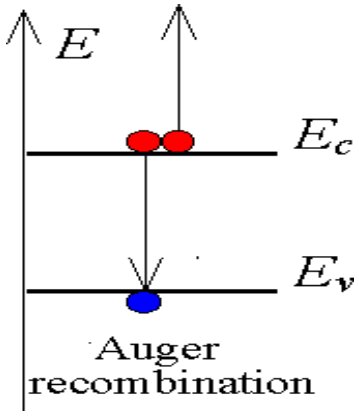


Figure 3.5: Auger recombination process.

This direct recombination process is called Auger recombination. Auger recombination, involves three particles (one electron and two holes, or vice versa). It occurs when the energy released by the recombination of an electron-hole pair is transferred to a third free carrier, as shown in Fig. 3.5.In this process, at low injection level, the expression of the recombination rate is related to the excess carrier concentration and to doping density [103]:

$$U_{Auger}^{n} = C_n \Delta_p N_D^2 \quad \text{For n-type material} \qquad (3.16)$$

$$U_{Auger}^{p} = C_p \Delta_n N_A^2 \quad \text{For p-type material} \qquad (3.17)$$

With C_n and C_p the Auger coefficients for electrons and holes and Δn and Δp are the density of electrons and holes in excess per unit volume.

Therefore, the Auger carrier lifetime at low injection level is given by:

$$\tau_{Auger}^{low} = \frac{1}{C_{n,p} N_{D,A}^2} \qquad (3.18)$$

Keeping in count that at high injection levels both carriers participate to the recombination process, the carrier lifetime at these regimes can be expressed as:

$$\tau_{Auger}^{high} = \frac{1}{C_a \Delta n^2} \tag{3.19}$$

Where $Ca = C_n + C_p$ is the ambipolar Auger recombination coefficient.

The values we used for C_n and C_p is 5×10^{-31} and 2×10^{-31} cm^6/s, respectively for n-type 4H-SiC with a doping concentration of 1×10^{18} cm^{-3} at room temperature [104].

3.2.4.3 Radiative Recombination

The radiative recombination consists of the annihilation of an electron-hole pair, which leads to the creation of a photon with energy close to that of the bandgap (see Fig.3.6). If the carrier has energy higher than that of the bandgap, the excess energy is released as thermal energy to the lattice.

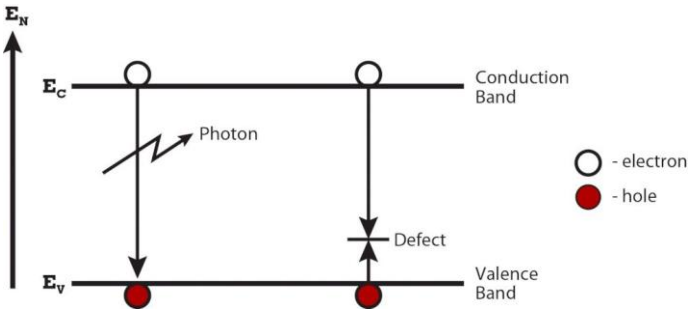


Figure 3.6: Radiative Recombination process

The radiative recombination rate depends directly on the availability of electrons and holes and it is given by:

$$U_{rad} = \beta(np - n_i^2) \tag{3.20}$$

Where β is the radiative recombination coefficient.

The radiative carrier lifetime results constant at low injection levels, while it is inversely proportional to the excess carrier density at high injection levels, as follows

$$\tau_{rad}^{low} = \frac{1}{\beta N_{D,A}} \quad (3.21\ a)$$

$$\tau_{rad}^{high} = \frac{1}{\beta \Delta n} \quad (3.21\ b)$$

Since the Silicon Carbide is an indirect semiconductor, like the Silicon, the radiative process must be assisted by a photon and a phonon in order to simultaneously preserve momentum and energy.
This makes the radiative recombination for SiC much less probable respect to the others recombination mechanisms.

3.2.4.4 Effective Lifetime

With different intensity, depending on the semiconductor topology and technology, all the above recombination mechanisms conjunctly contribute to the final effective carrier lifetime, whose value can be evaluated by the following:

$$\tau_{eff} = \frac{1}{\tau_{SRH}^{-1} + \tau_{rad}^{-1} + \tau_{Auger}^{-1}} \quad (3.22)$$

3.2.5 Impact Ionization

The acceleration of free carriers within a high electric field finally results in generating free carriers by impact ionization. This process corresponds to the inverse process of Auger recombination. It is modelled by the reciprocal of the mean free path which is called the impact ionization coefficient.
The corresponding avalanche generation rate can be expressed by [105, 106]

$$\int_0^w \alpha_n(x)\, exp\left[\int_x^w \left(\alpha_n(x) - \alpha_p(x)\right) dx\right] dx = 1 \quad (3.23)$$

The impact ionization coefficients are modelled by:

$$\alpha_n(x) = a_n exp\left[-\frac{b_n}{E(x)}\right] \quad (3.24\ a)$$

$$\alpha_p(x) = a_p exp\left[-\frac{b_p}{E(x)}\right] \quad (3.24\ b)$$

The critical field with an impurity concentration of $10^{15}cm^{-3} < N_D < 1\ 0^{18}cm^{-3}$ can be calculated by:

$$E_{cr} = \frac{E_{CR,Ref}}{1-\frac{1}{4}log10\left(\frac{N_D}{N_{Ref}}\right)} \quad (3.25)$$

Presently, there is only one report available on measured impact ionization coefficients at different temperatures [103].

	$a_n(cm^{-1})$	$b_n(v/cm)$	$a_p(cm^{-1})$	$B_n(v/cm)$
4H-SiC	$3.44x10^6$	$2.58x10^6$	$3.24x10^6$	$1.9x10^6$

Table 3.2: Average impact ionization coefficients of electrons and holes 4H-SiC.

Generally, the impact ionization coefficients of electrons are significantly smaller than those of holes. A review of the published data on impact ionization coefficients has been first published by Ruff et al. [106,107]. The extracted average parameter set (Tab. 3.2) is exceeded by newer measurements [106, 108], which yield an about 20% larger critical electric field.

It is important to note that the measured data rely on uniform avalanche breakdown with all possible influence of structural defects and edge termination excluded. There is experimental evidence that elementary screw dislocations reduce the breakdown voltage of a pn-junction [109, 110].

Considering such findings and the spread of measured data, the average parameters seem to be a good base for numerical simulations which should be calibrated to the applied process technology.

3.2.6 Mobility

It is well known that an accurate I-V model is strongly based on physical and accurate mobility and velocity saturation. The free carrier mobilities are the transport parameters relating the gradient of the quasi-Fermi potential to the corresponding current flow (see Eq. (3.4-3.5)). They are derived from relaxation times τ_v^{rel} which describe the average time between the scattering events of free carriers. Assuming a single isotropic scattering process,

they can be defined by:

$$\mu_v = \frac{q\tau_v^{rel}}{m_v^*} \tag{3.26}$$

However, there are various scattering mechanisms (see Fig3.7) which determine the free carrier mobilities such as acoustical and optical phonon scattering, piezoelectric and polar scattering, ionized and neutral impurity scattering as well as scattering at vacancies, dislocations, and surfaces. Due to the complex nature of these mechanisms, phenomenological models have been developed for the various experimentally observed mobility phenomena in Si devices [111]. The contributions from different scattering processes can be combined using the simple Mathiesen rule [112].

$$\frac{1}{\mu_v^{low}} = \sum_i \frac{1}{\mu_v^i} \tag{3.27}$$

provided that they can be considered as independent mechanisms. Due to the diagonal form of the mobility tensor of α–SiC, this concept can also be applied to its independent components in the principal axes system. However, a rigorous modeling of the anisotropic properties of α–SiC will be a challenge to semiconductor transport theory. A first attempt to calculate the anisotropy of the Hall mobility in n-type α–SiC based on detailed information about the band structure is reported in [113].

The transport parameters of semiconductors may significantly depend on the process technology. Therefore, reported mobility data from the period before wafers with a defined polytype in acceptable quality were available can hardly be used to investigate state-of-the-art devices. Hall measurements of the bulk epitaxial free carrier mobility tensor components of 4H- and 6H-SiC have been reported by Schaffer et al. [113] and Schadt et al. [114].

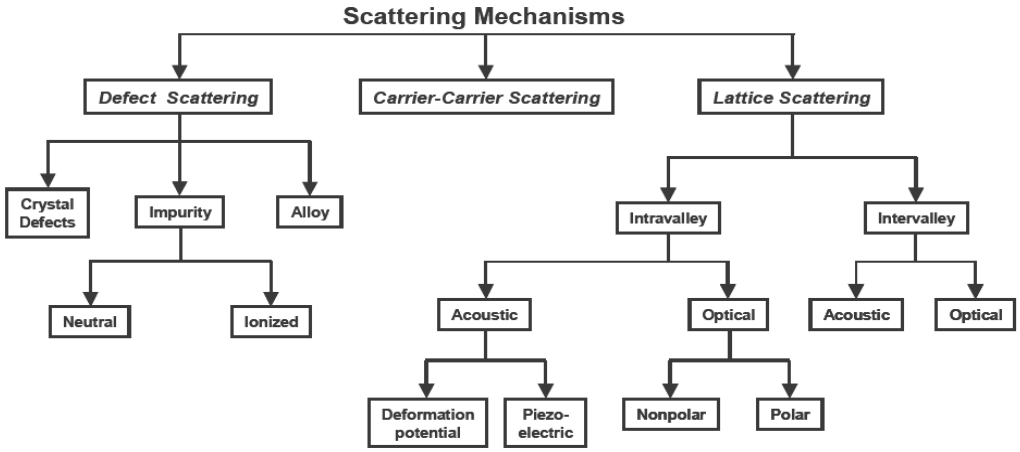


Figure 3.7: Schematization of the principal scattering mechanisms

Because of their crystallographic structure, the α-SiC polytype are characterized by an anisotropy of the principal electro thermal parameters. Although, in general, anisotropic parameters result expressed by second rank tensors, for 4H- and 6H- polytypes they are reduced to a diagonal form [115], so that it is possible to use the following convenient representation for the electron mobility:

$$\begin{bmatrix} \mu_{\perp} & 0 & 0 \\ 0 & \mu_{\perp} & 0 \\ 0 & 0 & \mu_{/\!/} \end{bmatrix}$$

Actually an complete modelling of anisotropic properties does not exist; since the most of SiC devices are realized on wafers with surface orthogonal, or lightly rotated, to c-axis ([0001] direction), it is common rule to define an anisotropic ratio between base-plane and the [0001] direction. Following this observation, because the commonly measured mobility is orthogonal to c-axis ($\mu_{\perp}$) while the parallel component is generally not equal, the ratio between these components is derived by experiment.

3.2.6.1 Acoustic-phonon and ionized-impurity scattering

The measurement results of Schaffer et al. [110] for $\mu_{\perp}$ of n-type (N) and p-type (Al) 4H/6H-SiC within a large doping range at 300K are shown in Fig.3.8 Acoustic-phonon and ionized-impurity.

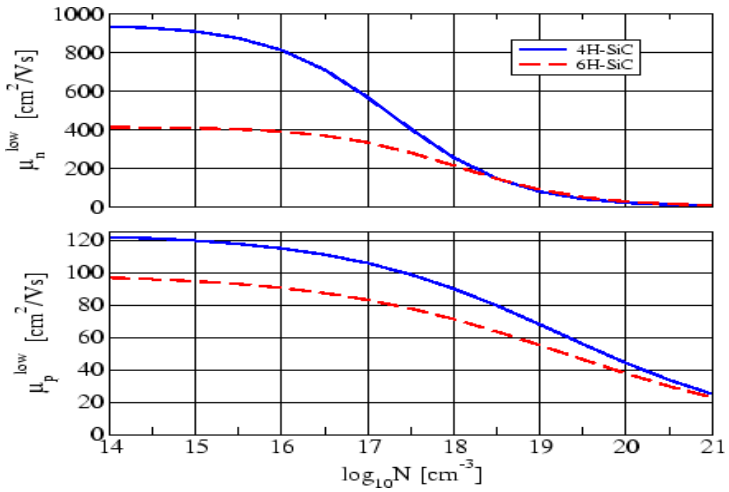


Figure 3.8: The n-type (N) and p-type (Al) mobility in α-SiC as a function of the doping concentration.

Acoustic-phonon and ionized-impurity scattering are not independent of each other.
Thus, Eq. (3.26) cannot be used and a combined model is needed. The data of Fig.3.8 can be modelled using the phenomenological model of Caughey-Thomas [116]:

$$\mu_v^{low} = \mu_{0v}^{min}\left(\frac{T}{300}\right)^{\alpha_v} + \frac{\mu_{0v}^{max}\left(\frac{T}{300}\right)^{\beta_v} - \mu_{0v}^{min}\left(\frac{T}{300}\right)^{\alpha_v}}{1+\left(\frac{N}{N_v^{crit}}\right)^{\delta_v}\left(\frac{T}{300}\right)^{\gamma_v}} \qquad v=n,p \qquad (3.28)$$

The parameters μ_0^{max} represents the mobility of undoped or unitentially doped samples, where lattice scattering is the main scattering mechanism, while μ_0^{min} is the mobility in highly doped material, where ionized impurity scattering is dominant. N_v^{crit} is the doping concentration at which the mobility is halfway between μ_0^{max} and μ_0^{min}, N is the total doping concentration. α_v, β_v, δ_v and γ_v are fitting parameters. The corresponding parameters are listed in Tab. 3.3.

	μ_{0v}^{max}	μ_{0v}^{min}	N_v^{crit}	α_v	β_v	δ_v	γ_v
	cm^2/v. s	cm^2/v. s	cm^{-3}				
n	950	40	2.00x10^{17}	-0.5	-2.40	0.76	-0.76
p	125	15.9	1.76x10^{17}	-0.5	-2.15	0.34	-0.34

Table 3.3: Values of low field mobility parameters for 4H-SiC, at T=300K [116].

Although the mobility parameters depend on technology, this table can serve as a base for evaluating measured device characteristics.

3.6.2.2 High field mobility

The effect of strong electric fields causes the carrier velocity to be no longer proportional to the field, and thus no longer can be described by a field independent mobility. Field-dependant mobility model is derived to account for carrier heating and velocity saturation effects; and analytically expressed in terms of the drift velocity as a function of the electric field in the direction of current flow. The analytical expression used for this aim is analogue to that largely employed for Silicon [117]:

$$\mu_v = \frac{\mu_v^0}{\left[1+\left(\frac{\mu_v^0 . E}{V_{sat}}\right)^{\beta}\right]^{\frac{1}{\beta}}} \qquad \text{v= n, p} \qquad (3.29)$$

Where μ_v^0 is the low field carrier mobility, V_{sat} is the saturation velocity, E the electric field, and β is a fitting parameter.

For 4H-SiC Khan et al [118] reported the values β=1.2 and V_{sat} =2.2x10^{7}cm.s^{-1}.The temperature dependence of V_{sat} and β can be modelled by

$$V_{sat} = V_{sat}^0 \left(\frac{T}{T_0}\right)^{\delta_{sat}} \qquad (3.30\ a)$$

$$\beta(T) = \beta_0 \left(\frac{T}{T_0}\right)^{\alpha_{sat}} \qquad (3.30\ b)$$

With δ_{sat}=-0.44 and α_{sat} =1 for 4H-SiC [119]. Fig3.9 shows the electron drift velocity versus the electric field for T=300K and T=293K. All measured refer to a current flow perpendicular to the c-axis (usual growth axis of epilayer).

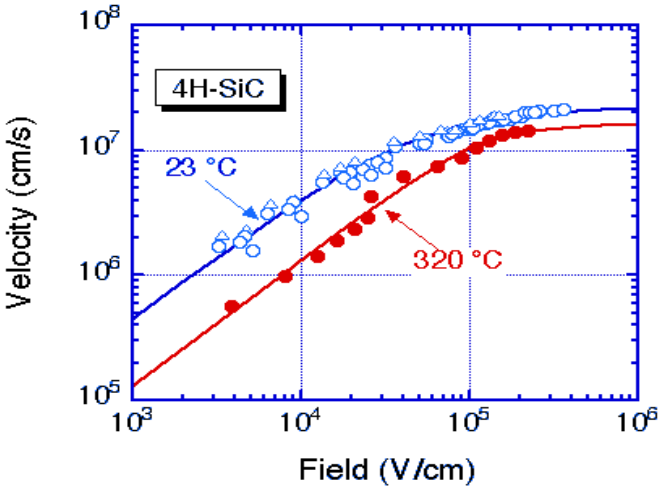


Figure 3.9: Electron drift velocity as a function of electric field in 4H-SiC at T= 300K and T=593K.

3.7 Dielectric constant

Using data available on the refractive indices, their dispersion, and on phonon energies obtained by Raman scattering, Patrick et al. published 1970 the two tensor components of the static dielectric constant of 6H-SiC [120]. They found a ratio of anisotropy $\varepsilon_{\perp}/\varepsilon_{//} = 0.96$ with $\varepsilon_{\perp} = 9.66$ and $\varepsilon_{//} = 10.03$. In a more recent investigation, Ninomiya et al. obtained $\varepsilon_{\perp} = 9.66$ and $\varepsilon_{//} = 9.98$ [121].Thus these values are well agreed upon within a very small error boundary. However, up to now, no values seem to be available for 4H-SiC. Therefore, the values of 6H-SiC have to be used. Since 4H-SiC has a somewhat larger bandgap than 6H-SiC, one may expect the dielectric constants of this polytype to be somewhat smaller [95]. Additionally, the ratio of anisotropy may differ, as the anisotropy of 4H-SiC seems to be generally weaker.

3.8 Critical field

For power-device applications, perhaps the most notable and most frequently quoted property is the breakdown electric field strength, E_{max}. This property determines how high the largest field in the material may be before material breakdown occurs. This type of breakdown is obviously referred to as catastrophic breakdown. Curiously, the absolute value of E_{max} for SiC is frequently quoted as the relative strength of the E_{max} against that of Si. Most discussions on this subject note that E_{max} of SiC is 10 times that of Si. As with Si, there exists a dependence of E_{max} with doping concentration. Thus, for a doping of approximately 10^{16} cm^{-3}, E_{max} is 2.49 MV/cm, according to a study by Kostantinov et al. [122]. For Si, the value of Emax is about 0.401 MV/cm for the same doping [123].

As can be seen, the value for SiC is only about a factor of six higher than that of Si and not the often-claimed 10 times higher critical field strength. Why the discrepancy? It is more correct to compare the critical strengths between devices made for the same blocking voltage. Thus, a Si device constructed for a blocking voltage of 1 kV would have a critical field strength of about 0.2 MV/cm, which should be compared with the 2.49 MV/cm of SiC.

3.9 Thermal conductivity

Another most important parameter for SiC material is the thermal conductivity. An increase in temperature generally leads to a change in the physical properties of the device, which normally affects the device in a negative way. Most important is the carrier mobility, which decreases with increasing temperature. Heat generated through various resistive losses during operation must thus be conducted away from the device and into the package. It is often quoted that the thermal conductivity of SiC is higher than that of copper at room temperature. There are even claims that it is better than any metal at room temperature [123]. The thermal conductivity of copper is 4.0 W/ (cm-K) [124]. That of silver is 4.18 W/ (cm-K) [125]. Values of the thermal conductivity as high as 5W/ (cm-K) have been measured by Slack [126] on highly perfect Lely platelets. More detailed studies have been made where the thermal conductivity in the different crystal directions have been determined for SiC (see Table 3.4 [127]).

Sample type	*direction*	*carrier concentration* (cm^{-3})	*Thermal conductivity* *W/cm K*	
			298K	378K
4H n	// c	2.0E18	3.3	2.5
4H n	⊥c	5.0E15	4.8	2.9
6H n	// c	1.5 E18	3.0	2.3
6H n	// c	3.5 E17	3.2	2.3
6H n	⊥c	3.5 E17	3.8	2.8
6H p	⊥c	1.4 E16	4.0	3.2

Table 3.4: The Thermal Conductivity of SiC.

Chapter 4

Results and Discussion

4.1 Introduction

In this chapter, simulations and measurements of SiC PiNs diodes are compared. A detailed investigation of the three main aspects, i.e., lifetime (τ), activation energies (E_a) and specific resistance (R_{on}) is presented. In addition, a brief overview of building factor is shown. Finally, an investigation of on the effect of some defect on the performance of a BMFET transistor is presented.

4.2 Device structure

The schematic cross-sections (plot not in scale) of the investigated Al implanted p-i-n diodes and the calculated net doping profile along the vertical axis of symmetry of a device realized using a 5 μm-thick and 3×10^{15} cm^{-3}-doped epilayer, are shown in figure 4.1.

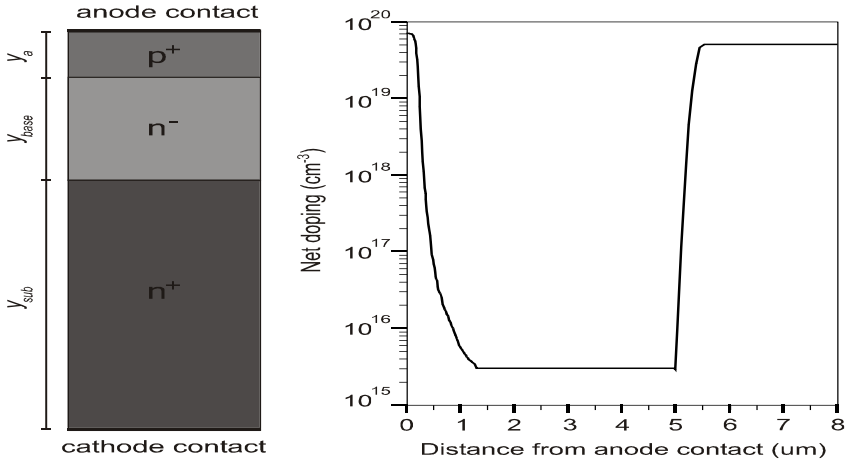


Figure 4.1: 4H-SiC p-i-n diode schematic cross-section and net doping profile of a device with a 3×10^{15} cm^{-3}-doped epilayer.

The diodes were provided by the CNR Institute for Microelectronics and Microsystems – Unit of Bologna (Italy). Details about the adopted technology were provided in [128] and references therein.

In short, starting from a commercially available <0001> 8° off-axis 4H-SiC n-type homoepitaxial wafer of elevated crystal quality [129], the diode structure consists of a n^+ substrate with a doping concentration in the order of 10^{19} cm^{-3}, a 3×10^{15} cm^{-3} n^- epilayer and a p^+ anode region obtained by Aluminium implant. As shown for the

Chapter 4: Results and Discussion

device in figure 4.1 the anode region exhibits a smooth half-Gaussian shaped profile with a peak doping of 6×10^{19}

cm^{-3} at the surface and a profile edge located at about 0.2 μm. The device ohmic contacts are made of a deposited Ni film on the back, while Ti/Al dots were deposited on the anode surface. As listed in table 4.1 almost similar diodes (structure #2) realized using a wafer with an epilayer thickness of 16.5μm have also been analysed. For all the samples the calculated active area is in the range $0.75\text{-}1\times10^{-3}$ cm^2.

Details about the implantation process and the post–implantation annealing are again reported in [128]. There, in particular, mainly depending on different thermal treatments of the samples, two different contact resistances in the order of 1.25×10^{-3} Ω·cm^2 and 2×10^{-5} Ω·cm^2 were measured at room temperature for the structures labelled #1 and #2 in table 4.1, respectively.

	Structure #1 (D1)	*Structure #2* (D2)
Anode thickness, Y_a (μm)	0.2	0.5
Anode doping (cm^{-3})	6×10^{19}	1×10^{20}
Base thickness, Y_{base} (μm)	4.8	16
Base doping (cm^{-3})	3×10^{15}	3×10^{15}
Cathode thickness, Y_{sub} (μm)	300	350
Cathode doping (cm^{-3})	5×10^{19}	1×10^{19}

Table 4.1: Geometrical and doping parameters of different 4H-SiC p-i-n diodes

4.3 Equipment and Procedures

A Micromanipulator probe station and a HP4156B parameter analyzer were used to obtain the I-V characteristics of the diodes. The sample was loaded on the chuck of the micromanipulator. A vacuum pump was used to create suction to hold the sample tightly to the chuck, so that the Nickel ohmic contacts on the backside of the sample could make electrical contact through the chuck. The micromanipulator setup was enclosed in a vibration-isolation chamber fig4.2.

The I-V characteristics of these diodes were studied at forward. Typically, the forward bias on all diodes was ramped up to 4 Volts, with the current compliance set to 100mA. The Source and Measure Unit (SMU) of the HP4155 can limit the current to prevent damaging the device under test. This limit, specified as the Current-Compliance, has a maximum value of 100mA on the HP4156B parameter analyzer. The sampling interval was set to 16.67ms by choosing the medium integration-time setting on the analyzer.

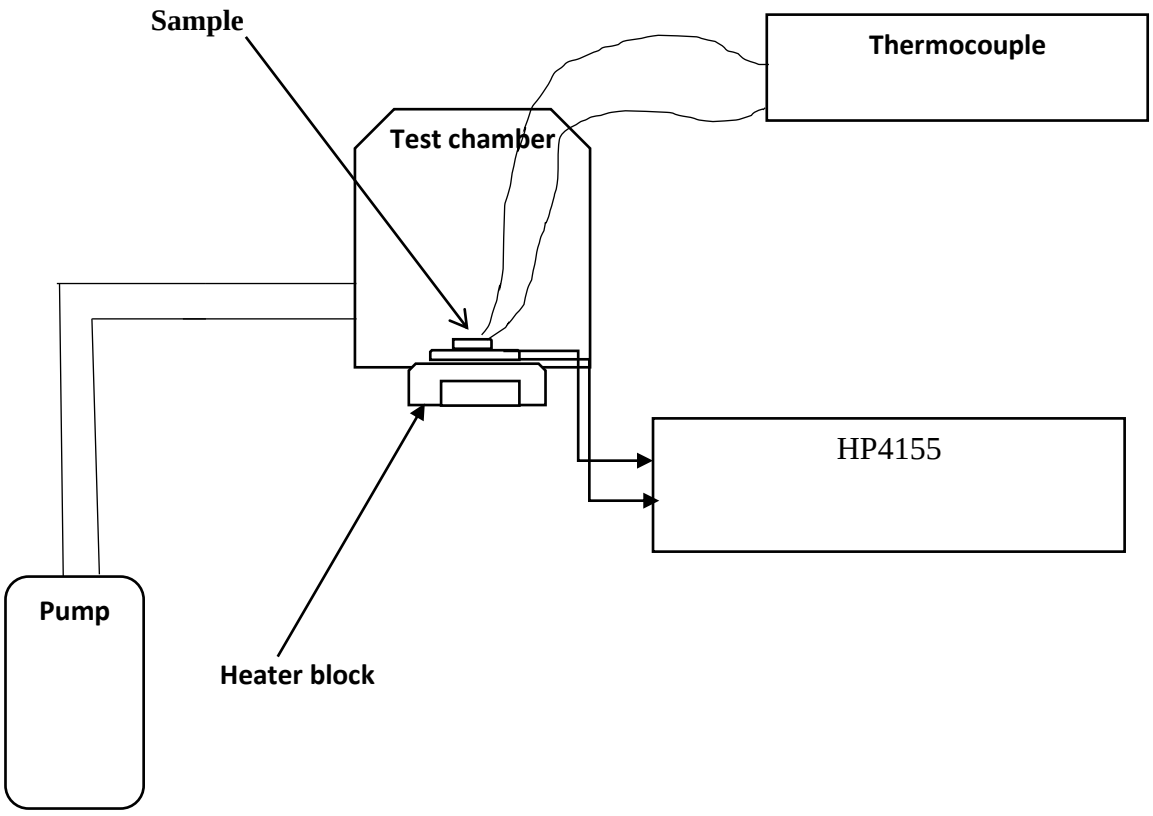


Figure 4.2: Experimental Set-up used for I-V-T measurements.

4.4. Results and Analysis

4.4.1 Introduction

The key to understanding a specific diode's shortcomings is to understand the current conduction mechanisms. In p-n diodes, several current transport mechanisms may occur at the same time. The ideal diode's dark current conduction, described by Shockley, is due only to diffusion [130]. This is generally not observed in experiment. No semiconductor is perfectly pure. As a result of impurities and lattice defects, energy levels will exist between the valence and conduction bands. These levels allow various other current conduction mechanisms to occur. It follows that fewer impurities and lattice defects give an I-V curve that more closely approximates Shockley's ideal case.

Current conduction in Si due to two exponential terms was first reported by Wolf, and later referenced by Reinhardt [131]. Wolf identified the two exponential terms as diffusion and junction space-charge recombination of the Shockley-Read-Hall type (Sah et al., 1957:1228) [132]. It was later found that the inclusion of shunt and series resistance terms, R_{sh} and R_s, respectively, produced a current-conduction model, which more closely matched experimental results.
The current-conduction model is given by [132]

$$J_{tot} = J_{diff}\left[exp\left(\frac{q\,V_D}{n_1\,k.T}\right) - 1\right] + J_{rec}\left[exp\left(\frac{q\,V_D}{n_2\,k.T}\right) - 1\right] + \frac{V_D}{R_{sh}} \qquad (4.1)$$

$$J_{rec} \sim \frac{qWn_i}{2\tau_{R-G}} \qquad (4.1\ a)$$

$$J_{diff} \sim \left(\sqrt{\frac{qkT\mu_n}{\tau_n}}\frac{{n_i}^2}{N_A^-} + \sqrt{\frac{qkT\mu_p}{\tau_p}}\frac{{n_i}^2}{N_D^+}\right) \qquad (4.1\ b)$$

Where J_{total} is the total current density, J_{dif} is the saturation current density for diffusion, and J_{rec} is the saturation current density for space-charge recombination. n_1 and n_2 are ideality factors. For the case of ideal diffusion, $n_1 = 1$. The value of n_2 is dependent on the location of recombination centers within the bandgap. If these recombination centers are located near the center of the bandgap, n_2 will have an approximate value of 2. The third term accounts for current due to shunting.

When shunting is due to carrier tunneling and capture-emission, then the shunting resistance term can be better modeled by [133]

$J_{sh} = J_0 \exp(B V)$ (4.2)

Where J_0 is the reverse-saturation current density due to tunneling and B is a fitting parameter. The diode junction voltage, V_D, is related to the applied voltage, V, the total current, and the series resistance by

$V_D = V - I_{total}R_s$ (4.3)

Tunneling current is due to carriers tunneling through the junction to the other side. The different possible tunneling paths are horizontal transitions are due to tunneling, while vertical transitions are due to capture and emission processes. A majority carrier can tunnel all the way through the junction. It can tunnel via states within the forbidden gap, or some combination of capture, emission, and tunneling can occur (Sze, 1981:528). The tunneling current density, as reported by Sze, is given by [134]

$$J_t = \sqrt{\frac{2m^*}{E_g}}\,\frac{q^3\varepsilon_s V}{h^3}\exp\left(\frac{-8\pi\sqrt{2m^*}}{3q\varepsilon_s h}E_g^{\frac{3}{2}}\right) \quad (4.4)$$

Where m* is the effective mass, and ε_s is the permittivity of SiC.

4.4.2 Forward I-V 4H-SiC PiN diodes Measurements

In Figure 4.3, the I-V characteristics for a well-behaved diode D1A, D1B, and leaky diode D1C are compared. Under forward bias, the well-behaved diodes are characterized by a sharp turn-on at a relatively high "threshold" voltage, and the current is dominated by carrier diffusion in a region (III) and recombination in a region (II). The diffusion and recombination current mechanisms produce a quick rise in slope, which is a characteristic of high quality, low resistance, and efficient operation. Conversely, the leaky diode conducts considerable current at much lower voltages in regions (I) and (II), which is characteristic of conduction through tunneling like leakage paths. Further, leakage currents showed exhibit a smaller slope after turn-on, which is also a characteristic of tunneling [136].

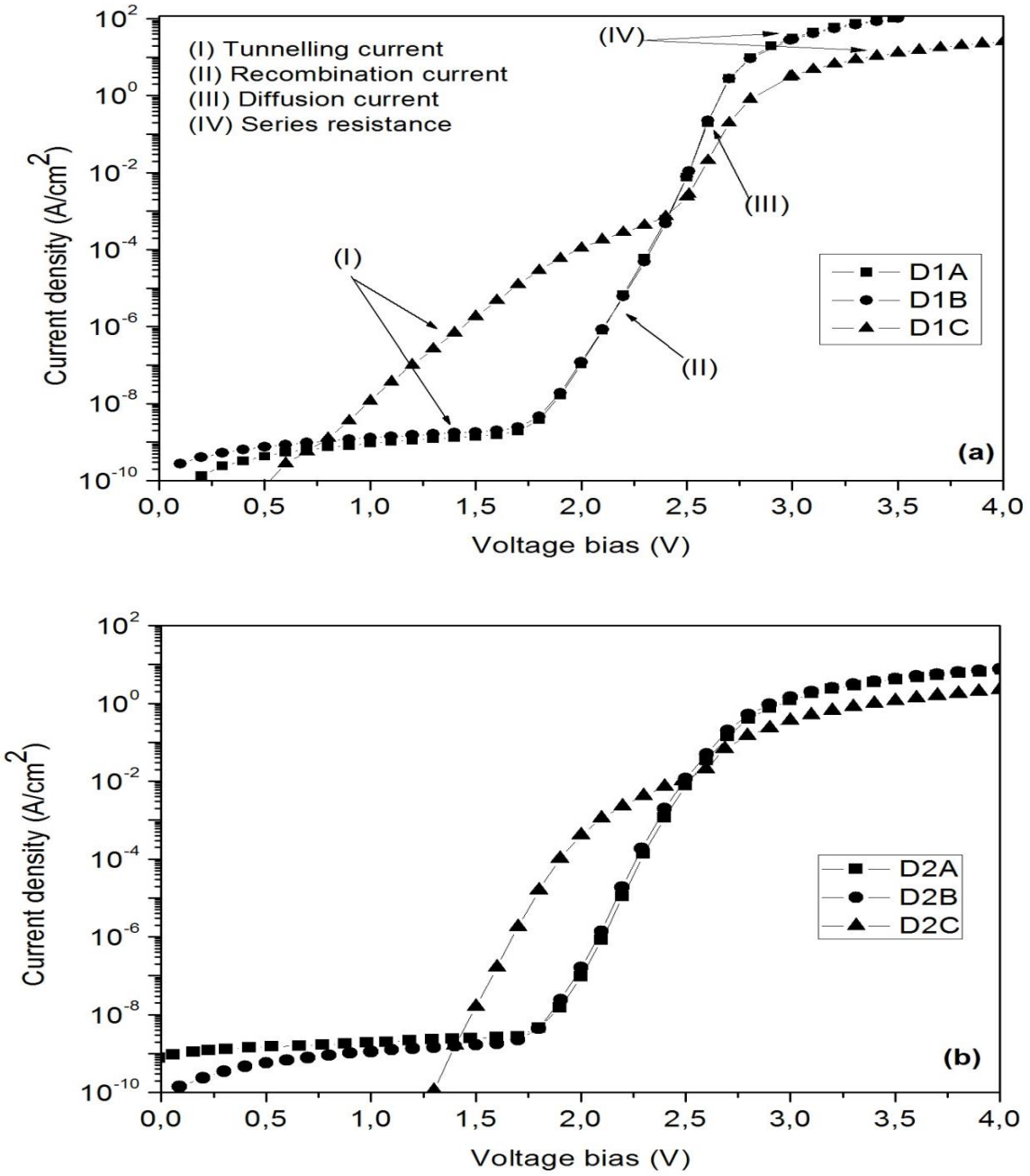


Figure 4.3: Forward *J-V* characteristics of several 4H-SiC p-i-n diodes (structure #1 (a), structure #2 (b)) measured at 298K.

Figure 4.3 also shows the effect of series resistance, Rs, at voltages greater than ~2.75 V as shown in region (IV). In this region, the forward voltage drop due to IRs becomes comparable to the applied voltage. Diode D1A and D1B in Figure 4.3 exhibits current due to tunneling, recombination, and diffusion, while diode D1C only exhibits current due to tunneling and recombination. In agreement with the theory, the tunneling currents shown by (II) in Figure 4.3 dominate at low voltages, while the recombination current (I) and diffusion current (III) dominate at mid-range and high voltages, respectively.

In the case of diode D1A and D1B, Eq. (4.1) describes the tunneling current well over the voltage range of 0-1.75 V. In the range of 1.75-2.85 V, values of the ideality factor n_2 obtained for two diodes ranged between 1.85 and 2.10. As noted earlier, a value of n_2~2 is characteristic of ideal recombination through traps at the center of the bandgap. An analogue analysis on the current transport mechanisms at different biases can be made for the samples D2 in figure 4.3(b). The well behaved diodes D1A and D2A were selected in order to fit with simulation results.

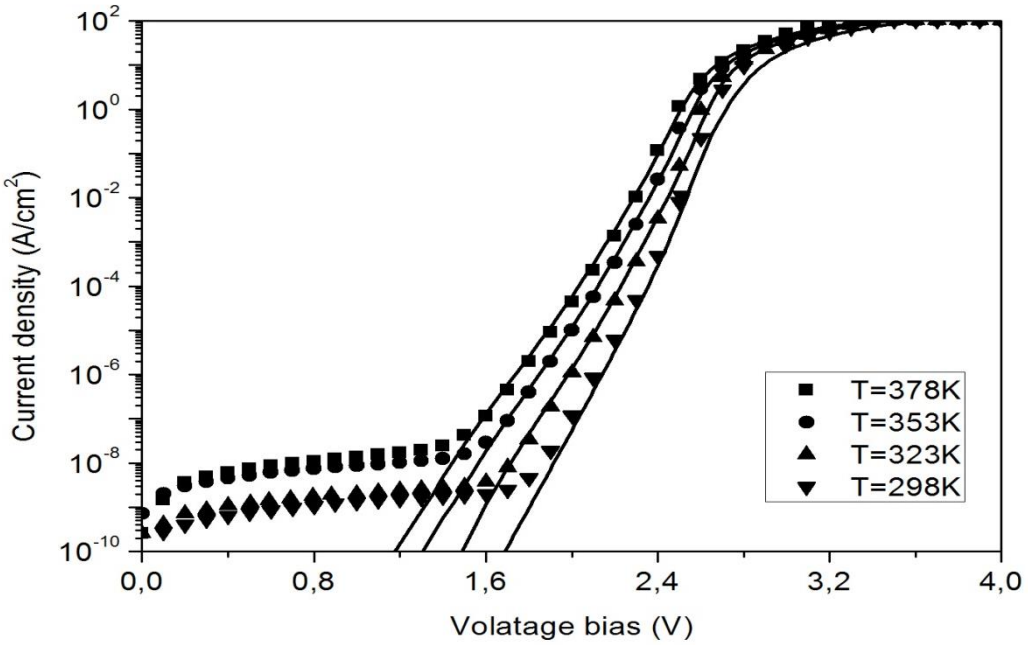


Figure 4.4: Simulated (solid lines) and experimental (dotted lines) forward characteristics of the diode D1A at different temperatures.

Interesting diode behaviours were obtained performing a high temperature analysis for both the D1 and D2 samples. Forward-bias I-V characteristics measured as a function of temperature (I-V-T) for diodes D1A and D2A are shown in Figures 4.3 and 4.11, respectively.

As shown in Figure 4.3, the voltage at which diode D1A turns on decreases with increasing temperature from ~1.71 V at 298 K to ~1.43 V at 378 K [136]. Before the device turns on, the I-V curve is dominated by tunneling current. As predicted by Eq. (4.4), the magnitude of tunneling current is weakly dependent on temperature. After the device turns on, the forward current increases at a fixed voltage with increasing temperature. Figure 4.3 and 4.4 shows that as the temperature increases the series resistance becomes a significant factor at lower voltages.

Considering the complete measured temperature range, it becomes obvious that there are significant differences between simulated and measured data at lower temperatures (Fig. 4.3 and fig.4.4). The activation energy, E_A, for the n =2 recombination current for well-behaved SiC PiN diodes was calculated using Eq. (4.4)

$$J_{rec} \sim T^{\frac{5}{2}} \exp\left(-\frac{E_A}{KT}\right) \qquad (4.4)$$

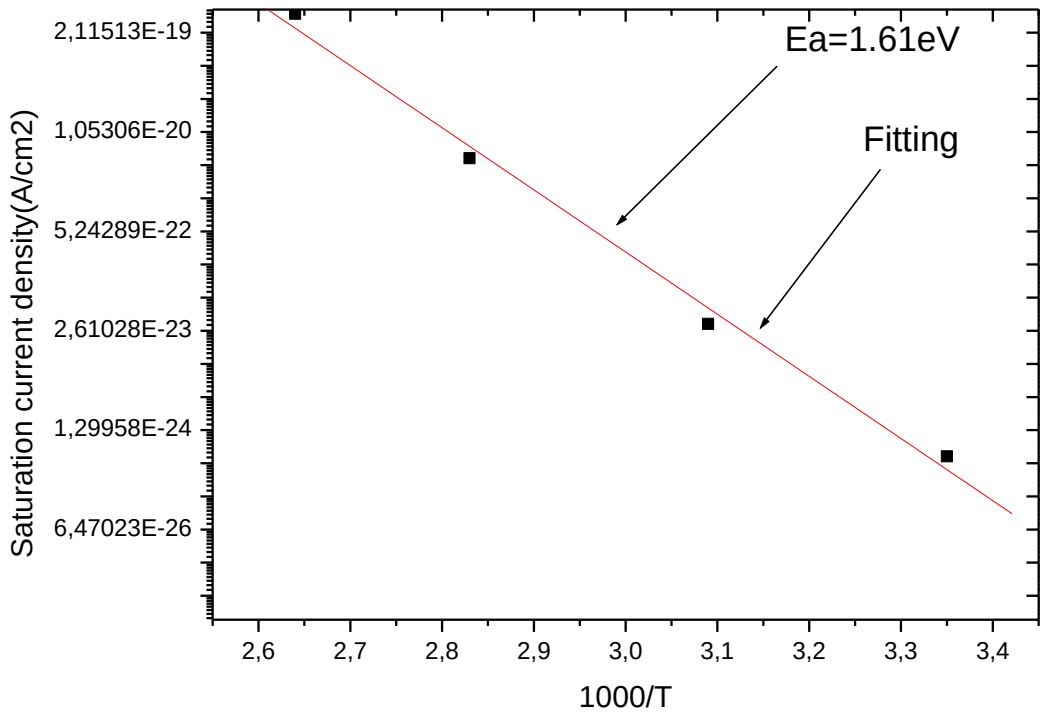


Figure 4.5: Plot of well-behaved recombination currents vs.1000/T. The average activation energy E_A = 1.61 eV has been obtained using Eq (4.4).

Using an Arrhenius plot, a best-fit line was drawn through the Ln (I_{rec}) vs. 1000/T data for the well-behaved diodes to yield a value for E_A as shown in Fig 4.5. The average value of E_A obtained was 1.61 eV, compared to a value of E_A=Eg/2 =1.63 eV for ideal recombination current in 4H-SiC with Eg= 3.26 eV [136].

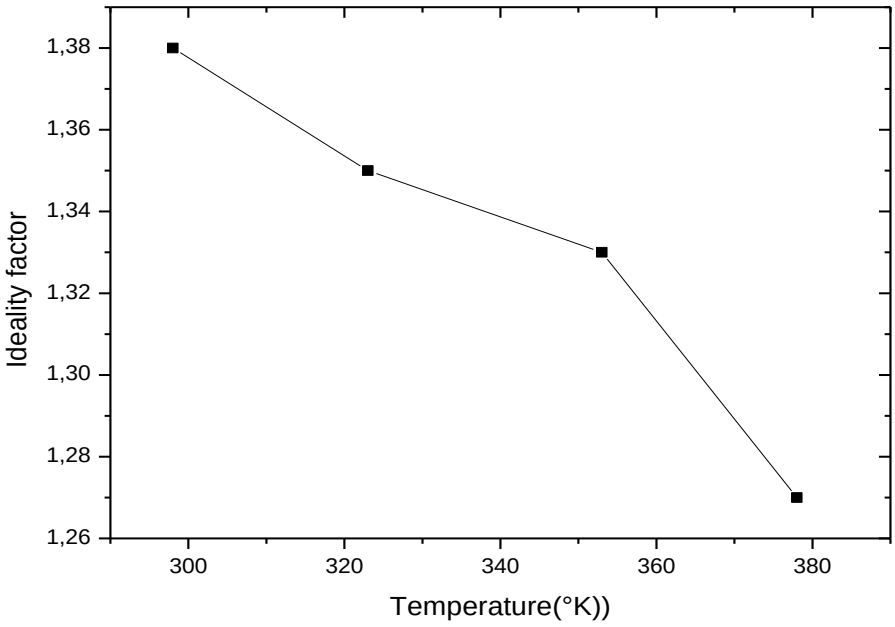


Figure 4.6: Temperature dependence the measured ideality factor of the diode D1A between 2.5V and 2.8V.

For an ideal PiN diode the carrier transport over the barrier is governed by thermionic emission. The current density, J, is given by equation 4.1. In order to analyze the electrical characteristics, the ideality factor, n is extracted using eq.4.5 [137].

$$n = \frac{1}{K_B T} \frac{1}{\frac{d(\ln(I))}{dV}} \qquad (4.5)$$

Fig.4.6 shows, for higher voltages the curve shows a smaller ideality factor in the order of $1.0 \leq n \leq 2.0$ before the high-injection regime is reached. The deviation from the theoretically predicted ideality factor of n = 1.0 can be explained by a generalized form of the Schottky-Noice-Sah theory [134] for the current transport through a junction. In this theory, the current transport is explained by means of carrier recombination through multiple deep and shallow levels in the band gap.

The theory predicts an ideality factor of

$$n = \frac{s+2d}{d+s} \qquad (4.6)$$

Where *s* is the number of discrete shallow levels and *d* is the number of discrete deep levels in the band gap, participating in the recombination process. According to this theory, the observed ideality factor of n ~ 1.33 = 4/3 (fig 4.6) would thus be caused by the participation of d =1 deep and s = 2 shallow levels in the bandgap [138].

In the series resistance region, where only a limited current increase is observed in figure 4.3 for voltage biases higher than 3V, a good agreement between the simulated and experimental data was achieved simply considering a temperature dependence of the contact resistance R_c in the order of -5μΩ·cm^2·K^{-1}. A negative temperature coefficient of R_c for the investigated 4H-SiC p-i-n diodes was also experimentally observed in [128], pointing out a mixing of thermionic and field-effect conductions through the contact-semiconductor interface.

In the series resistance region, however, the structure #2 exhibits a different J-*V*-*T* behaviour, as shown in figure 4.11 for the diode D2A. In fact, although there are weak differences between the two diode structures in the current contributions due to the carrier recombination and considering R_s in the form $R_s=2R_c+R_i$, whereas for the structure #1 we can assume $2R_c > R_i$, it is evident that for the diode D2A the R_i effect overcomes the R_c contributions at all temperatures limiting more and more the diode current capability as the carrier mobilities decrease increasing the temperature. In particular, $R_i \propto 1/qN\mu_n$ in fact, as a consequence of a higher dopant activated in the n$^+$ region that tends to suppress the hole injection in the substrate, above the *J*-*V* curve knee the total diode current is dominated from the electron injection into the anode. As a proof, the incomplete ionization model predicts a ~10 times lower saturation level of the ionized acceptor concentration.

4.4.3 Simulation of 4H-SiC devices

The simulation study of the 4H-SiC devices is based on the Atlas-Silvaco solid-state device simulator. The 4H-SiC physical parameters are set as in chapter 3, where a numerical analysis was focused on Al implanted 4H-SiC p +-i-n diodes and supported by experimental measures in a wide range of temperatures. In particular, a coincident carrier lifetime reference value for the implanted regions as low as 10 ns is assumed at room temperature (RT) [136].

Specific 4H-SiC physical models, including the SRH and Auger recombination processes incorporated with a concentration dependent carrier lifetime, the carrier mobility as function of doping, free carrier density and temperature, were taken into account during simulations both inside the epitaxial layer and implanted regions.

4.4.3.1 Statistical limit

By defining N_{min} = 100 carriers within the active volume V = A_{D1A}.4.8.1×10^{-4} cm^3 as the statistical limit for sample D1A, the density of free carriers determining the contact current at different operation conditions must be larger than n_{min} = N_{min} /V = 2.7.10^5 cm^{-3}. Using the analytical relation for the recombination current, Eq. (4.1), to estimate the minimum voltage needed for exceeding n_{min},

$$U > U_{min} = \frac{2kT}{q} ln\left(\frac{n_{min}}{n_{i,eff}}\right) \quad (4.7)$$

We obtain U*min* ≈ 1.5 V at room temperature. This leads to J_{min} ≈$10^{-9}$$Acm^{-2}$ (Fig. 4.3) which yield a minimum contact current of I*min* = J_{min}.AD1 ≈ 7.5.10^{-13}A which is very close to the limits of the measurement setup. In Fig. 4.3, the internal distribution of the free carrier densities of the forward biased sample D1A (Fig. 4.7) at different operation points is plotted. At U = 1.5V, the current is clearly dominated by recombination within the depletion region which mainly occurs within a narrow region of about 200nm (Fig. 4.8). At this point, the free carrier densities determining the current are in the order of n_{min} confirming the estimation of Eq. (4.7). U*min* increases with decreasing temperature because of the corresponding decrease of $n_{i;eff}$. At a temperature as low as 150K, we obtain U*min* ≈ 2.3V which again yields J*min* ≈$10^{-10}$$Acm^2$. This is corroborated with the decrease of Ubi with increasing temperature, thus yielding a minimum current density J*min* approximately independent of temperature.

4.3.3.2 Simulation of 4H-SiC pin diodes

In this section, Diodes D1A and D2A structures are introduced and compared to simulated results. First, some analytical models are presented, and then some hybrid models are described. With the exception of the model presented, where lifetime is variable in the epilayer , the mobilities are dependent of carrier concentration and temperature, the other compact models analysed in literature have the following assumptions:

• The problem is treated as two-dimensional in the space;
• The temperature T is variable;
• The P^+N^- and N^-N^+ are Gaussian;
• The doping in the base region is constant ;
• The lifetime τ_{hl} and the mobilities in the base are constant and independ of injection;
• The carriers density in the epilayer is much larger than the doping density (high injection).

The well behaved diodes D1A and D2A were selected in order to fit with simulation results. The parts of the forward current characteristics due to recombination and diffusion phenomena are well suited as reference for the calibration of the carrier lifetime parameters.

In fig 4.9 it is seen that up to 1.5V the device does not reach the high injection regime in the n- region and therefore in fact it behaves as a p+n- long diode. By comparison with fig 4.3, it also clear the change of the slope of J-V curve takes place around V_d = 2.9V marks the beginning of significant electrons and holes injection into the p+ and n- layers, respectively.

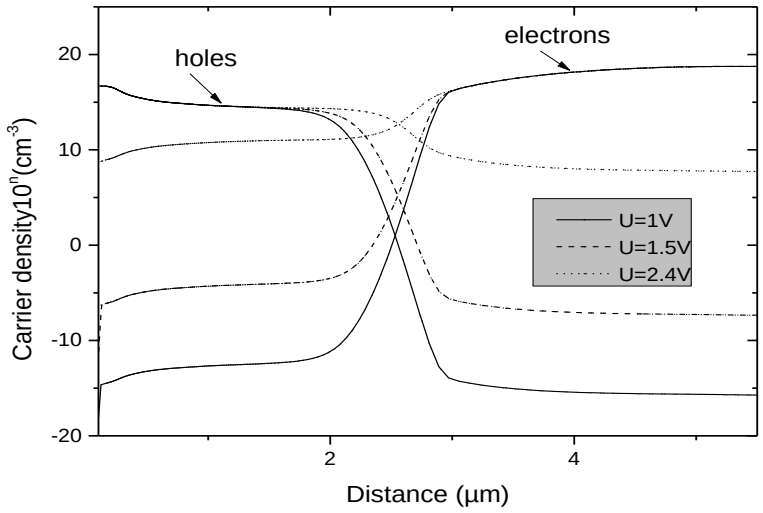


Figure 4.7: Electron and hole density distribution of forward of PiN diode at U_d=1V, 1.5Vand 2.4V

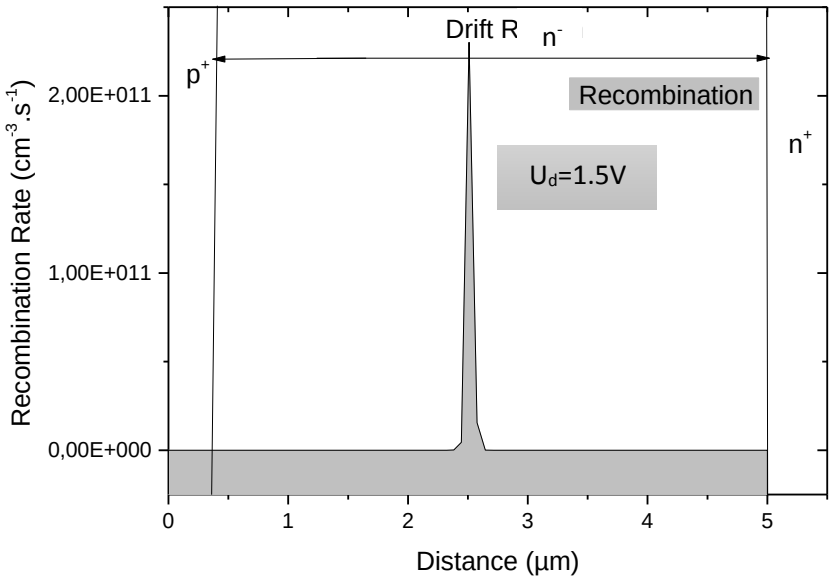


Figure 4.8: Localization of recombination rate at U_d = 1.5V.

On the other hand, the calculation of the carrier recombination depth profile shown in fig 4.8 reveals that, at biases of 1.5V, the recombination current, which is the dominant component of the current density, is largely concentrated inside a narrow region in the depletion layer.

In order to better highlight the temperature dependence of the carrier mobility and to properly fit the measured forward characteristics of the device D2A at highest current regimes, a simplified version of (3.28) in the form $\mu_{n,p}=\mu_{0n,p}(T/300)^{\alpha}$ was also considered during the simulations. Assuming μ_{0p}=6 cm^2/V·s at T=300K as measured in, the best fit gives μ_{0n}=30cm^2/V·s and α=-5.25. Such carrier mobilities should be considered as average values along the diode structure and predict a diode internal resistance in the order of 10 mΩ·cm^2. This result explains the limited maximum current handling of the samples D2 if compared to D1.Considering Fig. 4.3, there are two different recombination mechanisms, which may determine the recombination current of sample D1A: First bulk recombination within the depletion region along the junction and second surface related recombination as modeled by Eq. (3.16). While the surface recombination velocities v_v do not influence the diffusion dominated part of the characteristics, the bulk recombination current is coupled to the diffusion current by the minority carrier lifetimes τ_v and to a minor extend by the free carrier mobilities as long as the diffusion lengths are smaller than the layer thickness of the diffusion regions [134]. The well behaved diodes D1A and D2A were selected in order to fit with simulation results. The parts of the forward current characteristics due to recombination and diffusion phenomena are well suited as reference for the calibration of the carrier lifetime parameters.

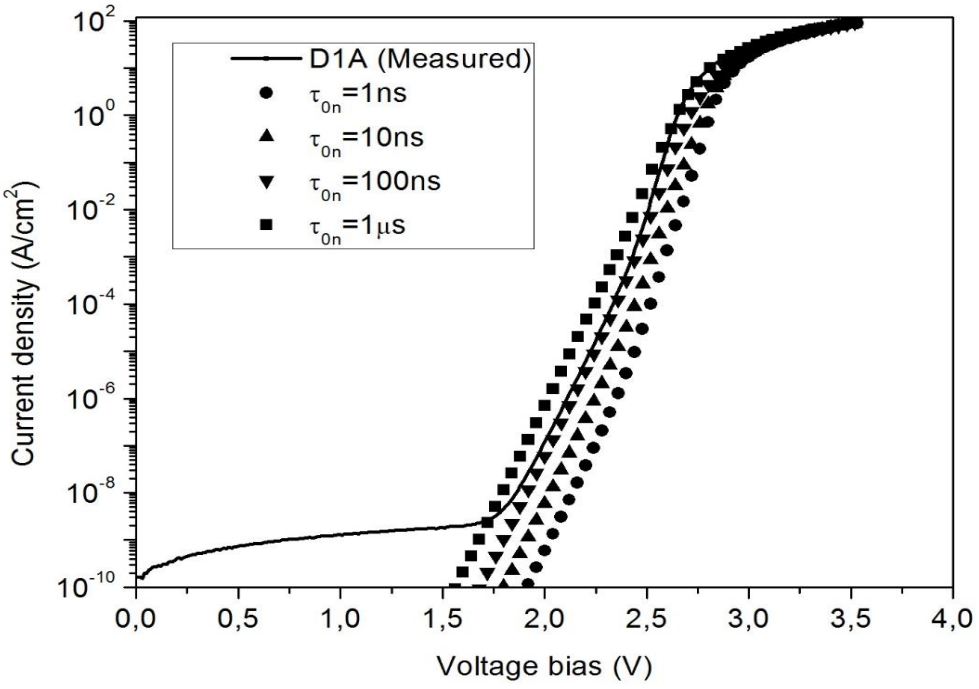


Figure 4.9: Measured and simulated forward characteristics of sample D1A at 298K including lifetime.

In Fig.4.9, the default parameters, as outlined in eq. (3.15), have been used and the minority carrier lifetime parameters τ_{0n} and λ of the Scharfetter relation have been adjusted such that the simulated recombination current at 298K agrees with the measured data. A fitting parameter τ_{0n}=10 ns is in accordance with the experimental results measured by reverse recovery at T=300K on similar p-i-n diodes have been reported [137]. For the sample D2A, τ_{0n} results ~3 times lower probably due to the presence of deep-level defects as efficient carrier traps, which can seriously affect the performance of the semiconductor devices in the diode active area [138]. The most important two intrinsic point defects suspects to play a role in recombination lifetimes are the Z1/2 and EH6/7 [139].The concentrations of these two centers are both inversely correlated with the minority carrier lifetime, and for a while it was uncertain which defect center was the actual culprit in limiting the lifetime.

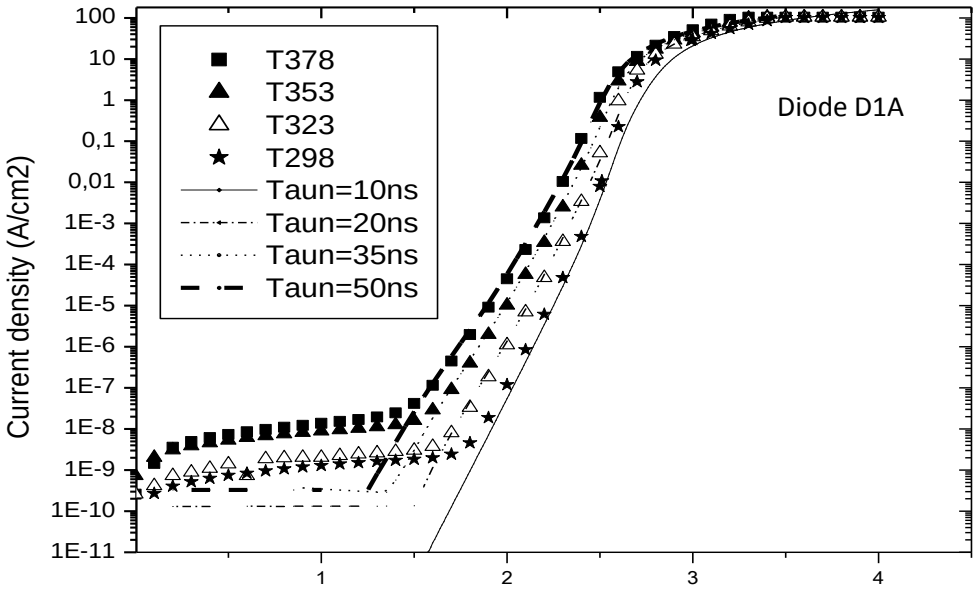


Figure 4.10: Measured and simulated forward characteristics of sample D1A at several temperature including corresponding lifetime.

Interesting diode behaviours were obtained performing an high temperature analysis both for the D1 and D2 samples. The measured and simulated *J-V* characteristics of the diode D1A at various temperatures are shown in figure 4.10 in semi-log scale. As the testing temperature increases, the carrier lifetime increases. When the testing temperature is at 378K, the carrier lifetime values increases up to 30ns in the base region. Although an overall qualitative agreement is observed, deviations are observed at higher temperatures within the recombination and diffusion part of the characteristics, respectively.

Similar disagreement between measured and simulated data below a certain threshold voltage depending on temperature has been observed by other groups [140, 141].

Assuming a power law for the temperature dependence of the SRH lifetimes, Eq. (3.15), with τ_{0n}=10 ns and λ=1.82, the simulated characteristics agree excellently with the measured data within the complete temperature range (Fig. 4.10) for both the recombination-dominated and diffusion-dominated part of the IV characteristics.

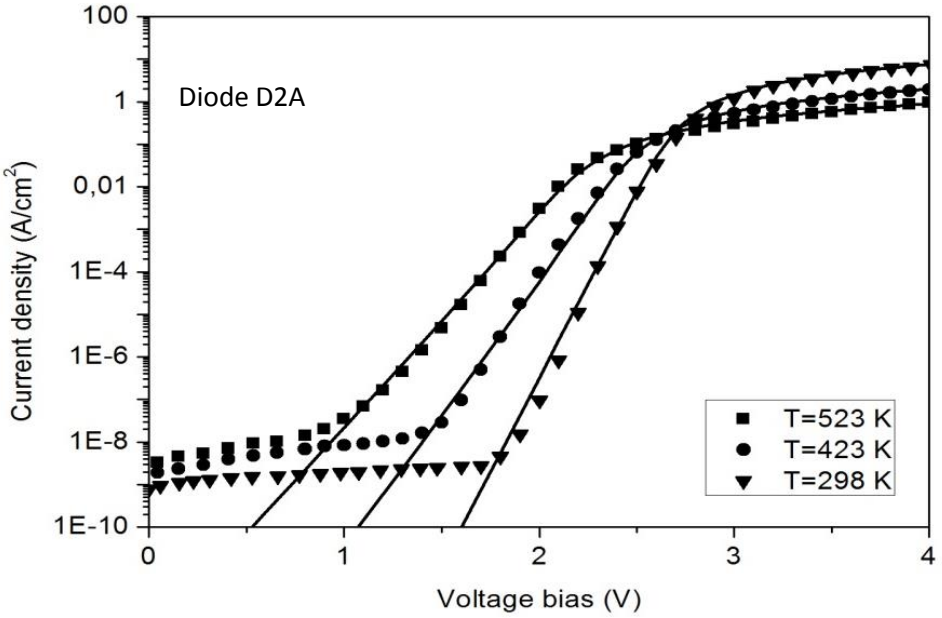


Figure 4.11: Simulated (solid lines) and experimental (dotted lines) forward characteristics of the diode D2A at different temperatures.

A similar finding is obtained in case of sample D2. In Fig. 4.11, the simulated IV characteristics with τ_{0n} = 3.65ns and λ = 1.6 are shown which again agree with the measured data within the recombination- and diffusion-dominated range. Other groups using the method described by Tien and Hu (reverse recovery measurement) [142]. There are several uncertainties among the material parameters, which may affect the quantities affecting the equation governing the IV characteristics. The diffusion current is underestimated due to larger bandgap and the corresponding lower intrinsic density, which may be partly compensated by a reduced concentration of ionized donors. Furthermore, the bandgap-narrowing parameters are only based on theoretical calculation [143].These most mentioned uncertainties would influence the simulated results compared to measured one.

4.5 Simulation of Trapping Effects in 4H-Silicon Carbide Bipolar Modulated Field Effect Transistor (4H-SiC BMFET)

In this section, the degradation of BMFETs due to the formation of crystal defects as a result of interactions with energetic particles or as growth is investigated. The crystal defects result in deep states in the SiC forbidden energy gap where carriers recombine, thereby affecting the electrical properties of the device. The impact of defects on the SiC BMFET performance is studied by introducing traps of various energies and densities on fully functional devices. Due to the different stopping mechanisms for ions in matter, it has been possible to introduce a certain amount of defects at a specific location in the device. By analysing the degradation of the electrical performance of the devices exposed to $Z_{1/2}$ $EH_{6/7}$ traps, with selected energies, density and cross-section, it is possible to identify different mechanisms involved in the degradation.

4.5.1 Device structure

The schematic cross-section of the considered BMFET elementary cell is shown in Fig. 4.12. The device parameters (p+-gate junction depth, epilayer thickness, and its doping, channel width, source, drain, and p+-gate peak doping) are chosen based on reported results in literature [145] are tabulated in Table 4.2.

By applying a forward gate-source voltage, we obtain an injection of minority carriers from the gate region into the epilayer that induces a conductivity modulation in the epilayer. Consequently, depending on the carriers injected by the gate, a large current can flow between source and drain. Otherwise, in the OFF-state of the device, the drain-source current is inhibited by FET mode of operation; in fact, without applying a gate-source voltage, the channel under the source region is kept in pinch-off by the gate junction built-in voltage.

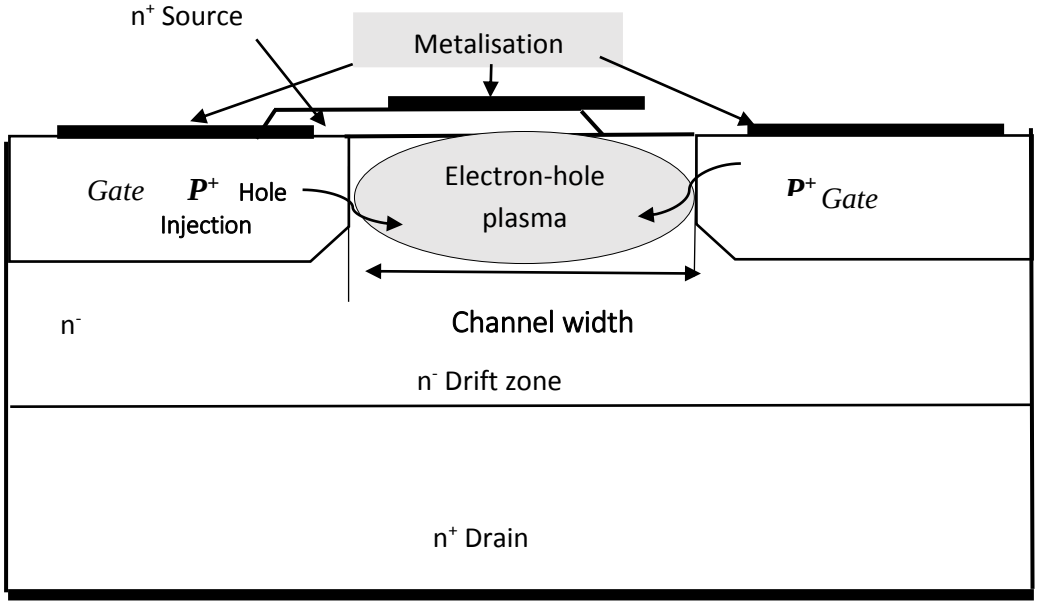


Figure 4.12: Schematic cross-sectional view of one-finger 4H-SiC BMFET transistor.

Epilayer thickness, (µm)	10
Gate junction depth, (µm)	2.7
Gate distance, W(µm)	1.5
Source depth, *Y*s (µm)	0.7
Device area (μm^2)	5.5
Epilayer doping, N_{epi} (cm^{-3})	10^{15}
Gate doping, N_A (cm^{-3})	$2x10^{19}$
Source doping, N_D(cm^{-3})	10^{19}
Substrate doping, N_{sub} (cm^{-3})	$5x10^{19}$

Table4.2 BMFET parameters

4.5.2 Simulation analysis

The 2-D numerical simulations were performed using SILVACO [90] TCAD to obtain the dc characteristics of BMFET.

The various models activated in the simulations are Fermi–Dirac distribution for carrier statistics, Caughey-Thomas mobility model for dopant and temperature dependent low-field mobility, analytical field-dependent mobility for high electric field, ionization-rate model for incomplete ionization, and Shockley–Read–Hall (SRH) and Auger recombination models for minority-carrier recombination lifetime and lindelfelt model for Band Gap narrowing supported by C interpreter (see appendix B).

The specification of meshes involves a trade-off between the requirement of accuracy and time in Silvaco. Accuracy requires a fine mesh that can resolve all significant features of the solution. Faster simulation requires a coarse mesh that minimizes the total number of grid points. This trade-off between accuracy and time is a source of problems for users.

Fig 4.13 shows a base mesh in 2D on diffusion with dense meshing; such a dense meshing will use up a lot of CPU memory and will takes a long time to simulate. The result generated will be very accurate.

When you increase the density of the mesh, it will definitively increase the simulation time. It is important that you only increase the density of the mesh in the critical area such on the pn junction. Subsequently is the to show of two different amount of mesh, one only denser in the critical area and the next was denser constantly throughout the area Fig.4.13.

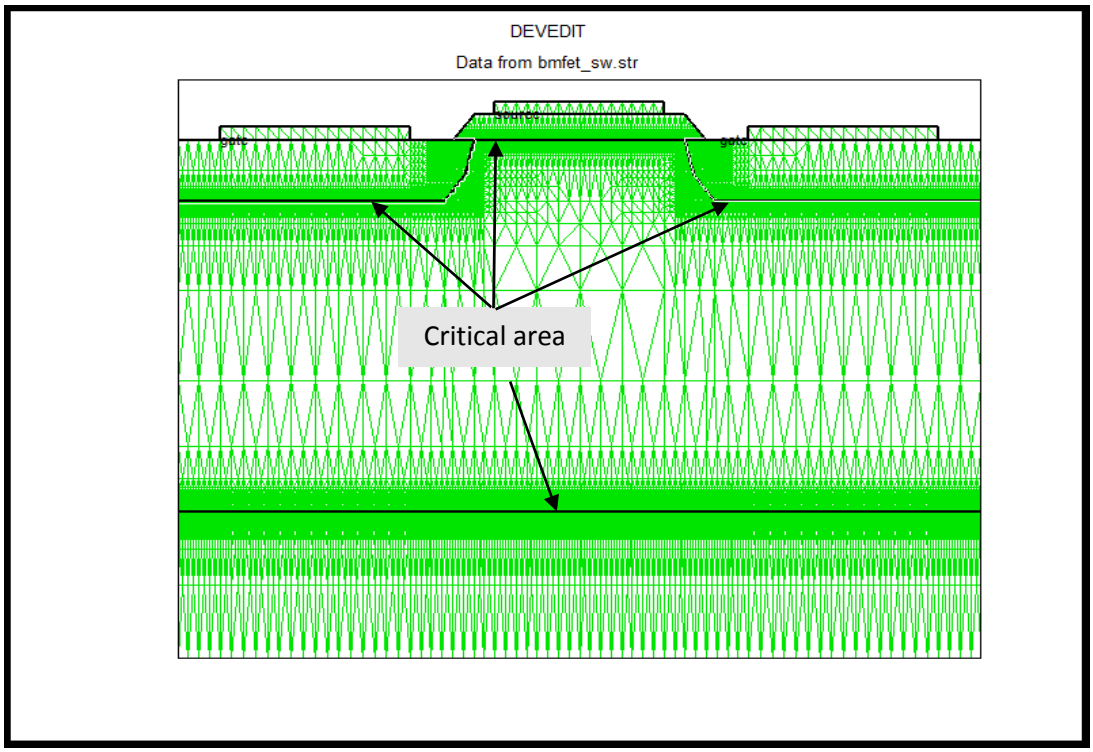


Figure 4.13: 2D an optimal meshing density of a 4H-SiC BMFET structure simulated using Silvaco atlas software.

The electron and hole concentrations in the n-drift region of the BMFET are shown in Fig.4.14. Fig.4.14 shows the thermal equilibrium hole and electron concentrations at zero-bias condition, i.e., at j_G = 0A and V_{DS} = 0 V. It can be seen that the concentration of electrons at this bias is about 10^{15} cm^{-3}, which is equal to the epilayer doping.

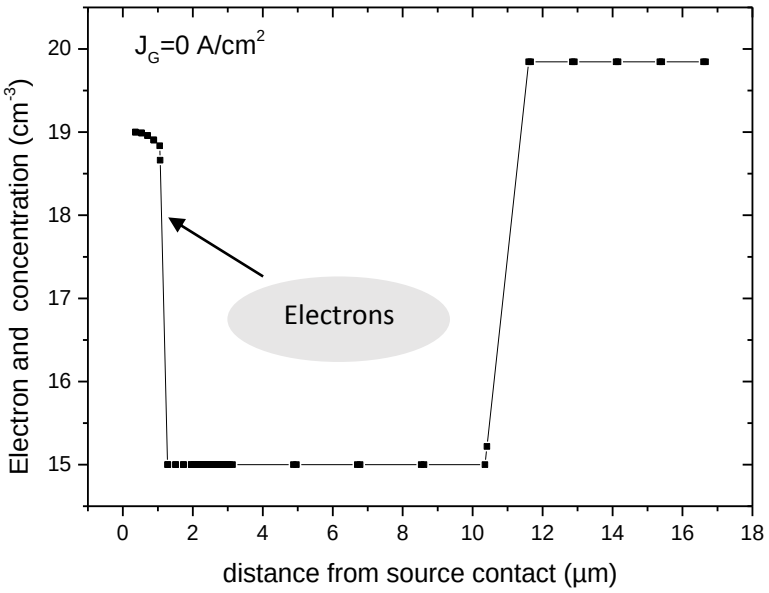


Figure 4 .14: Electron and hole concentration at J_G=0A (V_{DS}=0V).

Fig. 4.15 shows the concentration of holes and electrons in the channel for different values of J_G and V_{DS} = 0 V. On forward biasing gate, i.e., for a positive gate current, the concentration of holes and electrons in the channel rises, resulting in a conductivity modulation of the drift region. This clearly demonstrates the ability of the gate to inject excess holes into the n-drift region. When the drain voltage is increased to V_{DS} = 5 V at J_G = 7 A $A.cm^{-2}$, the holes are pushed deeper toward the source, making the low- resistance conductivity-modulated region shorter, as shown in Fig. 4.16. The presence of the conductivity-modulated region and its variation with the drain voltage can also be observed by calculating the electric field in the drift region, as shown in Fig. 4.17. It can be seen that, for V_{DS} = 1 V, the low-electric- field region (i.e., the conductivity-modulated region) is longer when compared to V_{DS} = 5 V.

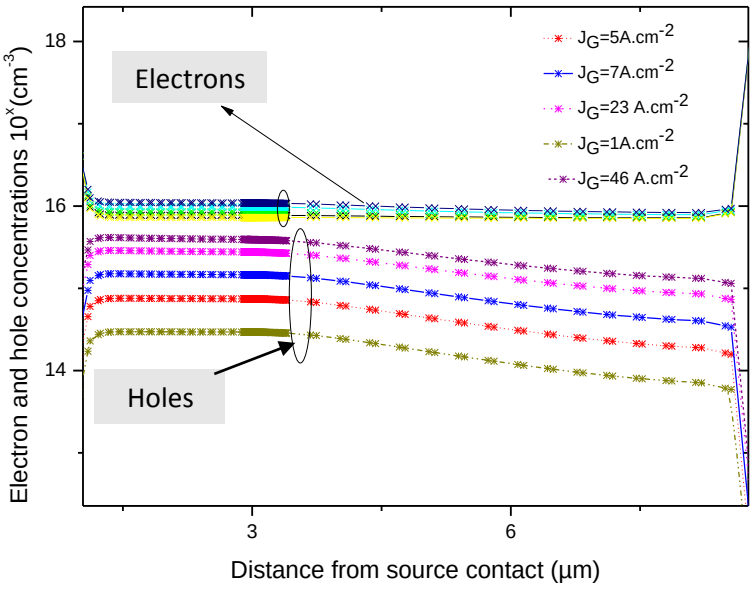


Figure 4 .15: Electron and hole concentration at different gate current (V_{DS}=0V).

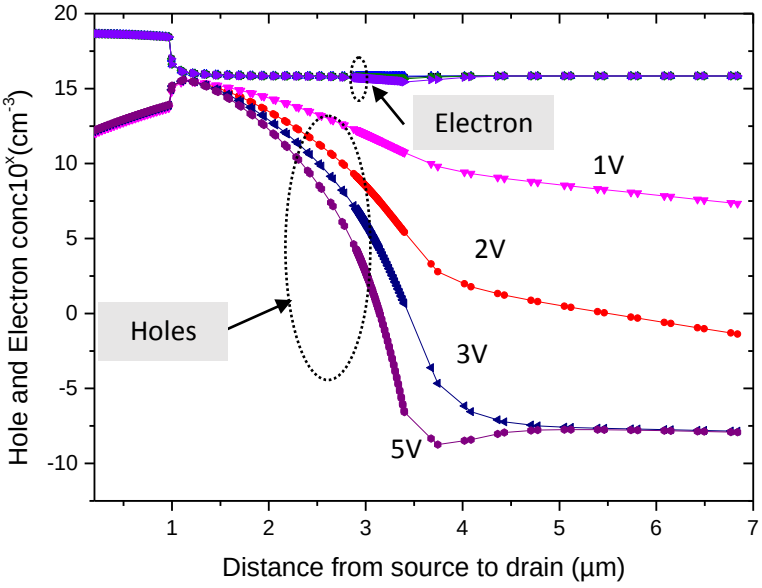


Figure 4 .16: Hole and electron concentrations in the channel from source to drain at J_G =7 A.cm^{-2} and V_{DS} = 1 V; V_{DS} = 2 V; V_{DS} =3V and V_{DS} = 5 V.

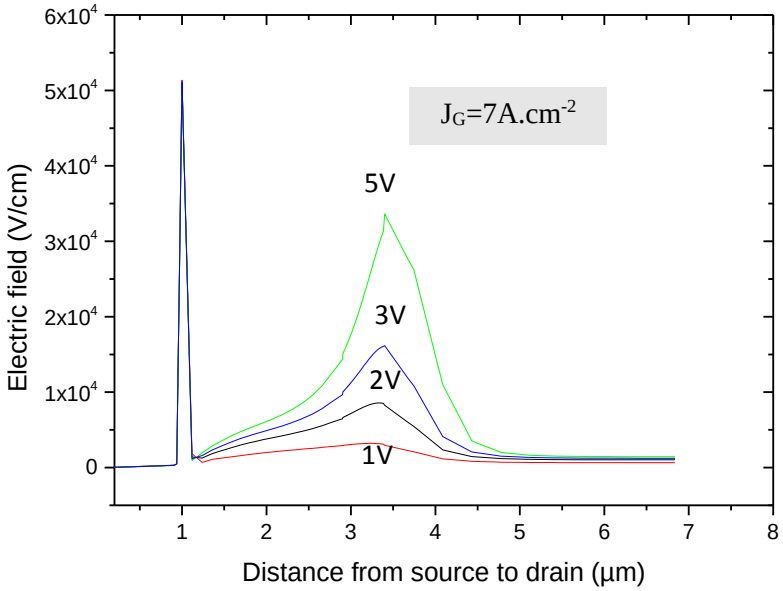


Figure 4 .17: Electric-field variation in the channel for V_{DS} = 1 V; 2V; 3V and 5 V.

4.5.3 Output Characteristics

The simulated output characteristics of the BMFET are shown in Fig. 4.18 for different gate currents. . It can be seen that, as the drain voltage is increased, the slope of the drain current curve reduces. However, with an increasing drain voltage, the drain current continues to increase, since the plasma region, which is responsible for the conductivity modulation of the drift region, is pushed away from the drain terminal Fig4.16. Due to the conductivity modulation of the drift region populated by holes and electrons, the saturation voltage is, however, extremely small.

The transistor shows a behaviour very similar to normally-off bipolar transistor with an additionally gate-current dependent on-resistance and a similar to HBT with large offset voltage, which was discussed in silicon BMFET [146]. The values of the off-set voltage and the strong drain-voltage dependence on drain current in saturation are very similar to the normally-on GaAs BMFET [147].

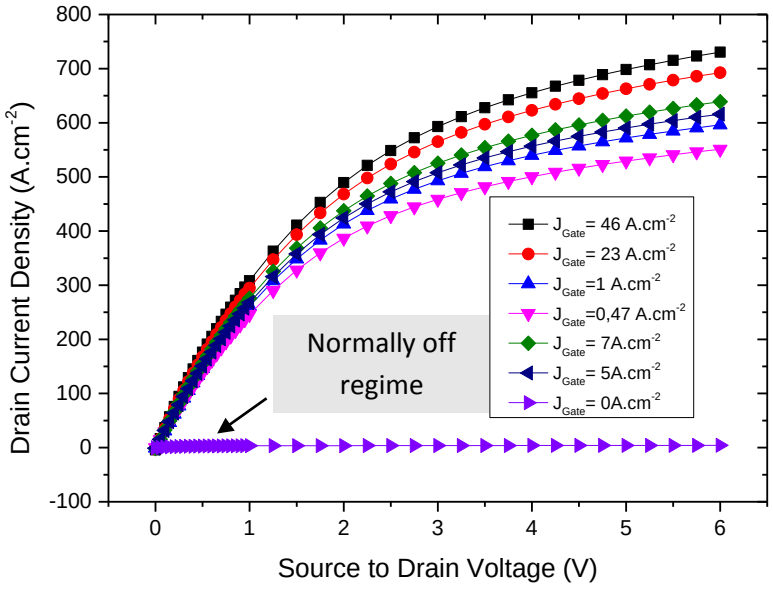


Figure 4 .18: BMFET forward J-V characteristics for different gate biases.

4.5.4 I-V characteristics of 4H-SiC BMFETs with Multiple Deep Level Traps (DLT)

Ionizing particles produces material defects mainly around their end of range due to the dominance of nuclear scattering processes. These defects lead to deep states in the forbidden energy gap where carriers recombine. It has also been shown that nitrogen donors in SiC are deactivated [149], as a result of energetic ions' induced defects. Both of these effects lead to a reduction of charge carrier densities. Higher concentration of defects may also lead to reduced carrier mobility. As a result, a highly resistive layer in the material is produced [150]. The material defects can also be introduced during device fabrication (described in Section 1.2). These defects also have a negative influence on the device performance. In the device simulator, material defects can be modeled by introducing traps in the device to obtain an insight into the device behavior in the presence of defects/traps. Additionally, bipolar degradation could be understood from this type of study, which is mainly caused by stacking faults already present in the material. Stacking faults can also be induced due to ion irradiation and lead to the degradation of the device. A theoretical investigation is conducted to quantify the effect of traps located at drift region in a SiC BMFET.

The mostly three deep level traps observed in 4H-SiC substrate are $Z_{1/2}$, $RD_{1/2}$, $EH_{6/7}$ (Chapter 1). The study is conducted for different values of capture cross-sections for electrons and holes ($\sigma_{n,p}$ = 1×10^{-12}, 1×10^{-13}, 1×10^{-14} and 1×10^{-15} cm^2), and traps concentrations ranging from 1×10^{13} to 1×10^{16} cm^{-3}. The capture cross-section values are taken from previous experimental studies [151,150,152].

Most researchers report that the intrinsic deep levels observed by DLTS in the upper half of the band gap are acceptor like. These traps have been listed separately because of the differences in capture cross section coefficient, which is shown in table 4.2.

Name of Trap	Trap location (eV)	Trap con(N_t) (cm^{-3})	Trap c/s of electron (cm^2)	Trap c/s of hole (cm^2)
$Z_{1/2}$	0.67	$3.8x10^{15}$	$2x10^{-14}$	$3.5x10^{-14}$
$EH_{6/7}$	1.65	$3x10^{15}$	$2.4x10^{-15}$	$3.5x10^{-15}$

Table 4.3: Deep levels by DLTS reported in the literature in the upper half of the band gap of 4H-SiC with location of trap level from conduction band.

4.5.4.1 Output characteristics of 4H-SiC BMFET with Z1/Z2 Trap Effects.

The canal layer in a BMFET transistor plays an important role for the current-voltage properties of the device, for instance, for determining the on-state resistance. Therefore, carrier traps in this layer can influence the overall characteristics of the device. For this purpose, Nt with different concentrations is studied at the canal in the drift region. Figure 4.19 shows the IV characteristics output of the BMFET transistor with different densities of the Z1/Z2 defects for acceptor type with capture cross-section of $\sigma_n = 2\times10^{-14}$ cm^2 and $\sigma_p = 3.5\times10^{-14}$ cm^2. Degradation due to traps in the canal is dependent on their concentrations. Simulations are performed for acceptor and donor type traps, but the degradation in device performance appears only due to acceptor type traps. The concentration of traps has been observed as an important parameter that controls the device output. In the present study, Nt concentrations was fixed to $1x10^{13}$, $1x10^{14}$, $1x10^{15}$ and $1x10^{16}$ cm^{-3} respectively in the drift region from the source to the drain. It has been seen that the value of drain current is reduced to around $10A.cm^{-2}$ from $550A.cm^{-2}$ which is caused by increasing trap density. A maximum current decrease appears when the traps concentration is in the order of $1x10^{16}cm^{-3}$. The study reveals also that the traps do not strongly affect the device characteristics by trapping electrons at biases below 0.6 V exempt for trap density exceeding the epilayer doping.

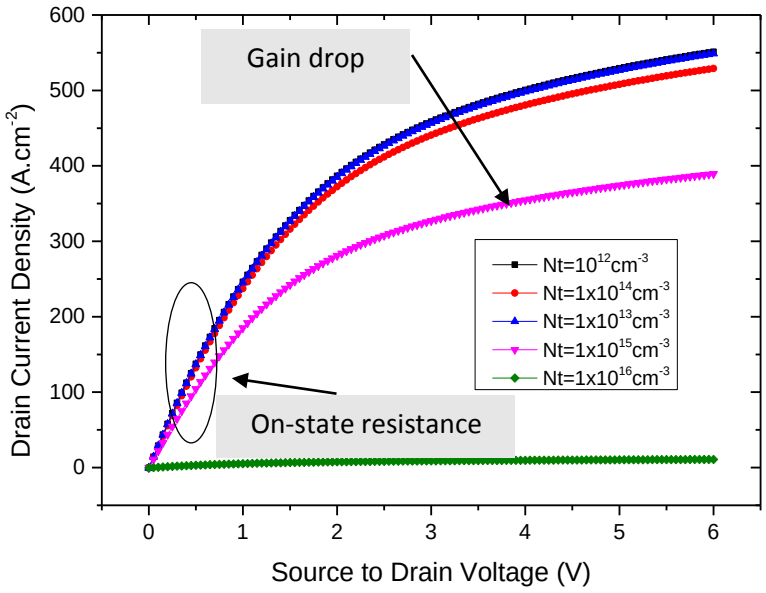


Figure 4 .19: Effect of increasing concentration of Z1/Z2 traps in the canal with $\sigma_n = 2\times10^{-14}$ cm^2 $\sigma_p = 3.5\times10^{-14}$ cm^2 (capture cross-section for electrons and holes has been considered to be unchanged in all simulations). The gate current used in these simulations is 7A/cm^2.

However, as Nt is increased a region with increased resistance appears before saturation of the drain current at a certain gate current appears, and the effect becomes more prominent at a trap concentration of $1x10^{15}cm^{-3}$ (Figure 4.19). The main reason for this behavior is the barrier in the flow of electrons due to trapped electrons in accepter type traps in the canal, which increases the local recombination rate (Figure 4.21) [155]. The effect of donor traps is negligible, since the excess carrier are only electrons (Figure 4.20).

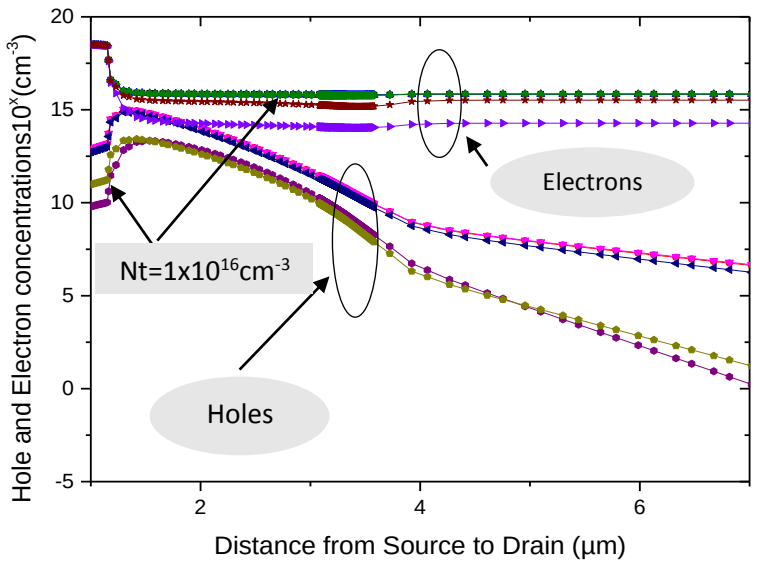


Figure 4.20: Hole and electron concentrations in the channel from source to drain at J_G =7A/cm^{2}and V_{DS} =1V at different Z1/Z2 Trap concentrations.

If high basal plane dislocation (BPD) (see chapter 1) density is present. It is widely believed that stacking faults (SFs) are created by the recombination of electron-hole pairs at the BPDs, which acts as a nucleation site. When the BMFET operates in the quasi-saturation or saturation region, the source and the drain regions are flooded with electron-hole pairs, and their recombination convert the BPDs (basal plane dislocation) into SFs. These SFs degrade both the current gain and the on-resistance (R_{ON}). The gain is degraded because these SFs reduce the carrier lifetime, whereas the R_{ON} because they act as carrier traps in the canal introducing local high-resistive layer [154].

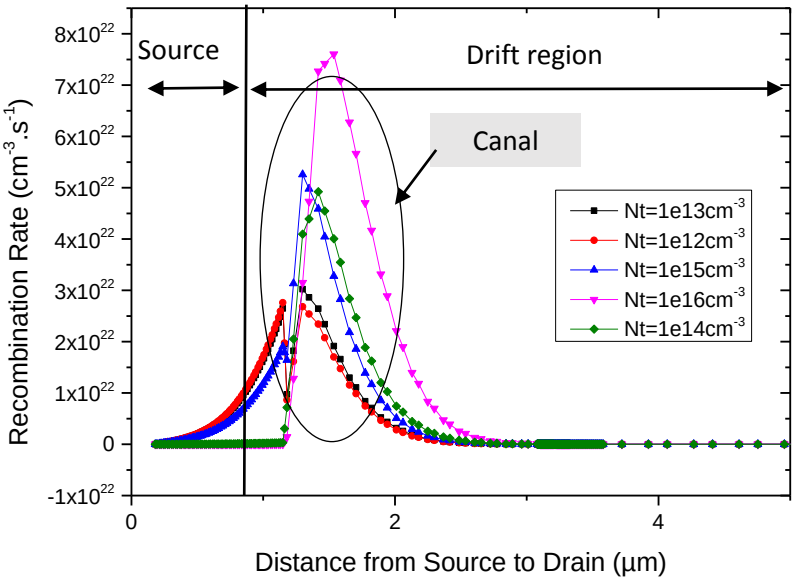


Figure 4.21: Total recombination in BMFETs by introducing Nt with different concentrations in the canal. The recombination rate has been extracted by taking vertical cut for simulated structures.

Moreover, the impact of electron and hole capture cross-sections on the canal characteristics is very evident, and the gain drops more for larger cross-section values, as shown in Figure 4.22. The excess carriers (electrons and holes) flowing through the canal at a certain bias voltage are trapped, giving rise to recombination rate in the trapped region and decreasing the local concentration of the carriers (Figure 4.23). In a similar way, when the concentration of traps is increased, i.e. more trapped electrons, a drop in the current gain occurs due to an increased rate of recombination in the canal. An important factor for the low degradation in gain is the emitter doping level which is of the order of ~10^{19} cm^{-3}. Therefore, it can be deduced that the emitter region is less sensitive for the degradation of the BMFET due to the presence of traps.

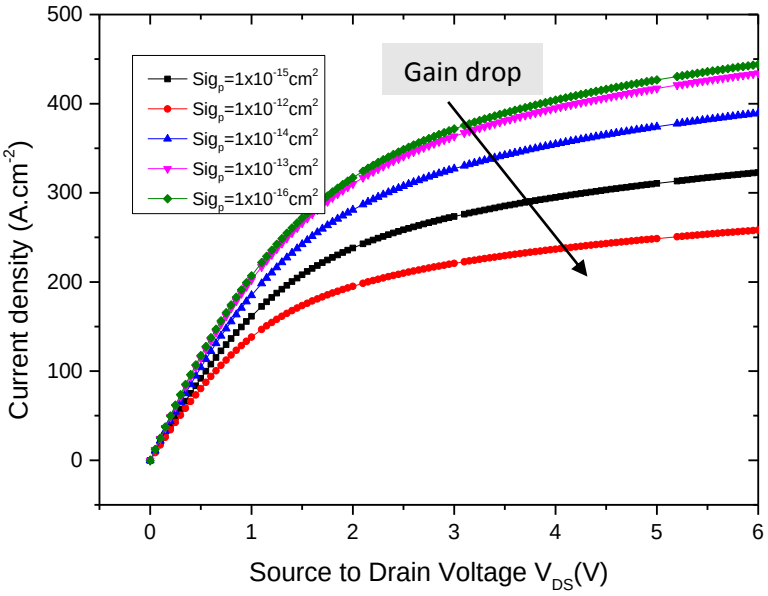


Figure 4.22: Effect of increasing cross section of Z1/Z2 traps in the canal with (Trap concentrations for holes has been considered to be same in all simulations Nt =1×10^{15}cm^{-3}). The gate current used in these simulations is 7A/cm^2.

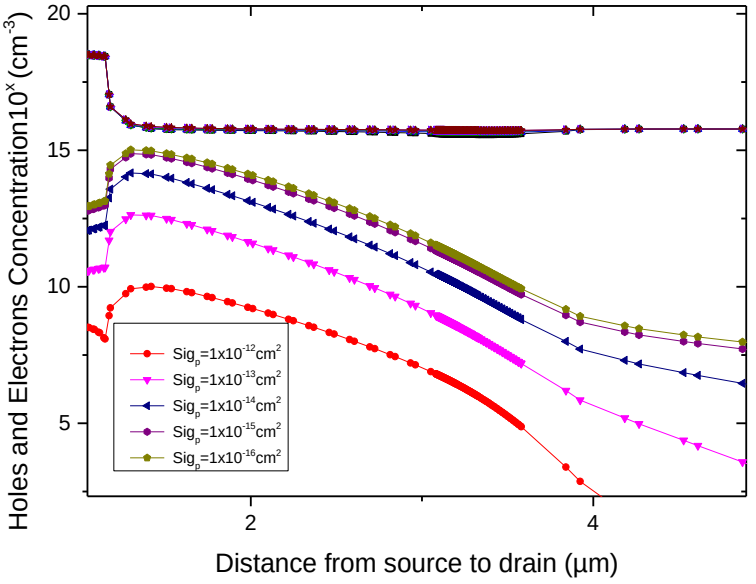


Figure 4.23: Hole and electron concentrations in the channel from source to drain at J_G =7A/cm^{2}and V_{DS} =1V at different Z1/Z2 Trap cross sections.

4.5.4.2 Output characteristics of 4H-SiC BMFET with EH6 /EH7 Trap Effects

The Output characteristics of the BMFET for different Nt values of EH6/EH7 are reported in Fig 4.24. As can be seen, all curves exhibit a linear region at low biases (V_F < 0.6 V), while their behaviour is dominated by a series resistance at higher voltage values. Moreover, as can be noticed, the linear region of the I-V curves becomes smaller and shifts toward higher voltages with increasing trap concentration. At the same time, the current decreases in the series resistance region too. From the Simulation it appears clear that the trap concentration above $10x10^{14}$ cm^{-3} modifies the electrical properties of the device, i.e., to the current gain and the series resistance, where similar devices, although BJT instead of BMFET, reported from another group [156] showed the same phenomena.

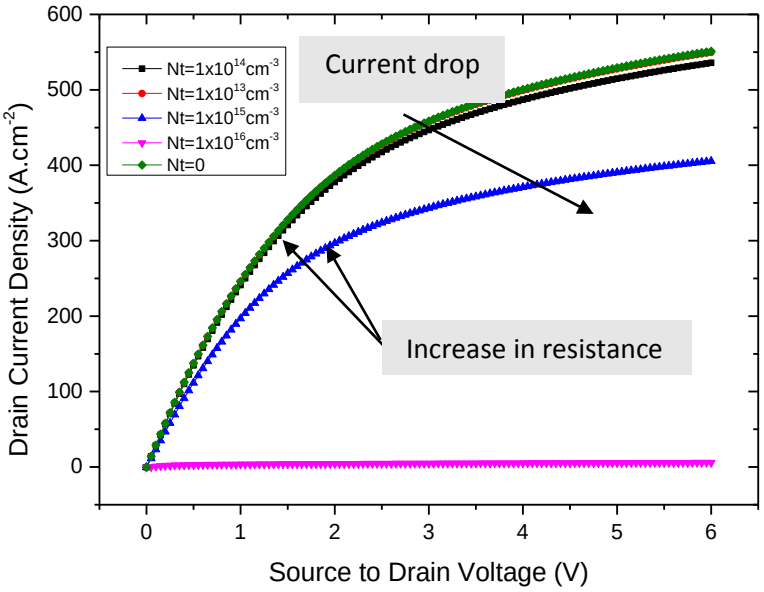


Figure 4 .24: Effect of increasing concentration of EH6/EH7 traps in the canal with $\sigma_n = 2\times10^{-14}$ cm^2 and $\sigma_p = 3.5\times10^{-14}$ cm^2 (capture cross-section for electrons and holes has been considered to be unchanged in all simulations). The gate current used in these simulations is $7A/cm^2$.

The results from simulations, presented in Figure 4.24 indicate also that the trap concentration above 4×10^{15} cm^{-3} with electron and hole capture cross-section of $\sigma_n = 2\times10^{-14}$ cm^2 and $\sigma_p = 3.5\times10^{-14}$ cm^2 follow the same trend as it has been obtained by Z1/Z2 trap in the canal region. This comparison suggests that the carrier concentration in the highly damaged.

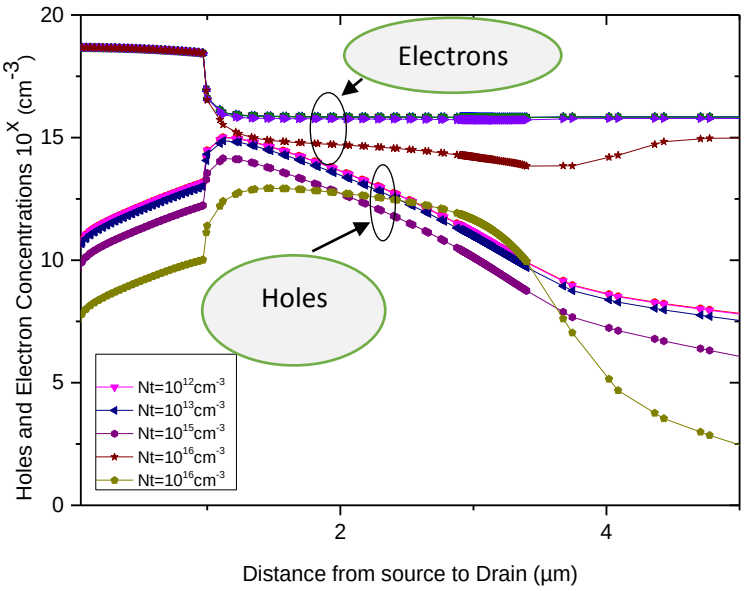


Figure 4.25: Hole and electron concentrations in the channel from source to drain at J_G =7A/cm^{2}and V_{DS} =1V at different EH6/EH7 Trap concentrations.

region (N_t =10^{16}cm^{-3}) in the canal is reduced after introducing traps Fig 4.25, although it is not possible to say if the lower carrier concentration is due to the deactivation of nitrogen dopants, or a high concentration of traps resulting in increased trapped electrons in the drift region and producing compensation of carriers. It has been seen in the simulations that the region, where traps are introduced, the flow of current through the canal is reduced and limits it to a certain level. As a result, a higher resistance is observed in the transistor characteristics.

From fig 4.26, it is seen the effect of traps on the electrical field. The EH6/EH7 concentration traps leads to the apparition of a peak of the electrical field at Y=3.8µm in the drift region where the gas of holes and electrons is located for a source drain voltage of 1V. Being this induced EF in this region, it has to point out the disadvantage of this defect for a better reliability as long as the trap concentrations does not reach a certain value, above which the EF starts increasing. Indeed this is what our simulations revealed, i.e. further increasing the trap concentrations above 10^{15}cm^{-3} the peak of the EF results by far higher than in the other cases. The modification of the EF results in a changing of the depletion region in the sense that wider is the electric field spread and wider is the depletion zone, as it is shown in fig 4.26.

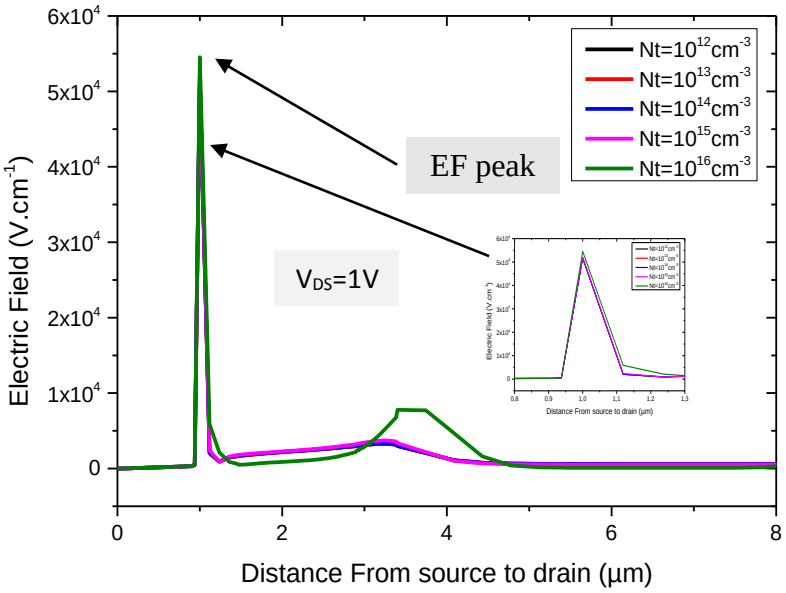


Figure 4 .26: Effect of the EH6/EH7 trap concentration on the Electric Field distribution. Cut in the 2D drift region along the source to drain of the device.

The results from simulations, presented in Fig 4.27 indicate that the electron and hole capture cross-section follow the same trend as it can be obtained by introducing a the Z1 /Z2 traps. It is well shown that the capture cross-section of the EH6/EH7 traps in the drift region strongly affect the output. Fig 4.27 also show that the highest cross-section of the traps (1×10^{-12} cm^2) reduces the gain down to about 67%. In general, when the epilayer is filled with traps, the trapped carriers increase the recombination rate in this region (Fig 4.28). As a result, the flow of current is reduced, which results in the degradation of the current gain.

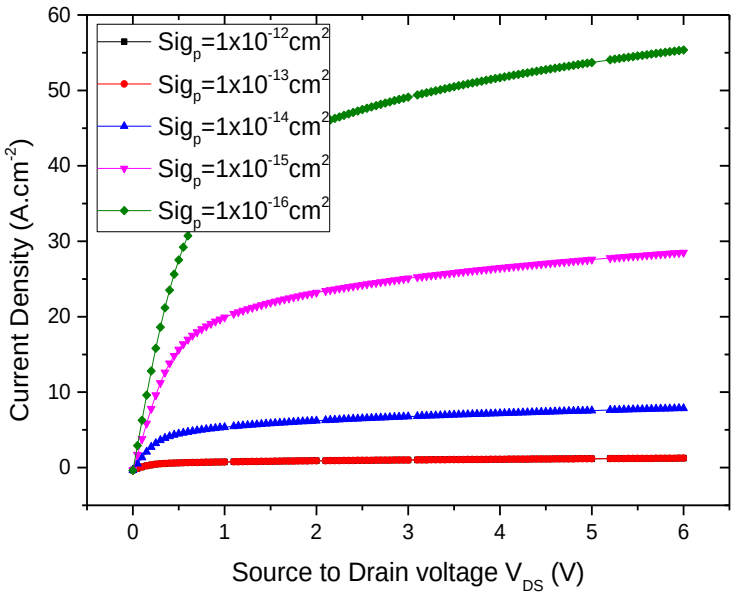


Figure 4.27: Effect of increasing cross section of EH6/EH7 traps in the canal with (Trap concentrations for holes has been considered to be same in all simulations
Nt =1×10^{15}cm^{-3}). The gate current used in these simulations is 7A/cm^2.

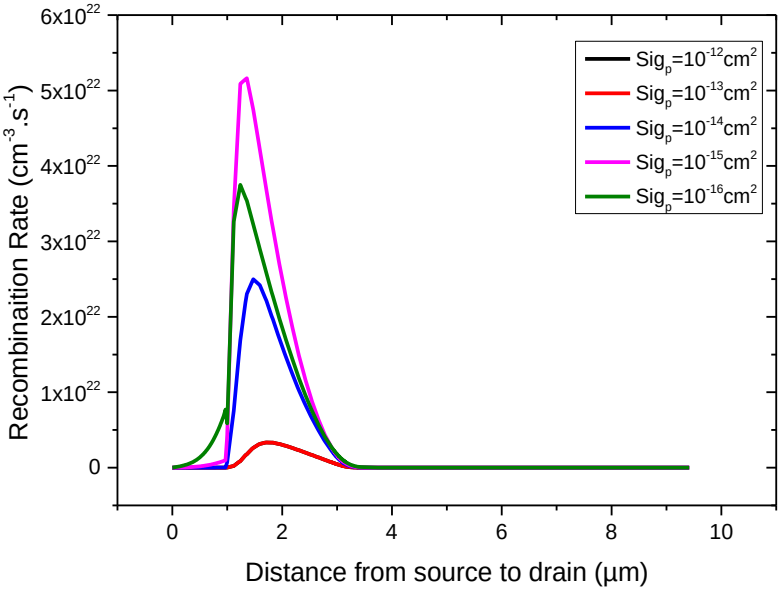


Figure 4 .28: Total recombination by introducing EH6/EH7traps with different capture cross-section in the epilayer. The recombination rate has been extracted by taking vertical cut for simulated structures.

4.6 Optical characterisation

4.6.1 Spectral Response for 4H-SiC D2A.

The spectral responsivity of the D2A was measured by utilizing a Xe arc lamp and a monochrometer. The incident light was focused by a lens, and modulated with a chopper at 1 kHz. Its power was calibrated using a UV-enhanced silicon photodiode. The photocurrent was measured using a lock-in amplifier. Typical responsivity curves as a function of incident wavelength of 4H-SiC D2A is shown in Figure 4.29, with bias at 3Volts.

The spectral response cut-off begins at 380 nm, corresponding to the 3.26-eV indirect bandgap of 4H-SiC. This long-wavelength cut-off is not as sharp as that of direct bandgap semiconductors such as GaN [157]–[159]. Nevertheless, the responsivity drops by four orders of magnitude between 220 and 400 nm, providing acceptable visible-blind performance.

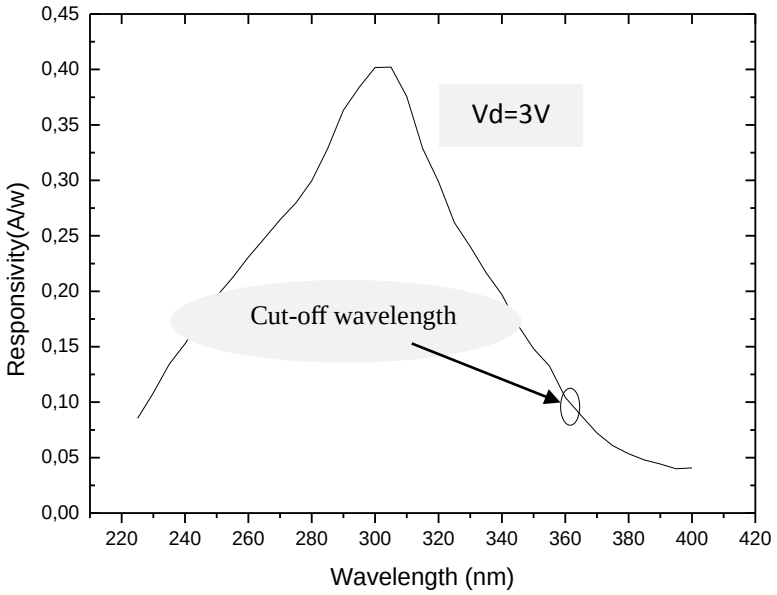


Figure 4.29: Spectral response for 4H-SiC D2A PiN diode.

4H-SiC has its cut-off just around 375 nm. Cut-off wavelength for 4H-SiC should be around 384 nm and it probably is, it just does not show in the measurements since the noise is too high. The higher doping concentration in 4H-SiC seems to play a role in larger current.

4.6.2 Photo Response and I-V Characteristics

I-V characteristics of dark current and photocurrent have been measured in darkness and by illuminating the sample D2A with different UV light sources respectively. Mainly UV-LEDs have been used since they gave better control, stability and higher intensity than a UV lamp. The photocurrents shown in this section come from illumination with a 365 nm UV-LED with a flux density of 0.5mW/cm^{-2} at a distance of about 6 cm between light source and diode. All measurements have been performed at room temperature. The electric current shown in fig 4.30 in this section is the absolute value of the actual current. Of course, a negative bias gives a negative current, but taking the absolute value gives a better idea of the characteristics.

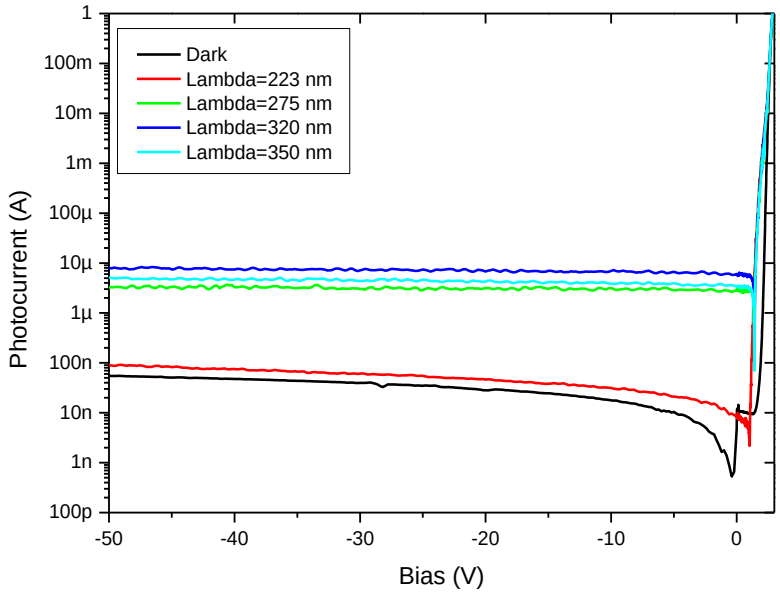


Figure.4.30: Photocurrent of vertical 4*H*-SiC PiN D2A as a function of the reverse bias, under dark conditions and under different illumination wavelengths.

As mentioned before D2A devices were fabricated on 4H-SiC. I-V characteristics were done using a probe station with very sharp needles just touching contact pads of the devices on the top side (Appendix G). A voltage sweep from negative to positive bias was done to measure the current. Since the dark current was very low in 4H-SiC devices special equipment, shielded and with signal filters had to be used to achieve the dark current. Photocurrent could be measured by a manual probe station since the signals were well above the noise level of that equipment, 100 pA.

The I-V characteristics of D2A vertical diodes under dark condition and under different illuminations are shown in Fig. 4.30. The value of the leakage current, measured in dark conditions, was ~1pA at −1 V and below 10nA up to a reverse bias of −50 V. As can be seen in Fig. 4.30, a significant increase of the current of more than two orders of magnitude occurs under an illumination at 320nm. The increase of the photocurrent with the applied reverse bias can be ascribed to the rise of the depleted junction region within the open area, resulting into an increase of the optically active area. When contiguous depleted regions merge, the device operates in the surface pinch-off [160] regime and the optically active area is coincident with the open area. A further increase of the reverse bias, with respect to the pinch-off voltage, does not change the optically active area. For example similar devices, although horizontal instead of vertical, reported from an Italian group [161] showed a magnitude difference of two orders for the same measurements. On the other hand their doping concentration of SiC was nearly the same ($N_d = 2.7 \times 10^{15}$ cm^{-3}), so that could be one reason why D2A device need to be improved.

Conclusions and future outlook

The 4H-SiC PiN diodes characteristics were in general found to agree with established PiN junction I-V-T. Of the three diodes studied using I-V-T techniques, two were found to be well-behaved exhibiting a minimum amount of tunneling current. One classified as very poor, where recombination and tunneling were the dominant current processes at all voltages. For well-behaved diodes, forward I-V-T data showed current conduction due to tunneling below 1.75 V, recombination between 1.75 and 2.85 V, and diffusion processes above 2.85 V. Series resistance was found to be a limiting factor around 2.9V. Recombination currents yielded an activation energy of 1.61 eV and an ideality factor values of 2.02-2.12 compared to the ideal activation energy of 1.6 eV with n=2. An excellent agreement to the measurements has been achieved by a fine-tuning of the technology-dependent carrier lifetime and mobility parameters in the base region. The role of the diode resistance contributions in determining different temperature dependencies of the current behaviours has been pointed out.

Moreover, BMFETs fabricated from SiC, for SiC radiation hardness are studied by exposure to high-energy ion beams with selected energies and fluences. For this purpose, a Multiple Deep Level Traps (DLT) effect has been proposed. In this, different type of traps are presented. Among them, the $Z_{1/2}$ and the $EH_{6/7}$ centers are the dominant and thermally stable defects commonly observed in all as-grown epilayer. An analytically based model of 4H-SiC BMFETs including trapping effects is developed. Then we explained the trapping process with the help of multi deep level trap by including various trap parameters like trap concentration and capture cross section played very important role for reducing of drain current. Therefore, BMFET output simulation lead to the $Z_{1/2}$ defects, which a large capture cross-section for holes, dominate in limiting the minority carriers lifetimes in the n^- epilayer.

Contrary to silicon, SiC does not suffer from the influence of visible light, thanks to its wide band gap energy. This is surely a relevant strength for future possible applications of 4H-SiC BMFET as radiation detectors, which can work in harsh environments forbidden to other types of semiconductor detectors.

PiN diodes have problems with ohmic contacts and low carrier lifetimes. Until these problems are solved, research on SiC is not complete. These fundamental problems need to be resolved. As SiC becomes more and more commercialized due to its superior material properties, there is a prevailing notion that it has matured past the research phase. This is not true by any stretch; much research remains for SiC. Further experimental and theoretical work is required for finally developing the simulation of SiC wide bandgap devices as far as state-of-the-art Si device simulation.

Deep level transient spectroscopy (DLTS) analysis is in progress in order to determine the density of trapping centres (in the range from 10^{14} to 10^{16} cm^{-3}) which are responsible for the major reduction of the minority carrier lifetime (MCL) in n-doped 4H-SiC epitaxial layers.

This thesis has been focused on modeling the dc characteristics of 4H-SiC BMFET for both the linear and saturation regions including multi deep level traps. So one may extend this work by taking ac characteristics (frequency dispersion) into account. Then buffer layer is also neglected between channel and substrate in this thesis, so this work can be extended by considering buffer layer. Finally, there is still some important work in this topic, which can be taken up as future work to improve the model of 4H-SiC BMFET.

Appendix A:

Material parameters for 4H-SiC

	Si	4H-SiC	6H-SiC	3C-SiC
Bandgap energy [eV]	1.12	3.26	3.03	2.4
Relative dielectric ε_s	11.9	9.7	9.66	9.72
Breakdown Field $E_B@N_D=10^{17}cm^3$[MV/cm]	0.3	‖c-axis:3.0	‖c-axis:3.2 ⊥ c-axis >1	>1.5
Thermal Conductivity κ [W/cm K]	1.31	4.9	4.9	3.2
Intrinsic Carrier Concentration [cm^{-3}]	$9.65x10^9$	$5x10^{-9}$	$1.6x10^{-6}$	$1.5x10^{-1}$
Electron Mobility μ_n [cm^2/Vs]	1430	‖c-axis: 900 ⊥ c-axis : 800	‖c-axis: 60 ⊥ c-axis: 400	800
Hole Mobility μ_p [cm^2/Vs]	480	115	90	40
Saturation Electron Velocity *v* [10^7cm/s]	1	2	2	2.5
Donors & Ionization energy [meV]	P:45 As:54	N:50, 92 P:54, 93	N:85,140 P:80, 110	N:50
Acceptors & Ionization energy [meV]	B:45 Al:67	Al:200 B:285	Al:240 B:300	Al:270

Appendix B:

Band gap narrowing C interpreter

```
#include <stdio.h>
#include <stdlib.h>
#include <math.h>
#include <ctype.h>
#include <malloc.h>
#include <string.h>
#include <template.h>


int bgn(double xcomp,double ycomp,double temp,double na,double nd,double
*deg,double *ddegdt)
{
        const To=300; const Nc_300=1.6626e19; const Nv_300=3.29868e19;
const k=8.61738e-5;
        const gD=2; const gA=4; double na_ion; double nd_ion;
        double num1; double num2; double num3; double pow1; double pow2;
double pow3; double pow4;
        double Nc; double Nv; double DEc; double DEv;

        num1=(temp/To);
        pow1=1.5;
        pow2=0.5;
        pow4=0.25;
        pow3=0.3333333;
        Nc=pow(num1,pow1)*Nc_300;
        Nv=pow(num1,pow1)*Nv_300;
        if (na-nd > 0)
        {
```

```
        na_ion=na*(-1+sqrt( 1+4*gA*(na/Nv)*exp(190e-3/(k*temp))
))/(2*gA*(na/Nv)*exp(190e-3/(k*temp)));
        /* printf("na_ion= %e \n",na_ion); */
        num2=(na_ion/1e18);

        DEc=-1*(1.57e-2*pow(num2,pow4)+3.87e-4*pow(num2,pow2));
        DEv=1.3e-2*pow(num2,pow3)+1.15e-3*pow(num2,pow2);
        *deg=DEv-DEc;

          /* printf("pow(num2,pow4)=%e \n", pow(num2,pow4));*/
          /* printf("pow(num2,pow2))=%e \n",pow(num2,pow2)); */
          /*printf("in p+= %e \n",*deg);*/
          /* printf("Temp= %e \n",temp);*/
        }
     else
        {
        nd_ion=nd*(-1+sqrt(1+4*gD*(nd/Nc)*exp(70e-
3/(k*temp))))/(2*gD*(nd/Nc)*exp(70e-3/(k*temp)));
        /* printf("nd_ion= %e \n",nd_ion);*/
        num3=(nd_ion/1e18);
        DEc=-1*(1.5e-2*pow(num3,pow3)+2.93e-3*pow(num3,pow2));
        DEv=1.9e-2*pow(num3,pow4)+8.74e-3*pow(num3,pow2);
        *deg=DEv-DEc;

        /* printf("DEcn=%e \n", DEc);*/
        /* printf("DEvn=%e \n",DEv);*/
        /*printf("in n+= %e \n",*deg);*/
          /*printf("Temp= %e \n",temp);*/
        }
        *ddegdt=0;
        return(0);
}
```

Appendix C:

Gummel iteration method

Gummel's method solves the equations with a decoupled procedure. If we choose the quasi-Fermi level formulation, we solve first a nonlinear Poisson's equation. The potential obtained is substituted into the into the continuity equations, which are now linear, and are solved directly to conclude the iteration. The result in terms of quasi-Fermi levels is then substituted into Poison's equations until convergence is reached [162].

In order to check for convergence, one can calculate the residual obtained by positioning all the terms to the left hand side of the equation and substituting the variables with iteration values. For exact solution values, the residual should be zero. Convergence is assumed when the residuals are smaller than a set to tolerance. The rate of convergence of the Gummel method is faster when there is little coupling between the different equations.

The computational cost of one Gummel iteration is one matrix solution for each carrier type plus one iteration solution for linearization of Poisson's equations is necessary, since the equilibrium Fermi level is constant and coincide with both quasi-Fermi levels.

Let take in 1D case at equilibrium, solve the Poisson's equation only as the exact expression for the carrier concentration are known. Substitute equation 5.1 and 5.2 into Poisson's equation to give equation 5.3 [162].

$$n = n_i \exp\frac{q(V-\varphi_n)}{k_B T} \tag{5.1}$$

$$p = n_i \exp\frac{q(\varphi_n-V)}{k_B T} \tag{5.2}$$

$$\frac{d^2v}{dx^2} = \frac{q}{c}\left[n_i exp(-q\varphi_n)exp\left(\frac{qv}{K_B}\right) - n_i exp(q\varphi_p)exp\left(-\frac{qv}{K_B}\right) + N_A - N_D\right] \tag{5.3}$$

At equilibrium $\varphi_n = \varphi_p$ (Fermi level taken as reference for potential energy). The equation have been scaled by using the (minimum) extrinsic Debye length for the space charge coordinate x, and thermal voltage $\frac{K_B T}{q}$ for the potential V. Indicating with $\bar{V}$ and $\bar{x}$ for normalized potential and space charge [163].

$$\frac{d^2\bar{V}}{dx^2} = \frac{n_i}{N}\left[\exp(\bar{V}) - \exp(-\bar{V}) + \frac{N_A-N_D}{n_i}\right] \tag{5.4}$$

Eq.5.4 is now the Poisson's equation at equilibrium. It can be solve using quasi linearization procedure. Below is the list of procedure.

1. Set initial guess for potential V.
2. Potential at next iteration as $V_{new} = V + \delta V$, write Poisson's equations for V_{new} for substitution.

$$\frac{d^2\bar{V}}{d\bar{x}^2} + \frac{d^2\delta V}{d\bar{x}^2} = \frac{n_i}{N}\left[\exp(\bar{V}).\exp(\delta V) - \exp(-\bar{V}).\exp(-\delta V) + \frac{N_A - N_D}{n_i}\right] \quad (5.5)$$

3. Use linearization exp ($\pm\delta V$) ≈1+ δV and discretize equation 5.5. This will give you equation 5.6 that solves for δV(i) and it as an equation has a triangular matrix.

$$\delta V(i-1) - \left[2 + \frac{n_i}{N}\Delta^2 x\left[\exp\left(\bar{V}\ (i)\right) - \exp\left(-\bar{V}\ (i)\right)\right]\right]\delta V(i) + \delta V(i+1) = -\bar{V}(i-1) + 2\bar{V}(i) - \bar{V}(i+1) + \frac{n_i}{N}\ \Delta^2 x\left[\exp(\bar{V}\ (i) - \exp(-\bar{V}\ (i) + \frac{N_A - N_D}{n_i}\right] \quad (5.6)$$

4. Next is to check for convergence. When the residual of equation 5.4 calculated, convergence is achieved when the nominal of the residual is smaller than a present tolerance. When the convergence is not achieved, return to step 2.In practice people usually check the nominal of the error stated in equation 5.7.

$$\|\delta V\|^2 \leq Tol \quad or \quad \|\delta V\|_{\infty} \leq Tol \quad (5.7)$$

For the solution of Poisson's equation, boundary condition are refer to the equilibrium Fermi level. The boundary conditions are the contacts can be stated as tha separation between the Fermi level and intrinsic Fermi level at contacts. After the solution at equilibrium is achieved, increase the applied voltage in steps of $\Delta V \leq K_B T/q$. Equation 5.8 shows the scaled nonlinear Poisson equation [162].

$$\frac{d^2V}{dx^2} = \frac{n_i}{N}\left[\exp(-\varphi_n)\exp(V) - \exp\left(\varphi_p\right)\exp(-V) + \frac{N_A - N_D}{N_i}\right] \quad (5.8)$$

The quasi-Fermi level are also been normalized. When the Einstein's relation are valid, the continuity equations can be written in equation 5.9.

$$j_n = -qn\mu_n\frac{\partial V}{\partial x} + q\mu_n\frac{K_B.T}{q}\frac{\partial}{\partial x}\left[n_i\exp(\frac{q(V-\varphi_n)}{K_B.T})\right]$$

$$= -qn\mu_n \frac{\partial V}{\partial x} + q\mu_n \frac{K_B.T}{q} n \frac{q}{K_B.T}\left[\frac{\partial V}{\partial x} - \frac{\partial \varphi_n}{\partial x}\right]$$

$$= -qn\mu_n \frac{\partial \varphi_n}{\partial x}$$

$$= q\mu_n \left[n_i \exp\left(\frac{q(V-\varphi_n)}{K_B.T}\right)\right].\frac{\partial \varphi_n}{\partial x}$$

$$= q\mu_n n_i \exp\left(\frac{q(V)}{K_B.T}\right).\frac{-K_B T}{q}\frac{\partial}{\partial x}\left(\frac{-q\varphi_n}{K_B T}\right) \qquad (5.9)$$

Equation 5.9 can be compacted to form equation 5.10 and equation 5.11 show you the formula for the holes. The continuity equations is stated in equation 5.12.

$$j_n = a_n(x).\frac{\partial}{\partial x} \exp(-\varphi_n) \qquad (5.12\ a)$$

$$j_p = a_p(x).\frac{\partial}{\partial x} \exp(\varphi_p) \qquad (5.12\ b)$$

$$\frac{\partial}{\partial x}\left[a_n(x).\frac{\partial}{\partial x} \exp(-\varphi_n)\right] = qU(x)$$

$$\frac{\partial}{\partial x}\left[a_p(x).\frac{\partial}{\partial x} \exp(-\varphi_p)\right] = qU(x)$$

Slotboom variables have been used to simplify the notation. The inner derivative has been discretized with difference around the point $(i \pm \frac{1}{2})$ of the interleaved mesh. Variables on the interleaved mesh must be determined very carefully, using consistent interpolation schemes for potential and carrier density, as discussed later. The continuity equations give the tridiagonal system, equation 5.13 shows the new electron continuity equation with Slotboom variables and equation 5.14 for holes.

$$a_n\left(i-\frac{1}{2}\right)\varphi_n(i-1) - \left[a_n(i-1) + a_n 1\left(i-\frac{1}{2}\right)\right]\varphi_n(i)$$

$$+a_n\left(i+\frac{1}{2}\right)\varphi_n(i+1) = \Delta^2 x U(i) \qquad (5.13)$$

$$a_p\left(i-\frac{1}{2}\right)\varphi_p(i-1)-\left[a_p(i-1)+a_p 1\left(i-\frac{1}{2}\right)\right]\varphi_p(i)$$

$$+a_p\left(i+\frac{1}{2}\right)\varphi_p(i+1)=\Delta^2 xU(i) \qquad (5.14)$$

Poisson equation in equation 5.8 is been solved with decoupled iteration initially with a guess for the quasi-Fermi level. Voltage distribution obtained for the previous voltage is usually a good initial guess for the potential. Quasi-Fermi levels are use as the input for Poisson's equation, the quasi-linearization procedure for equilibrium can be used again. The potential is been used to update the $a_n(i)$ and $a_p(i)$.

Equation 5.13and 5.14 are been used to solve in order to provide new quasi-Fermi level values for Poisson's equations. This process was repeated until convergence was reached. The generation-recombination term would generally depends on electron and hole concentrations of the device; therefore, it has to be updated after each iteration.

The result of equation 5.13 for the electron concentration and 5.14 for hole concentration that can update the generation-recombination term [162].

These equation and examples given above are limited to the no degenerate case. If field depend mobility and diffraction coefficient are introduced, minimal change should be necessary, as long as it is still justified to use of Einstein's relations.

For equation 5.15 shows the 2D quasi-linearized Poisson's equation.

$$-\left(4+h^2\frac{n_i}{N}\left[\varphi_n(i,j)\exp(V(i,j)+\varphi_p(i,j)\exp(-V(i,j)\right]\right)\partial V(i,j)$$

$$+[\partial V(i-1,j)+\partial V(i+1,j)+\partial V(i,j-1)+\partial V(i,j+1)]=$$

$$4V(i,j)-V(i-1,j)-V(i+1,j)+V(i,j-1)-V(i,j+1)+h^2\frac{n_i}{N}\left[\varphi_n(i,j)\exp(V(i,j)+\varphi_p(i,j)\exp(-V(i,j)\right]+\frac{N_A+N_D}{n_i})$$

(5.15)

The normalized size is h=$\Delta x=\Delta y$. The thermal voltage $\frac{K_B T}{q}$ has been used to normalize the potential V and the quasi-Fermi levels φ_n and φ_p included in the Slotboom variables $\Phi_{n,p}=\exp(\pm\varphi_{n,p})$.

Equation 5.16 shows the form that the continuity equation will be [162].

$$\nabla.(a(x,y)\nabla\Phi = \pm U(x,y) \tag{5.16}$$

Equation 5.16 will be discretized to form 5.17

$$-\left[a\left(i+\frac{1}{2},j\right)+a\left(i-\frac{1}{2},j\right)+a\left(i,j+\frac{1}{2}\right)+a\left(i,j-\frac{1}{2}\right)\right]\Phi(i,j)+a\left(i+\frac{1}{2},j\right)\Phi(i+1,j)$$

$$+a\left(i-\frac{1}{2},j\right)\Phi(i-1,j)+a\left(i,j+\frac{1}{2}\right)\Phi(i,j+1)+$$

$$a\left(i,j-\frac{1}{2}\right)\Phi(i,j-1)=\pm h^2U(i,j) \tag{5.17}$$

Gummel iteration typically converges relatively slowly, but the method will often tolerate relatively poor initial guesses. The Gummel algorithm cannot be used with lumped elements or current boundary condition. Two variants of Gummel's method can improve its performance slightly. These booth limit the size of the potential correction that is applied during each Gummel loop [162].

The first method, called damping, truncates corrections that exceed a maximum allowable magnitude, it is used to overcome numerical ringing in the calculated potential when bias steps are large (greater than 1V for room temperature calculation). The maximum allowable magnitude of the potential correction must be carefully specified: too small a value slows convergence, while too large a value can lead to overflow. Specifying the damp parameter in method statement activate damping.

The second method limits the number of linearized Poisson equations per Gummel iteration, usually to one. This leads to under-relaxation of the potential update. This "single-Poisson "solution mode extends to the usefulness of Gummel's method to higher currents. It can be useful for performing low current bipolar simulation, and simulating MOS transistors in the saturation region. It is invoked by specifying the single Poisson parameter of the model statement.

Appendix D:

Newton iteration method

Newton method is a coupled procedure, which solves the equations simultaneously, through a generalized of a generalization of the newton-Raphson method for determining the roots of an equation. By writing the Poisson's equation in 5.18 and the pair of continuity equation in 5.19 into residual form to give equation 5.20 [163].

$$\nabla(\nabla V) = q(n - p + N_B) \qquad (5.18)$$

$$\nabla . J_n = qU(n,p) + q\frac{\partial n}{\partial t} \qquad (5.19\ a)$$

$$\nabla . J_p = -qU(n,p) + q\frac{\partial p}{\partial t} \qquad (5.19\ b)$$

$W_V(V, n, p)=0 \quad W_n(V, n, p)=0 \quad W_p(V, n, p)=0 \qquad (5.20)$

Starting from the initial guess V_0, n_0 and p_0, the corrections V, Δ_n and Δ_p are calculated from the Jacobian system to form equation 5.21

$$\begin{vmatrix} \frac{\partial W_V}{\partial V} & \frac{\partial W_V}{\partial n} & \frac{\partial W_V}{\partial p} \\ \frac{\partial W_n}{\partial V} & \frac{\partial W_n}{\partial n} & \frac{\partial W_n}{\partial p} \\ \frac{\partial W_p}{\partial V} & \frac{\partial W_p}{\partial n} & \frac{\partial W_p}{\partial p} \end{vmatrix} = - \begin{vmatrix} W_V \\ W_n \\ W_p \end{vmatrix} \qquad (5.21)$$

Convergence is usually fast for the newton method, provided that the initial conditions is reasonably close to solution, and is in the neighborhood where the solution is unique. There are three equations for each mesh point on the grid and this is the main disadvantage of a full newton iteration. It is related to the computational cost of matrix inversion (one may estimate that a 3Nx3N matrix takes typically 20 times longer to invert than an analogue NxN matrix). Using Taylor's expansion the solution is updated to form equation 5.22; k indicates the iteration number. A relaxation approach is also applied to avoid excessive variation of the solutions at each iteration step. [162]

$$V(k+1) = V(k) + \Delta V(k) \qquad (5.22\ a)$$

$$n(k+1) = n(k) + \Delta n(k) \qquad (5\ .22\ b)$$

$$p(k+1) = p(k) + \Delta p(k) \qquad (5.22\ c)$$

In the Newton-Richardson approach, the Jacobian matrix in equation 5.21 is updated when the nominal value of the error does not decrease according to a present criterion. Generally, the Jacobian matrix is not symmetric positive definitive, and fairly expensive solves are necessary. Iterative schemes have been proposed to solve each step of Newton's method by reformulating equation 5.21 to form 5.23.

$$\begin{vmatrix} \frac{\partial W_V}{\partial V} & 0 & 0 \\ \frac{\partial W_n}{\partial V} & \frac{\partial W_n}{\partial n} & 0 \\ \frac{\partial W_p}{\partial V} & \frac{\partial W_p}{\partial n} & \frac{\partial W_p}{\partial p} \end{vmatrix} \begin{vmatrix} \Delta V \\ \Delta n \\ \underbrace{\Delta p}_{k+1} \end{vmatrix} = - \begin{vmatrix} W_V \\ W_n \\ W_p \end{vmatrix} - \begin{vmatrix} 0 & \frac{\partial W_V}{\partial n} & \frac{\partial W_V}{\partial p} \\ 0 & 0 & \frac{\partial W_n}{\partial p} \\ 0 & 0 & 0 \end{vmatrix} \begin{vmatrix} \Delta V \\ \Delta n \\ \underbrace{\Delta p}_{k} \end{vmatrix} \qquad (5.23)$$

Since the matrix on the left hand side is lower triangular, one may solve decoupling into three systems of equations solved in sequence. Firs, one solves the block of equations (again, one for each grid point).

$$\frac{\partial W_V}{\partial V}(\Delta V)_{k+1} = -W_V - \frac{\partial W_V}{\partial n}(\Delta n)_k - \frac{\partial W_V}{\partial p}(\Delta p)_k \qquad (5.24)$$

Results in eq5.24 is substituted into next block to form equation 5.25.

$$\frac{\partial W_n}{\partial n}(\Delta n)_{k+1} = -W_n - \frac{\partial W_n}{\partial V}(\Delta V)_{k+1} - \frac{\partial W_n}{\partial p}(\Delta p)_k \qquad (5.25)$$

Results in eq5.25 is substituted into last block to form equation 5.26.

$$\frac{\partial W_p}{\partial p}(\Delta p)_{k+1} = -W_p - \frac{\partial W_p}{\partial V}(\Delta V)_{k+1} - \frac{\partial W_p}{\partial n}(\Delta n)_{k+1} \qquad (5.26)$$

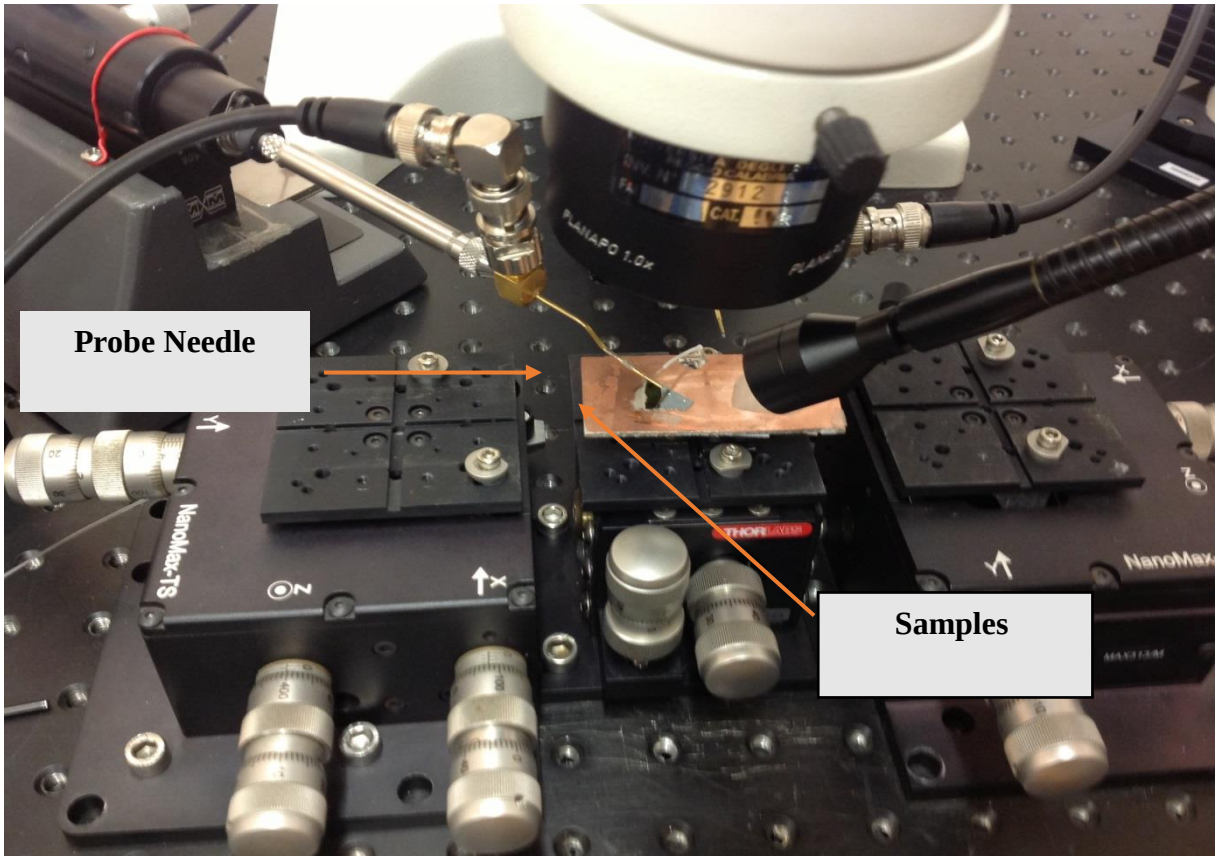
The procedure achieved a decoupling of equations as a block-Seidel iteration, and can be intended as a generalization of the Gummel method. A block-SOR method is obtained if the left hand sides are premultplied by a relaxation parameter. This iteration procedure has better performance if the actual variables are (V, φ_n , φ_p). [162]

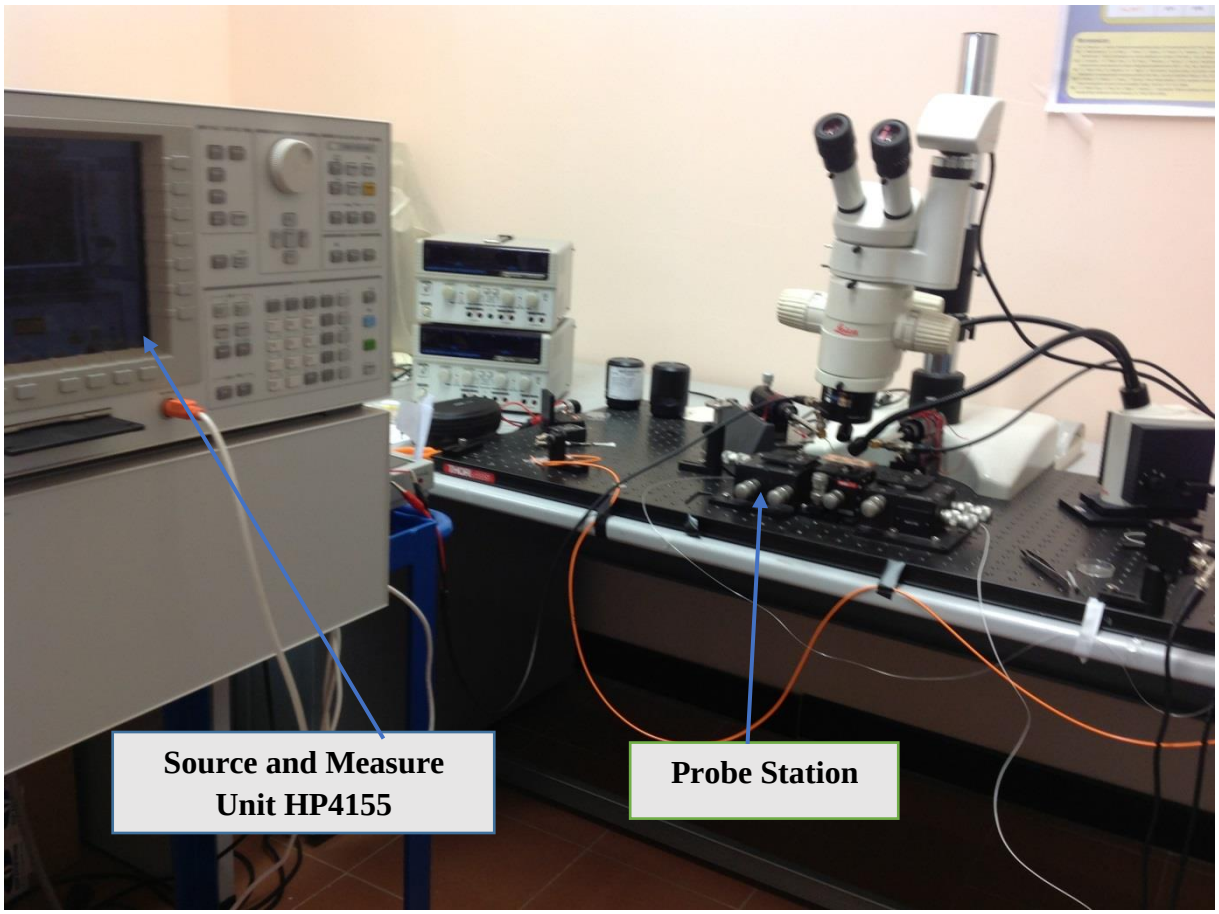
Newton method is the default for drift-diffusion calculation in atlas. There are several calculation for which atlas require that newton's method is used. These are: DC calculation for which that involve lumped elements. Transient calculations, curve tracing; and when frequency-domain small-signal analysis is performed.

The Newton-Richardson method is a variant of the newton iteration that calculates a new version of the coefficient matrix only when slowing convergence demonstrates that this is necessary. An automated New-Richardson is available in atlas, and improves performance significantly on most problems.

Appendix E:

Experiment set up




Source and Measure Unit HP4155
Probe Station

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Analysis of different forward current–voltage behaviours of Al implanted 4H-SiC vertical p–i–n diodes

M.L. Megherbi [a], F. Pezzimenti [b], L. Dehimi [a,c], S. Rao [b,*], F.G. Della Corte [b]

[a] Laboratory of Metallic and Semiconducting Materials, Mohammed Kheider University, 07000 Biskra, Algeria
[b] DIIES – Università Mediterranea di Reggio Calabria, Via Graziella, 89122 Reggio Calabria, Italy
[c] Faculty of Science, Elhadj Lakhdar University, 05000 Batna, Algeria

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ABSTRACT

In this work different experimental current–voltage behaviours of several Al implanted 4H-SiC p–i–n diodes are investigated by means of numerical simulations in a wide range of currents and temperatures. Some devices for which recombination and tunneling are the dominant current processes at all biases are classified as "leaky" diodes. The well behaved diodes, instead, show good rectifying characteristics with a current conduction due to tunneling below 1.7 V, recombination between 1.7 V and 2.5 V, and diffusion processes above 2.5 V. At higher current regimes, a series resistance in excess of 1 mΩ cm^2 becomes the main current limiting factor. Depending on the relative weight between the contact resistances and the internal diode resistance, different temperature dependencies of the current are obtained. A good agreement between numerical and measured data is achieved employing temperature-dependent carrier lifetime and mobility as fitting parameters.

1. Introduction

Silicon carbide (SiC) is a wide band-gap semiconductor with interesting physical properties in order to realize electronic devices well suited to operate under high-temperature, high-power, and/or high-radiation conditions. The potentials of the 4H-SiC polytype, in particular, are expected to enable significant improvements to a far ranging variety of applications and systems [1–5]. However, since this is a relatively new technology, intensive efforts are still necessary to ascertain the detailed physics and the real design benefits that can be obtained by developing simple SiC-based devices. To this extent, in this paper different forward *J–V* behaviours of several Al implanted 4H-SiC vertical p–i–n diodes are investigated by means of measurements and numerical simulations in a wide range of currents and temperatures. In details, diode experimental data and results of a proprietary simulation software [6] are combined to extract key physical parameters, including temperature dependent carrier lifetime and mobility, which aid to differentiate the current transport mechanisms at different biases. The current–voltage characteristics of well behaved and leaky diodes, realised with the some fabrication process, are presented. In addition, the role of the diode internal resistance in determining a crossing point from a positive to a negative temperature coefficient of the current [7–9] is reconsidered by simulations.

The realization of 4H-SiC p–i–n diodes with a negative temperature coefficient of the forward current could be well suitable for stable applications using parallel devices. This study could also turn useful in the design of more complex 4H-SiC power devices, such as the various JFET-based devices recently presented in literature [10–13], where p–i–n diodes are the embedded structures determining the device on- and off-state characteristics.

2. Device structure

The schematic cross-section (plot not in scale) of the investigated Al implanted p–i–n diodes and the calculated net doping profile along the vertical axis of symmetry of a device realized using a 5 μm-thick and 3×10^{15} cm^{-3}-doped epilayer, are shown in Fig. 1.

The diodes were provided by the CNR Institute for Microelectronics and Microsystems – Unit of Bologna (Italy). Details about the adopted technology were provided in [7] and references therein. In short, starting from a commercially available ⟨0001⟩ 8° off-axis 4H-SiC n-type homoepitaxial wafer of elevated crystal quality [14], the diode structure consists of a n$^+$ substrate with a doping concentration in the order of 10^{19} cm^{-3}, a 3×10^{15} cm^{-3} n$^-$ epilayer and a p$^+$ anode region obtained by

* Corresponding author.
E-mail address: sandro.rao@unirc.it (S. Rao).

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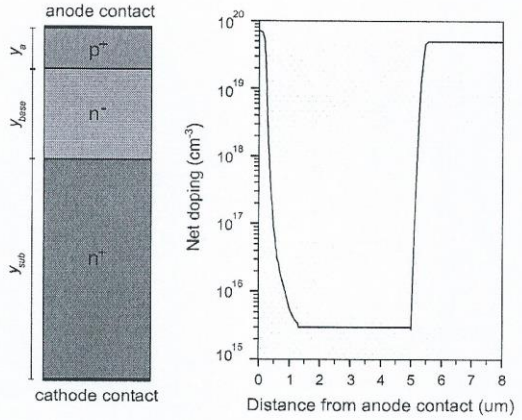

Fig. 1. 4H-SiC p–i–n diode schematic cross-section and net doping profile of a device with a 3×10^{15} cm^{-3}-doped epilayer.

aluminium implant. For the device in Fig. 1 (structure #1) the anode region exhibits a smooth half-Gaussian shaped profile with a peak doping of 6×10^{19} cm^{-3} at the surface, a profile edge located at about 0.2 μm and a profile tail crossing the epilayer doping at 1.35 μm, as verified by SIMS measurements. Almost similar diodes (structure #2) realized using a wafer with an epilayer thickness of 16.5 μm have also been analysed in this paper. The device ohmic contacts are made of a deposited Ni film on the back, while Ti/Al dots were deposited on the anode surface. Details about the implantation process and the post-implantation annealing are again reported in [7]. There, in particular, mainly depending on different post-implantation thermal treatments of the samples, two different anode contact resistances in the order of $1.25 \times 10^{-3}\ \Omega\,\text{cm}^2$ and $2 \times 10^{-5}\ \Omega\,\text{cm}^2$ were measured at room temperature for the structures labelled #1 and #2 in Table 1, respectively. For all the samples, the calculated active area is in the range $0.75–1 \times 10^{-3}$ cm^2.

3. Physical models

The simulation analysis was carried out using the Silvaco's ATLAS simulator. The fundamental 4H-SiC physical models taken into account, such as the incomplete ionization of dopants, the band-gap temperature dependence, the carrier mobility and the carrier lifetime as a function both of doping and temperature, are briefly recalled as follows.

3.1. Incomplete ionization

Due to the wide bandgap of SiC, not all doping atoms can be assumed as fully activated. Using the Fermi–Dirac statistics, the carrier concentration N_a^- and N_d^+ (i.e. the number of ionized acceptors and donors) can be calculated with the expression [15]:

$$N_{a,d}^{-,+} = N_{a,d}\left(\frac{-1+\sqrt{1+4g_{a,d}\frac{N_{a,d}}{N_{V,C}(T)}e^{\frac{\Delta E_{a,d}}{kT}}}}{2g_{a,d}\frac{N_{a,d}}{N_{V,C}(T)}e^{\frac{\Delta E_{a,d}}{kT}}}\right) \quad (1)$$

where, N_V and N_C are the hole and electron density of states varying with temperature, N_a and N_d are the p-type and n-type doping concentrations, ΔE_a and ΔE_d are the acceptor and donor energy levels, and $g_a = 4$ and $g_d = 2$ are the appropriate degeneracy factors of the valence and conduction band. Considering the nature of the doping species (i.e. Al and N), an ionization energy level $\Delta E_a = 190$ meV and $\Delta E_d = 70$ meV is assumed [16,17].

3.2. Band gap model

The temperature dependence of the 4H-SiC band-gap is [18]:

$$E_g(T) = E_{g0} - \frac{\alpha T^2}{\beta + T} \quad (2)$$

where $E_{g0} = 3.26$ eV is the assumed band-gap energy at 300 K, $\alpha = 3.3 \times 10^{-4}$ eV/K and $\beta = 0$ are specific material parameters and T is the lattice temperature.

An apparent band-gap narrowing effect as a function of the activated doping in the p-type and n-type regions, i.e. ΔE_{ga} and ΔE_{gd} respectively, is also included during the simulations according to the Lindefelt's model of the band edge displacements [19]:

$$\Delta E_{ga} = A_a\left(\frac{N_a^-}{10^{18}}\right)^{1/2} + B_a\left(\frac{N_a^-}{10^{18}}\right)^{1/3} + C_a\left(\frac{N_a^-}{10^{18}}\right)^{1/4} \quad (3a)$$

$$\Delta E_{gd} = A_d\left(\frac{N_d^+}{10^{18}}\right)^{1/2} + B_d\left(\frac{N_d^+}{10^{18}}\right)^{1/3} + C_d\left(\frac{N_d^+}{10^{18}}\right)^{1/4} \quad (3b)$$

where $A_{a,d}$, $B_{a,d}$ and $C_{a,d}$, are appropriate 4H-SiC constants.

3.3. Mobility models

The low electric field mobility is modelled by the Caughey–Thomas empirical equation validated for 4H-SiC in [20]:

$$\mu_{n,p} = \mu_{0n,p}^{\min}\left(\frac{T}{300}\right)^{\alpha_{n,p}} + \frac{\mu_{0n,p}^{\max}\left(\frac{T}{300}\right)^{\beta_{n,p}} - \mu_{0n,p}^{\min}\left(\frac{T}{300}\right)^{\alpha_{n,p}}}{1+\left(\frac{T}{300}\right)^{\gamma_{n,p}}\left(\frac{N}{N_{n,p}^{crit}}\right)^{\delta_{n,p}}} \quad (4)$$

where N is the local (total) concentration of the ionized impurities. The model parameters $\mu_0^{\min}$, $\mu_0^{\max}$, N^{crit}, α, β, δ, and γ, are taken from [18,20] and summarized in Table 2.

For high electric fields a carrier mobility reduction due to a carrier saturated drift velocity of 2×10^7 cm/s is considered as described in [10].

3.4. Carrier lifetimes

The carrier lifetimes useful to define the Shockley–Read–Hall recombination rate are modelled as functions of doping and

Table 1
Geometrical and doping parameters of different 4H-SiC p–i–n diodes.

	Structure #1 (D1)	Structure #2 (D2)
Anode thickness, Y_a (μm)	0.2	0.5
Anode doping (cm^{-3})	6×10^{19}	1×10^{20}
Base thickness, Y_{base} (μm)	4.8	16
Base doping (cm^{-3})	3×10^{15}	3×10^{15}
Cathode thickness, Y_{sub} (μm)	300	350
Cathode doping (cm^{-3})	5×10^{19}	1×10^{19}

Table 2
4H-SiC carrier mobility parameters.

	n	p
$\mu_0^{\min}$ (cm^2/V s)	40	15.9
$\mu_0^{\max}$ (cm^2/V s)	950	125
N^{crit} (cm^{-3})	2×10^{17}	1.76×10^{19}
α	−0.5	−0.5
β	−2.4	−2.15
δ	0.76	0.34
γ	−0.76	−0.34

temperature by means of a relation derived by the Scharfetter's model [10]:

$$\tau_{n,p} = \frac{\tau_{0n,p}\left(\frac{T}{300}\right)^{\lambda}}{1+\left(\frac{N}{N_{n,p}^{SRH}}\right)^{\kappa}} \quad (5)$$

Here, N is the total doping density for a given device region, $N_{n,p}^{SRH} = 5 \times 10^{16}$ cm^{-3} is a reference constant, and τ_0 is a process-dependent fitting parameter.

4. Experimental results and simulations

The current–voltage measurements were realised by means of a HP4155 Semiconductor Parameter Analyser. Imposing a compliance current of 100 mA, several diodes with the structure #1 and #2 in Table 1 were characterized at different operating temperature. Almost all the samples showed good rectifying behaviours.

4.1. Room temperature analysis

The forward log(J)–V characteristics of good quality diodes labelled as D1A, D1B, D2A and D2B are shown in Fig. 2(a) and (b). For comparison, each figure also reports the characteristic of a typical "leaky" diode (D1C in Fig. 2(a) and D2C in Fig. 2(b)). The good quality diodes are characterised by a sharp turn-on at a threshold voltage close to 2 V and perform at relatively high biases a current densities in the range 10–100 A/cm^2.

By analysing with the aid of numerical and analytical simulations the electron and hole concentrations, as well as the recombination rate depth profiles of similar p–i–n structures at various voltage biases as described in [21,22], four different current regimes can be determined. In details, referring to Fig. 2(a), the current is dominated by carrier diffusion in the region (III) and recombination in the region (II). The diffusion and recombination current mechanisms produce a quick rise in slope, which is a characteristic of high quality, low resistance, and efficient operation. Conversely, the diode D1C conducts a considerably high current at the lowest voltages in region (I), which is a characteristic of conduction through tunneling phenomena. This excess current can be related to a leakage path or a shunt resistance connected in parallel with the principal (ideal) p–i–n junction. In other words, such a shunt resistance has nonlinear characteristics and then the D1C current behaviour can be modelled as due to two diodes with different barrier heights connected in parallel, each contributing to the current independently, where the defective diode has a lower turn-on voltage. This effect is most likely due to an inhomogeneous epitaxial material structure containing intrinsic defects, like micropipes, regardless of the subsequent diode fabrication process [23–25]. From the experimental analysis, a percentage in the order of 20% of the samples has been classified as "leaky" diode. Obviously, this statistic is related to the effective diode size and crystal quality of the starting 4H-SiC wafer.

Finally, at voltages higher than ~2.9 V, all diodes in Fig. 2(a) show a series resistance effect in the region (IV). Here the plots tend to become flat and the current is entirely dominated by a series resistance value that can be considered as the sum of the contact contributions and the diode internal resistance. In this region, the D1C behaviour can be related to the lack of an effective carrier injection through the junction, preventing the setup of a conductivity modulation regime in the low doped middle region.

An analogue analysis on the current transport mechanisms at different biases can be made for the samples D2 in Fig. 2(b), though they show lower current densities in region (IV) if compared to D1, as a consequence of a higher series resistance due to the thicker epilayer and lower doping of the substrate (see Table 1).

The well behaved diodes D1A and D2A were selected in order to fit with simulation results. The parts of the forward current characteristics due to recombination and diffusion phenomena are well suited as reference for the calibration of the carrier lifetime parameters. In particular, from the simulations it is evident that at low and medium current regimes, namely in the voltage bias range 1.8–2.75 V, the total diode current is strongly influenced by the effective carrier lifetime in the base region as shown in Fig. 3 for the diode D1A assuming different values of τ_0 in (5) with a ratio $\tau_{0n}/\tau_{0p} = 5$ [18].

A fitting parameter $\tau_{0n} = 10$ ns for D1A is in accordance with the experimental results measured on similar p–i–n diodes by using both the reverse recovery [26] and the open-circuit voltage decay [27] techniques. For D2A, τ_{0n} results ~3 times lower. This value is due to the existence of a higher concentration of deep-level defects produced by the Al$^+$ ion implantation process probably located near the metallurgical boundary of the p$^+$–n junction [28] and responsible of an explicit carrier recombination effect. The Al implantation into 4H-SiC epitaxial layers, in fact, yields only a fraction of Al atoms that really occupy a substitutional position in the crystal. Therefore, depending on the implantation process and the annealing conditions, a deep-centres density correlated with the non-substitutional Al concentration that produces a donor-like trap effect (the traps are positively charged when empty), with energy levels in the range 0.2–0.3 eV from the valence band edge, can be assumed [29].

4.2. High temperature analysis

Interesting diode behaviours were obtained performing a high temperature analysis for both the D1 and the D2 samples.

The measured and simulated J–V characteristics of the diode D1A at various temperatures are shown in Fig. 4 in semi-log scale.

As the temperature increases the curves tend to shift left and up. This is an explicit effect of the temperature dependence on the carrier lifetime and intrinsic carrier concentration, which are fundamental parameters in determining the recombination and diffusion components of the diode current behaviours. For example, when the testing temperature is at 378 K, the simulations indicate a carrier lifetime value that increases up to about 30 ns in the base region. At all temperatures, the simulated J–V characteristics are in good agreement with the experimental data over several decades for current.

The diode saturation current density, J_s, was also estimated from the simulations at different temperatures. The Arrhenius plot of ln(J_s) against 1000/T is shown in Fig. 5. The best linear fit indicates that the recombination currents determine an activation energy of 1.61 eV. This value is close to the half value of the material band-gap energy.

At the medium biases, namely between 2.5 V and 2.75 V, an ideality factor in the order of 1.3 was extracted in the considered temperature range as shown in Fig. 6.

In the series resistance region of the curves in Fig. 4 only a limited current increase is observed for voltage biases higher than 3 V. A good fit between the simulated and experimental results was achieved considering a temperature dependence of the contact resistance in the order of -5 μΩ cm^2 K^{-1} as experimentally measured in [7] in the 298–563 K temperature range, pointing out a mixing of thermionic and field-effect conductions through the contact-semiconductor interface. This result is also confirmed in [22] where the distributed contact resistance of similar p–i–n diodes was investigated.

In the series resistance region, however, structure #2 exhibits a different J–V–T behaviour, as shown in Fig. 7 for the diode D2A. In fact, although there are weak differences between the D1 and D2 diodes in (a) the current components related to the carrier recombination and diffusion phenomena with a positive

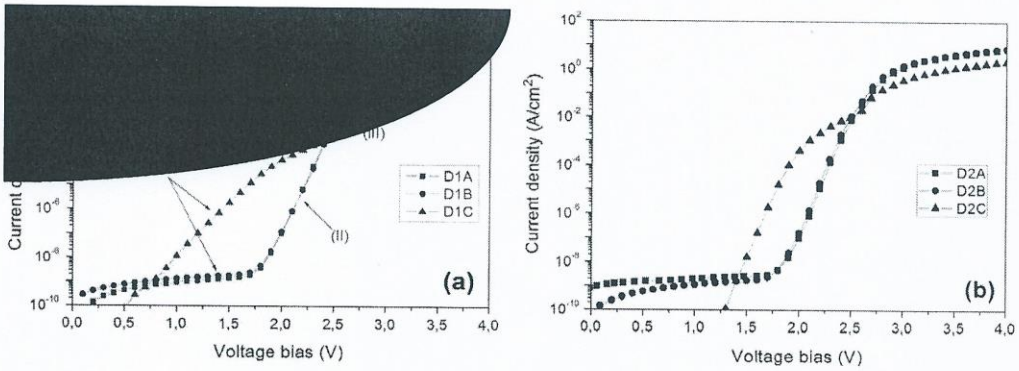

Fig. 2. Forward *J–V* characteristics of several 4H-SiC p–i–n diodes (structure #1 (a), structure #2 (b)) measured at 298 K.

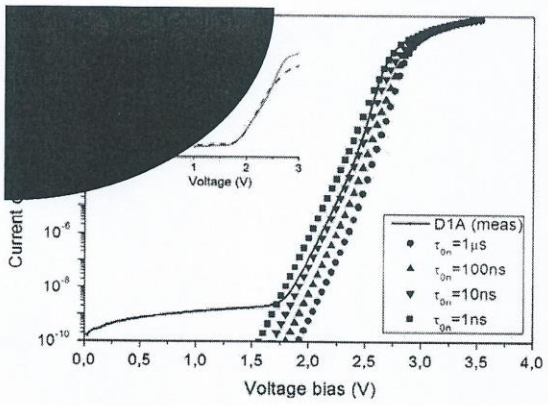

Fig. 3. Calibration of the carrier lifetime simulation parameters for the diode D1A at $T = 298$ K. The inset shows a comparison between the measured *J–V* curves of the diodes D1A and D2A.

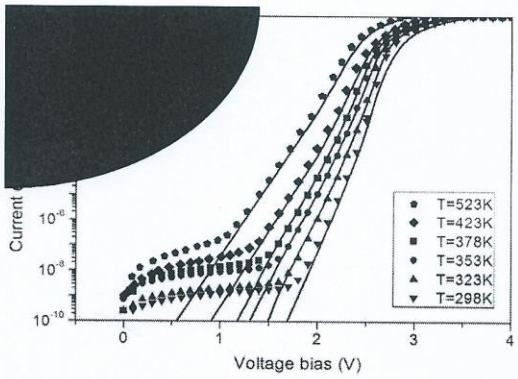

Fig. 4. Simulated (solid lines) and experimental (dot lines) forward characteristics of the diode D1A at different temperatures.

temperature coefficient, (b) the carrier lifetime increasing with temperature and (c) an ideality factor close to 2, we can note the existence for the D2 samples of a crossing point in the *J–V* characteristics as the temperature increases. In particular, for the diode D2A this point is located at a voltage bias close to 2.8 V, corresponding to a current density of 300 mA/cm^2.

Considering the diode series resistance, R_s, in the form $R_s = 2R_c + R_i$, where R_i represents the diode internal contribution and $R_c(D2) < R_c(D1)$ as obtained from measurements [7], whereas for the diode D1A we can assume $2R_c > R_i$ (see the negative temperature coefficient of the curves in Fig. 4), in order to explain the current behaviours shown in the series resistance region of Fig. 7, it is evident that for the diode D2A the R_i effect overcomes the R_c contributions at all temperatures determining a positive temperature coefficient. In fact, since the carrier lifetime is too low to ensure a proper conductivity modulation, the diode internal contribution R_i is mainly determined by the thickness and doping of the epilayer and substrate. Therefore, the carrier mobilities decrease with temperature limits more and more the D2A current capabilities. In particular, $R_i \propto 1/qN\mu_n$ and, in fact, as a consequence of a higher dopant activated in the n$^+$ region that tends to suppress the hole injection in the substrate, above the *J–V* curve knee the total diode current is dominated by the electron injection into the anode. This can be explained with the incomplete ionization model, predicting a ~10 times lower saturation level of the ionized acceptor concentration with respect to donors. In other words, in the anode region the substitutional Al atoms give origin only to a limited concentration of free holes for conduction.

In order to better highlight the temperature dependence of the carrier mobility and to properly fit the measured forward characteristics of the device D2A at highest current regimes, a simplified version of (4) in the form $\mu_{n,p} = \mu_{0n,p}(T/300)^{\alpha}$ was also considered

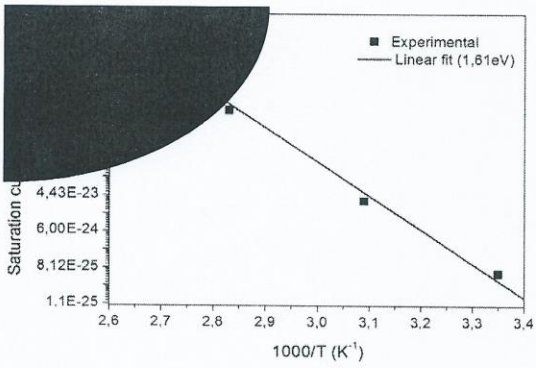

Fig. 5. Arrhenius plot of the diode D1A saturation current density.

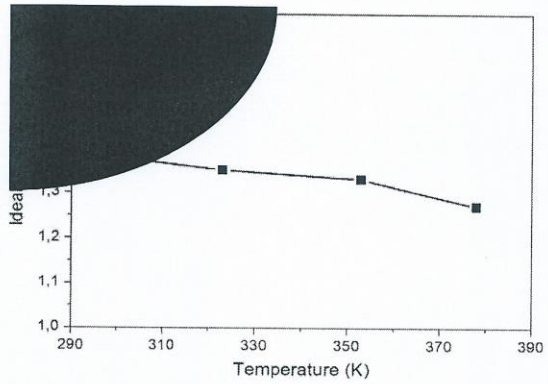

Fig. 6. Ideality factor of the diode D1A between 2.5 V and 2.75 V at different temperatures.

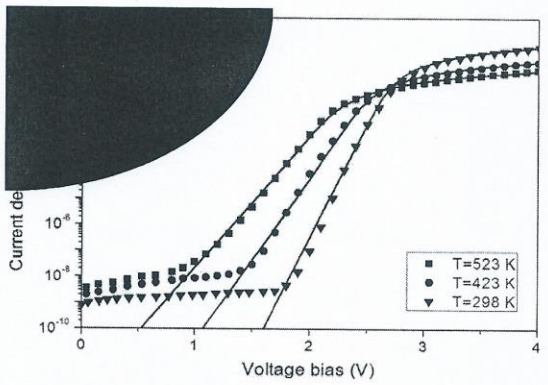

Fig. 7. Simulated (solid lines) and experimental (dotted lines) forward characteristics of the diode D2A at different temperatures.

during the simulations. Assuming $\mu_{0p} = 6\ cm^2/V\ s$ at $T = 300$ K, as measured by Hall effect in [7], the best fit gives $\mu_{0n} = 30\ cm^2/V\ s$ and $\alpha = 5.25$. Such carrier mobility should be considered a minimum value along the diode structure, predicting a diode internal resistance that can be as high as about 10 $m\Omega\ cm^2$. This result explains the limited maximum current handling of the samples D2 compared to D1.

5. Conclusion

The current–voltage characteristics of several Al implanted 4H-SiC p–i–n diodes have been presented reporting experimental and numerical results in the 298–523 K temperature range. The measured forward *J–V* curves show leaky behaved and well behaved diodes with good rectifying characteristics. The latter have been considered for simulation comparison. An excellent agreement to the measurements has been achieved by a fine tuning of the technology-dependent carrier lifetime and mobility parameters in the base region. The role of the diode resistance contributions in determining different temperature dependencies of the current behaviours has been pointed out.

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