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Design of a-IGZO Thin film transistors

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Abstract

Thin film transistors (TFT) have received great attention due to their applications in flat planed display, e-paper and flexible electronics. a-IGZO based TFTs have shown superior performance as far the stability is concerned. However, some issues remain to be treated properly. In this thesis, numerical simulation (by SILVACO ATLAS) was carried out to investigated three problems. The first, the effect of Hydrogen contamination of a-IGZO was investigated. It was found that donor defects near the valance band has no effect, while the mobility degradation induces a degradation in the TFT performance. Acceptor defects states near valance band is the reason of positive V_{th} shift. It is therefore concluded that near valance band defects are not donor defects but acceptor defects with a Gaussian distribution which can also degrade the mobility. The second, is the effect of different gate dielectrics. Four different insulators (SiO_2 Si_3N_4, Al_2O_3 and HfO_2) are examined. It is found that the output performance is significantly enhanced with high relative permittivity of the insulator. The HfO_2 gate insulator gives the best performance: lower threshold voltage 0.23V and subthreshold 0.09 $Vdec^{-1}$, and higher field effect mobility 13.73 cm^2 s^{-1} V^{-1}, on current and I_{on}/I_{off} ratio 2.81×10^{-6} A,5.06×10^{12} respectively. Therefore, The HfO_2 gate insulator showed high stability compared with other gate insulators materials. The third is a comparison of simulation to measurement of ultra-thin channel on the TFT performance. The thinner channel layer was found to have a better performance than the thicker channel layer. The 4 nm-thick, ultra-thin a-IGZO TFT exhibited high saturation mobility (7.56 cm^2 V^{-1} s^{-1}), low threshold voltage (2.73 V), a small value of sub threshold swing (0.22 $Vdec^{-1}$) and a high on/off ratio (1.77×10^8). It was also noticed that the threshold voltage (V_{th}) shifts negatively as the thickness increases. The 4 nm long channel TFT shows more stability under NIBS and PBS while 16 nm have a strong degradation under NIBS and PBS

Résumé

Les transistors à couches minces (TFT) ont fait l'objet d'une grande attention en raison de leurs applications en afficheur à écran plat, en papier électronique et en électronique flexible. Les TFT à base d'a-IGZO ont montré des performances supérieures en ce qui concerne la stabilité. Cependant, certains problèmes restent à traiter correctement. Dans cette thèse, une simulation numérique (par SILVACO ATLAS) a été réalisée pour étudier trois problèmes. Le premier est l'effet de la contamination par l'hydrogène d'a-IGZO a été étudié. On a examiné les défauts donneurs près de la bande de valence n'avaient aucun effet, la dégradation de la mobilité induisant une dégradation des performances du TFT. Les états de défauts de type d'accepteur près de la bande de valence sont la raison du décalage positif de tension de seuil. Il est donc conclu que les défauts proches de la bande de valence ne sont pas des défauts donneurs, mais des défauts accepteurs avec une distribution gaussienne qui peuvent également dégrader la mobilité. Le second est l'effet de différents diélectriques de la grille. Quatre isolants différents (SiO_2, Si_3N_4, Al_2O_3 et HfO_2) sont examinés. On constate que les performances de sortie sont considérablement améliorées avec une permittivité relative élevée de l'isolant. L'isolant de grille HfO_2 donne les meilleures performances : tension de seuil inférieure 0,23V et 0,09 $Vdec^{-1}$ sous-seuil et mobilité de champ supérieure 13,73 $cm^2\ s^{-1}\ V^{-1}$, sur le courant et le rapport marche / arrêt $2{,}81 \times 10^{-6}$ A ; $5{,}06 \times 10^{12}$ respectivement. Par conséquent, l'isolant de grille HfO_2 a montré une stabilité élevée par rapport aux autres matériaux isolants de grille. La troisième travaille est une comparaison de la performance entre simulation et mesure de canal ultra mince . La couche de canal la plus mince s'est avérée plus performante que la couche de canal la plus épaisse. Le TFT ultra-mince a-IGZO de 4 nm d'épaisseur présentait une mobilité de saturation élevée (7,56 $cm^2\ V^{-1}\ s^{-1}$), une tension de seuil faible (2,73 V), une faible valeur de sous-seuil (0,22 $Vdec^{-1}$) et un rapport du curent marche / arrêt élevé ($1{,}77 \times 10^8$). Il a également été remarqué que la tension de seuil (V_{th}) se déplace négativement à mesure que l'épaisseur augmente. Le TFT à canal long de 4 nm montre plus de stabilité sous NIBS et PBS alors que 16 nm ont une forte dégradation sous NIBS et PBS

ملخص

ترانزستور الشرائح الرقيقة حضى باهمتام كبير من اجل تطبيقاته في الشاشات المصطحة ، الاوراق الالكترونية و الالكترونيات المرنة الترنستور انديوم غاليوم زينك اكسيد لا بلوري (a-IGZO) اظهر خصائص مميزة و اسقرار جيد بالاضافة الى نتائج الجيدة لكن هناك بعض الظواهر التي يجب ان تدرس بإهتمام. في هذا العمل استعملت المحاكات الرقمية بواسطة (SILVACO ATLAS) من اجل دراسة ثلاث اشكاليات. اولا، دراسة تأثير شوائب الهيدروجين في مادة انديوم غاليوم زينك اكسيد. الدراسة وجدت ان العيوب المانحة بالقرب من عصابة التكافئ ، ليس لها تأثير، تقهقر الحركية يتسبب في تراجع أداء ترانزستور الشرائح الرقيقة. العيوب الاخدة بالقرب من عصابة التكافئ هي سبب الانزياح الى الموجب لقيم جهد العتبة. وجد ان العيوب من القرب عصابة التكافئ هي عيوب اخذة و ليست مانحة بالاضافة الى انها ذات توزيع غوسي كما ان هذه العيوب تسبب في تراجع قيم الحركية. ثانيا، تأثير عدة انواع من عوازل كعازل لبوابه، تم استعمال اربعة عوازل (اكسد السليوم ، نيتريد السليسوم ، اكسيد الاليمنيوم ، و اكسيد الهفنيوم) لدراسة تأثير العازل ، وجد ان اداء ترانزستور يتحسن بشكل ملحوظ مع عوازل ذات ثابت عزل كبير. العازل اكسيد الهفنيوم اظهر افضل نتائج حيث قيمة جهد العتبة 0.23 V و انحراف ما فوق جهد العتبة $0.09\ Vdec^{-1}$. حركية التأثير الحقلي $13.73\ cm^2\ s^{-1}\ V^{-1}$ تيار الاشتغال و نسبة تيار الاشتغال على تيار الاطفاء كانت على توالي 2.81×10^{-6} A 5.06×10^{12} بالاضافة اكيسد الهفنيوم اظهر استقرار جديد مقارنة مع العوازل الاخرى في هذه الدراسة. ثالثا تمت مقارنة بين محاكات و قياسات تجريبية لترانزستور ذو قناة جد رقيقة .القناة ذو الطبقة الرقيقة اظهرت اداء افضل من القناة الاخثن . السمك 4 نانو متر للقناة ترنسيتور انديوم غاليوم زينك اكسيد لا بلوري اظهرت حركية تشبع عالية ($7.56\ cm^2\ V^{-1}\ s^{-1}$) جهد عتبة صغير ($2.73$ V) ، و قيم صغيرة للانحارف ما فوق جهد العتبة ($0.22\ Vdec^{-1}$) و قيم علية لنسبة التيار الشغيل على تيار الاطفاء .(1.77×10^8) . كما تم ملاحظة ان مع زيادة في السمك نلاحظ انزياح جهد العبتة نحو الاتجاه السالب . السمك 4 نانو متر للقناة ترنستور اظهر اكثر استقرار تحت اجهاد الجهد السالب و الاضاءة و اجهاد الجهد الموجب بينما 16 نانو متر اظهر اكثر تقهقر تحت اجهاد الجهد السالب و الاضاءة و اجهاد الجهد الموجب.

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General introduction

Transistors take much attention in research due to its their application in logical circuits. The development in transistors technology leads to discovery of metal oxide semiconductors transistor which was the secrete of developing numerical technology. Thin film transistors (TFT) is one type of Metal Oxide Semiconductor (MOS) transistors and which have received much attention due to their ease fabrication and wide range applications especially in flat panel display and mobile display.

Many semiconductor materials were used as channel in TFT. a-Si:H was most material used in TFT. Hydrogenated amorphous silicon (a-Si:H) have many disadvantages such as low mobility [1], high defects [2], and instability [3] and it has complicated fabrication [2]. Zinc oxide (ZnO), indium oxide (In_2O_3) and tin oxide (SnO_2), known as transparent oxide semiconductors (TOS) are widely used in TFTs due to their unique properties such high stability in atmosphere, ease of fabrication and high mobility compared to a-Si:H. Most TOS require high temperature to fabricate plus the problems of grain boundary [4]. Those two problems are very critical for industry application. Amorphous transparent oxide (AOS) tend to replace binary TOS and Si:H in TFT technology. AOS can be fabricated at room temperature and deposited on very large scale which attracted TFT producers [5]. Amorphous Indium gallium zinc oxide (a-IGZO) is the most famous AOS. a-IGZO has attracted great attention because of its good properties (high mobility, high transmittance, low defects, atmosphere stability) and good performance a-IGZO based TFTs (small threshold voltage and subthreshold and high mobility , on current) [6]. Designing an optimal a-IGZO TFT is still a challenge, however.

The stability of a-IGZO TFTs, defined by the threshold voltage shift, is a crucial issue for its practical applications. There is an intense ongoing research work investigating possible causes of the threshold voltage shift (ΔV_{th}). One of such possible causes is oxygen vacancies near the conduction band minimum (CBM) states [7]–[9]. The oxygen vacancies are the reason of negative V_{th} shift. The presence of hydrogen creates defect states near the valance band maximum (VBM) [10], [11]. The oxygen disorder is origin of deep defects states [12]. The high density subgap defects in a very deep energy region just above the valance band maximum (near-VBM states) may be other causes of the instability. However, it is not yet known what kind of influence defect near VBM states have on the device performance such as threshold voltage shift. As an important part of the TFT, the gate insulator plays a vital role in its performance. Various gate insulators, such as, silicon dioxide (SiO_2) [13], silicon nitride (Si_3N_4) [14], [15] , Aluminum oxide (Al_2O_3) [16], [17], and hafnium oxide (HfO_2) [18], [19] have been investigated for use in TFTs.

The thickness of channel is an important factor to optimize work of a-IGZO TFT. It has been observed that the a-IGZO TFT stability improved with increasing channel thickness [20]–[22]. By contrast other work showed that a decrease in the TFT channel thickness enhanced its stability [23]–[25]. Therefore, it seems that the experimental investigation the effect of thickness on the stability is not conclusive due to many factors. For example, contamination during the TFT fabrication, density of defects in the channel films, morphology of these films or absorption of ambient gases during or after fabrication. In this work and using numerical simulation, the effect of gate insulators, the channel thickness effect and the defects created by Hydrogen on a-IGZO TFTs performance and stability.

This thesis contains four chapters. In the first chapter the history and physics of thin film transistors is presented. Second chapter deals with the operation and performance of a-IGZO thin films transistors. The simulation and fabrication of a-IGZO TFT are presented in the third chapter. Finally, the fourth chapter details the results obtained in this thesis and their discussion. This thesis finishes with a conclusion and recommendation for further work.

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Chapter I

History and physics of thin film transistors

I.1 Introduction

This chapter introduces the thin film transistor (TFT) history and its development decade by decade until nowadays. After that the physics of metal insulator semiconductor (MIS) is explained. TFT is a type of MIS device. At this section we explain and modulate the phenomena in MIS structure which explain how transistor works.

I.2 History of thin film transistors

The research on thin films transistors started about 80 years ago. It was in that time the understanding about semiconductors become clearer. In this section, decade by decade, how the thin-film transistor has evolved in materials and structure to the forms most widely used today will be reviewed.

I.2.1 Field effect device

The idea of the field effect device started in 1930s with a patent of J.E Lilenfeld [1]–[3] and O. Hei [4]. They suggested a device for controlling an electric current by a voltage. The problem is that no clear idea on how this is this device working of as they failed in describing the invention due to misunderstanding of semiconductors in this period of time.

The patent of J.E Lilenfeld and O. Heil shown in Figure I-1 and Figure I-2 respectively They use Copper Sulfide (CuS) as the active layer, Aluminum(Al) as electrodes and Aluminum Oxide (Al_2O_3) as insulator which has a thickness of about 100 nm. However, this TFT never worked because the thickness of the insulator is quite thick.

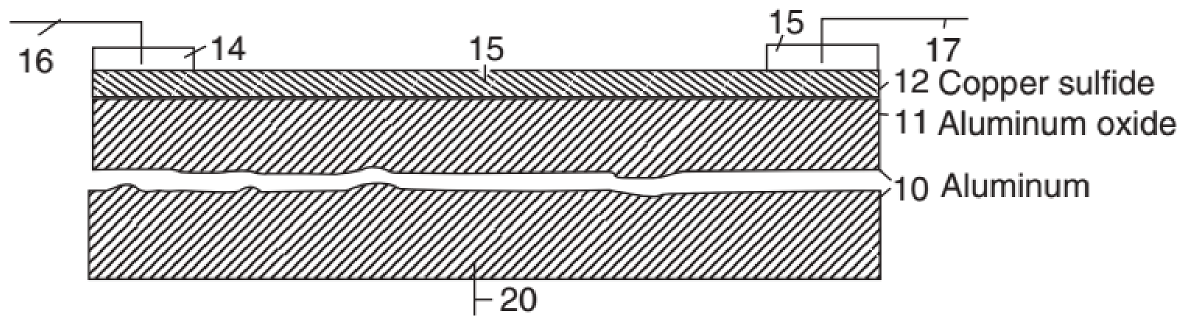

Figure I-1 Diagram of the first field-effect electronic device.

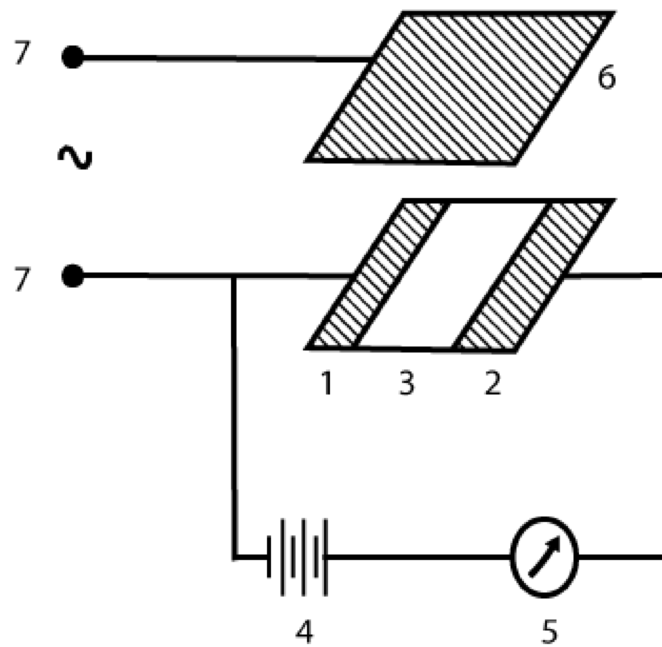

Figure I-2 Diagram of an early field-effect device.

As it is normal with many innovations at that time, its practical realization was delayed until adequate materials and technologies were available for its fabrication. It can be even said (and for most it could be surprising) that the TFT was the first solid-state amplifier ever patented [5], [6].

The work of Shockley on semiconductors and the discovery of the point-contact transistor by Bardeen and Brattain in late 1947 has led to the creation of the first filed effect transistor in 1952. Shockley was able to explain the phenomena of field effect on semiconductors materials.

The TFT as everyone knows it today really began with the work of P. K. Weimer at RCA Laboratories in 1962 [7]. He used thin films of polycrystalline Cadmium Sulfide (CdS) as active layer. The thin film of CdS was deposited by evaporation on a glass substrate, while source, drain and gate contacts are formed by evaporation. Silicon monoxide thin film of insulator is interposed between the gate electrode and the semiconductor. This CdS TFT structure is shown in Figure I-3

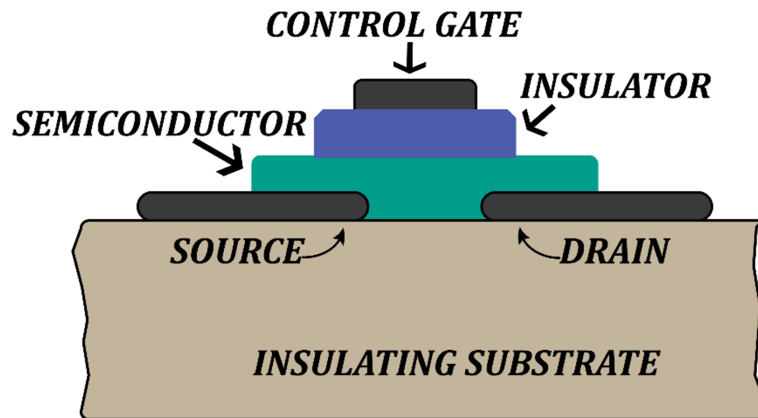

Figure I-3 TFT structure of Weimer's top-gate staggered CdS TFT structure.

The threshold behavior of Weimer's TFTs suggested a fairly large density of interface states. This density was estimated at 10^{12}– 10^{13} cm^{-3}. In 1964 Weimer [8] reported p $channel$ TFTs made with tellurium as the active material. On the theoretical side, Borkan and Weimer published in 1936 [9] their analysis of TFT characteristics. As mentioned earlier, this was based upon Shockley analysis of the JFET, which is now known as the gradual channel approximation.

I.2.2 TFT based on $a-Si:H$ and poly crystal Si

The work of Lecnher et al [10] was a big motivation for research on TFT. They have used TFTs to control the pixel of a liquid crystal displays (LCD), obtaining considerably less crosstalk, lower response time and higher contrast ratios than that achieved when controlling liquid crystals with more conventional $x-y$ disposed electrodes. By this time, the display applications of TFTs were motivating the work of most groups. As a result, efforts were increasingly focused on the issues of stability and ON/OFF ratio, as well as OFF current, or leakage. Stability was a serious

issue. CdSe is a polycrystalline compound; its properties are influenced by grain size, grain boundary interface states, stoichiometry, etc., and it can be sensitive to ambient gases such as H_2O and oxygen. From this time a big debate as to which material was best suited for use in TFTs for most important application such as in liquid crystal displays has started.

Le Comber, Spear, and Ghaith used amorphous silicon (a-Si) as active layer for thin films transistor [11]. Figure I-4 shows the structure of first with a-Si TFT.

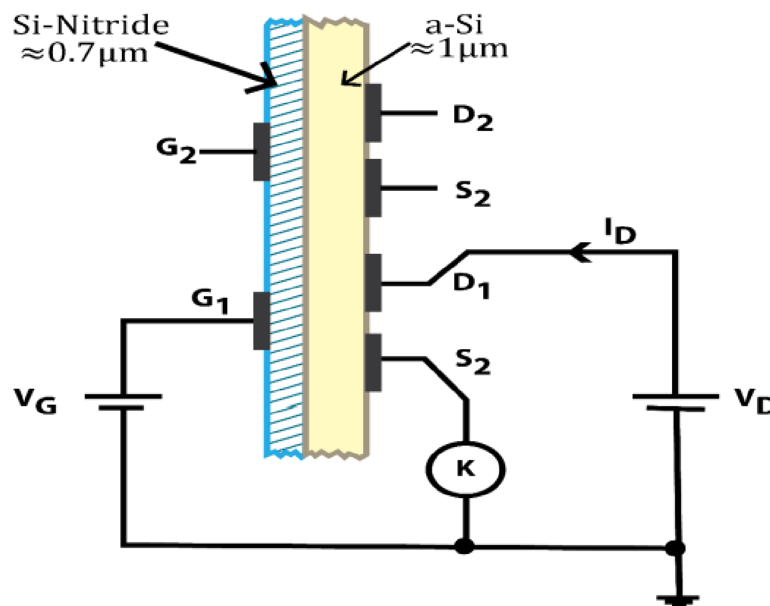

Figure I-4 First TFT with a-Si like active layer

The high concentration of defects in a-Si makes its TFTs having poor characteristics but it is promising for application on LCD. The hydrogenated amorphous silicon (a-Si:H), in contrast to pure amorphous silicon (a-Si) has higher mobility and is stable in the atmosphere [12]. Those properties make a-Si:H the material for next decade in TFT application. a-Si:H is perfectly suitable for the application of TFTs as switching elements in LCDs, since it has low cost, good reproducibility and uniformity in large areas and on/off exceeding 10^6a, threshold voltage (V_{th}) of $< 3\ V$, and a subthreshold slope (S) of $< 0.5\ V/dec$ [13]. In 1982, both IBM group [14] and Nishimura et al [15] using Polycrystalline silicon (Poly-Si) as channel on TFTs in LCD. Poly-Si TFTs have field-effect mobility (μ_{FE}) hundreds of times higher than that of a-Si TFTs and exhibit great performance. The development of poly-Si TFTs for displays started with the realization of

low temperature poly-Si TFTs, based on molecular beam epitaxy (MBE) technology by Matsui and co-worker [16]. They fabricated TFTs on a glass substrate at a low temperature of below 610 °C.

I.2.3 Organic TFT

Conventional electronics is based on inorganic semiconductors such as germanium, silicon or Gallium arsenide. Organic materials like plastics are usually associated with electrical insulation. In the 1960s it was discovered that some organic materials can carry an electric current [17], [18]. In the beginning, Organic conductive materials were applied in xerographic devices (photocopiers) [19]. The work Shirakawa and all stimulated the research in organic when they found that the electrical conductivity of polymer semiconductor could be higher and closer to a-Si [20]. The first application of organic material on TFT was reported in the literature in 1983 [21]. Figure I-5 shows the structure of an organic TFT.

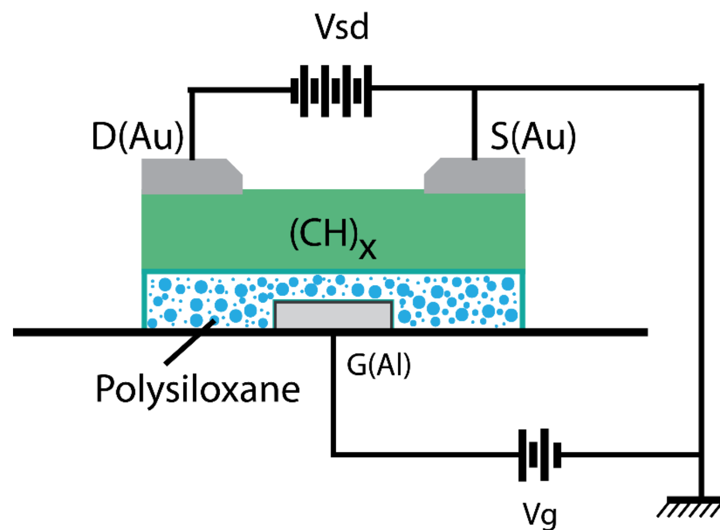

Figure I-5 the first Organic thin films transistor

The active organic material in the middle is called organic semiconductor. An organic semiconductor consists of aggregates of organic molecules bound by weak van der Waals forces. These molecules contain loosely bound π-electrons that are ultimately responsible for electrical

conduction [22]. There are several organic materials used as the active semiconducting layer, including small molecules such as rebrene, tetracene, pentacene, diindenoperylene, perylenediimides, tetracyanoquinodimethane (TCNQ), and polymers such as polythiophenes (especially poly 3- hexylthiophene (P3HT)), polyfluorene, polydiacetylene, poly 2,5-thienylene vinylene, poly p-phenylene (PPV). Organic TFTs made of small organic molecules, such as pentacene, have better characteristics than those made of large molecule polymers [23]. Organic materials can be n-type or p-type. The properties of organic semiconductors in general, can be tuned by changing their chemical composition. Mechanical properties; suitable for flexible applications; can be adjusted. Polymer can be made strong; flexible, lightweight. Organic material can be processed at low temperatures, typically below 150°C, compatible with most type of substrates and can use cheap and large-scale methods like inkjet printing, spin coating, roll-to-roll to fabricate organic electronic circuits. This later make the cost of production lower [24]. The challenge for researcher in the field of organic semiconductors is to increase the low mobilities, solve the major rapid oxidation in the air. The stability of the organic TFT in the atmosphere is another common concern, the metallic electrodes is another problem due to low melting point of organic materials. Thin films of organic semiconductors are not heat durable, organic TFT have high threshold voltage V_{th} of about $15\ V$, For that all these reasons, commercial applications of organic TFTs is very limited [25].

I.2.4 Transparent Oxide Semiconductors TFT

Transparent conducting oxide (TCOs) is an unusual class of materials possessing two physical properties: high optical transparency (more than 80%) in the visible region. high electrical conductivity (about $10^3 \Omega^{-1} cm^{-1}$or more). The first is due to the material large energy band gap of about $3.0\ eV$ while the last is because of high concentration of electrical carries (electron or hole) about $10^{19} cm^{-3}$, with a sufficiently large mobilities $> \sim 1\ cm^2 V^{-1} S^{-1}$. The TCO are considered to be good conductors compared to semiconductors, while they are actually very poor conductors compared to metals. They are also called transparent semiconducting oxides TSO [26], [27]. The properties and stability of TSO on atmosphere attracted several academic and industrial groups. The first application of TFT in which TSO is used as a channel layer was in 1964, when

SnO_2 is evaporated on a glass substrate with aluminum source-drain and gate electrodes, Al_2O_3 was used as a gate dielectric. Figure I-6 shows the SnO_2 TFT structure[28]. Later on; ZnO was used as TSO channel lyre for TFT [29].

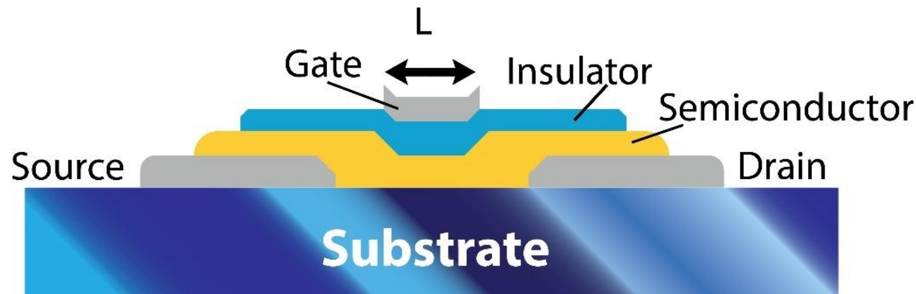

Figure I-6. The first TFT based on SnO_2

The first generation of TFTs based on TSO had very poor output characteristics. In 2001 the work of Ohya et al achieved good I_{on}value but the problem was with saturation [30] . The revolution of transparent transistors based on oxide semiconductors was in 2003 when Hoffman et al, Carcia et al and Masuda et al [31]–[33] obtained results for ZnO TFT comparable or even superior to a-Si:H and organic TFTs. The advantage of ZnO is the good properties obtainable by non-vacuum methods and on low temperature or room temperature process [34]–[36].

The first modeling and simulation of polycrystalline ZnO thin films transistor helped in discovering large properties of the TSO polycrystalline structure[37]. There are other TSO used as an active layer in TFT such as In_2O_3 and SnO_2 [38], [39]. ZnO_2 got eventually the upper hand due to its abundance and low cost. Binary polycrystalline n-type TSO like ZnO and SnO_2 are sensitive to environmental atmospheres because of adsorption of oxygen species on the surface/grain boundaries (GBs) which act as traps for electrons. Long term stability plus high cost for large scale production are a big obstacle for industry and commercialization. Issues like degradation in mobility and stability are probably due to GB issues.

In 2003 Nomura et al introduced a new type of TSO by using complex $InGaO_3(ZnO)_5$ or IGZO single crystalline semiconductor layer as channel in TFT [40]. This layer was epitaxially grown on an yttria stabilized zirconia substrate and has achieved a spectacular result: turn on voltage of $-0.5\ V$, On/Off ratio of 10^6 and effective mobility about 80 $cm^2V^{-1}s^{-1}$. To attain this

level of performance high temperature of about $1400°C$ was required. It turns out that this publication attracted huge attention and opened new field of research on multicomponent oxide semiconductors. One year later Nomura et al made history, when they obtained high performance of TFT based on amorphous IGZO, depositing near room temperatures by pulsed laser deposition (PLD) on flexible substrates [41]. Figure I-7 shows $I_{DS} - V_{DS}$ curves and structure of a-IGZO TFT on flexible substrate.

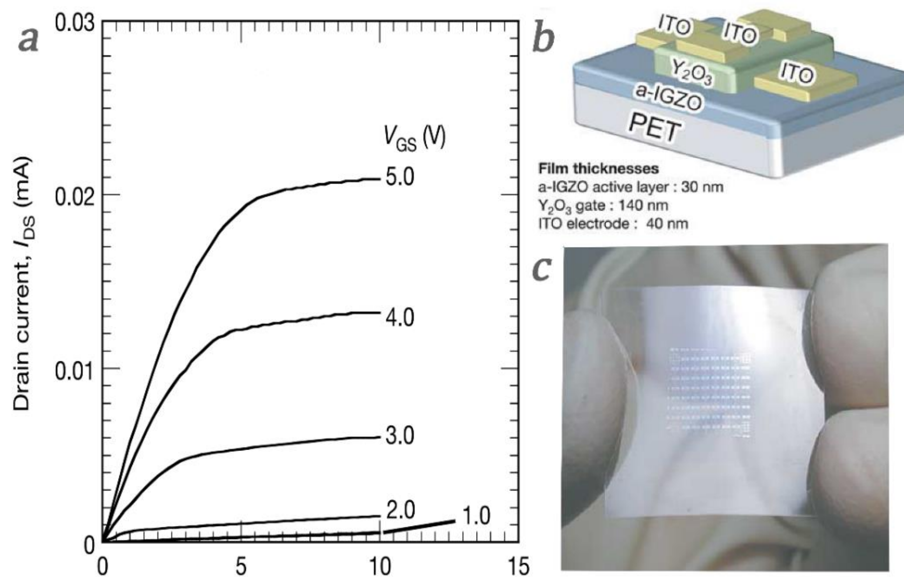

Figure I-7. The first a-IGZO deposited at room temperature by Nomura et al. a) $I_{DS} - V_{DS}$ curve b) structure of a-IGZO TFT c) the flexible substrate

Even a-IGZO showed lower performance compared with single crystalline TFTs, but a-IGZO TFT still having good performance with $\mu_{sat} = 9\, cm^2V^{-1}s^{-1}$, $V_T \approx 1 - 2\, V$ and $^{On}/_{off} \approx 10^3$. These results are superior than $a - Si{:}H$ ororganic semiconductors. This proved the low sensitivity of multicomponent oxide to structural disorder; in other word the multicomponent oxides are the future material for TFT application. Nowadays a-IGZO has receive great importance in research and development to achieve high performance with non-vacuum methods, lower the cost of large areas devices and long term of stability.

I.3 Physics and modeling TFTs

Thin film transistors (TFT) is field effect device, the heart of field effect devices is contact metal-insulator-semiconductor MIS, the MIS device is most useful devices to describe semiconductor surface. In this section we concentrate on MIS system to understand the physics phenomena which happen on ideal MIS. The Figure I-8 presents structure of simple MIS device where The Insulator between metal and semiconductor and V is applied voltage. this device show similarity with capacitor for that it is also known MIS capacitor.

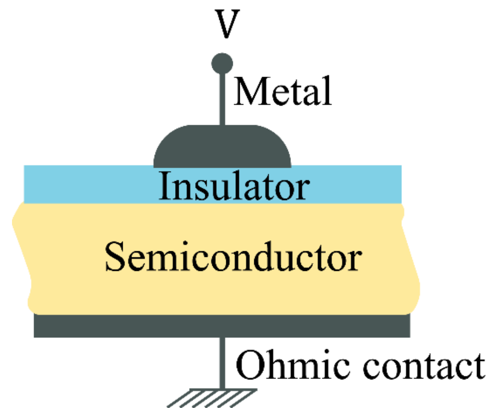

Figure I-8 Metal Insulator Semiconductor system

I.3.1 Ideal MIS Capacitor structure

Figure I-9 shows the band diagram of an ideal MIS capacitor, on a n-type substrate, in which the Fermi levels in the metal and in the semiconductor perfectly align, such that there is no induced band bending within the structure. In the analyses below, the following conventions will be used: The Fermi potential, V_F, will be measured from the bulk intrinsic level, E_i, and will be taken as positive below E_i and negative about it. Similarly, the band bending, V_s, will be measured from the bulk intrinsic level, and the polarity convention will be the same as used for V_F.

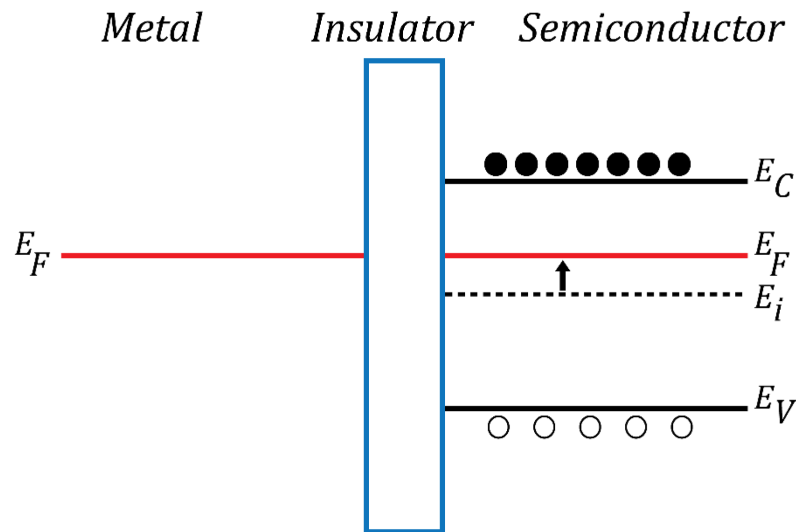

Figure I-9 Energy-band diagrams of ideal MIS capacitors at equilibrium (V = 0)

When a positive charge, Q_G, is placed on the metal gate, it will induce an equal and opposite negative charge in the semiconductor, Q_s, and this negative charge will consist of an increase in the electron density, due to an increase in the free electrons density. This is associated with bending downwards by an amount $+V_s$. In this case, the surface is said to be *accumulated* Figure I-10 (a) shows the accumulated state. With a negative bias applied to gate, there is an increase in the positive charge in the semiconductor and a decrease in the free electrons density, thereby, leaving behind immobile, ionized donor centers, N_d. In order to accommodate these charges in free carries density, the bands within the semiconductor will have to bend upwards near its surface, as shown Figure I-10 (b). It will also be seen that the negative charge on the gate results from a negative bias being applied to the gate relative to the semiconductor. Following the convention discussed above, the Fermi level in the metal is moved upwards in response to a negative gate bias, V_G, and the semiconductor surface potential is $-V_s$. The situation shown in the diagram is for a small negative compared with N_d, and surface is said *depleted* (of free electron). For a lager positive gate bias, the situation shown in Figure I-10 (c) occurs. In this case, there is a corresponding increase in the band bending, V_s , and the free hole concentration at the surface is larger than N_d. The surface is now said to be *inverted*. Between these two situations, when the band bending, $V_s = V_F$, the surface

will be intrinsic, and $n_s = p_s = n_i$. Further negative band bending beyond this point will lead to $n_s < p_s$.

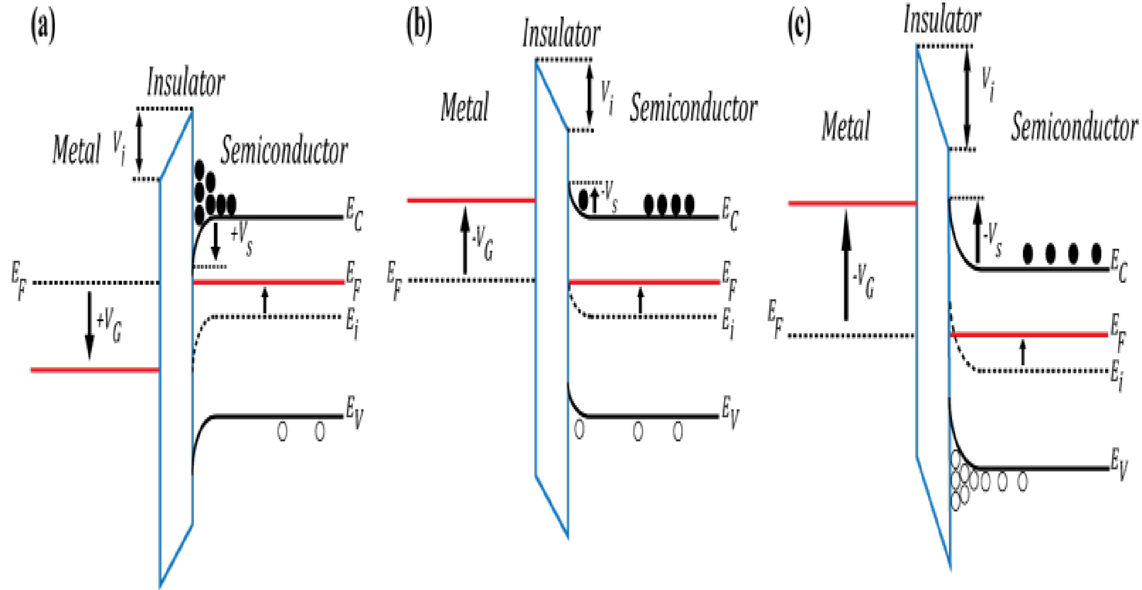

Figure I-10 Energy-band diagrams for ideal MIS capacitors under different bias conditions: (a) accumulation, (b) depletion, and (c) inversion. The semiconductor substrate is n-type.

With a p-type substrate, the opposite situation occurs. Negative bias leads to accumulation, and positive bias causes the surface depleted/ inverted. To find the relationship between V_s and Q_s and V_G, it is necessary to solve Poisson's equation, thus

$$\frac{d^2V}{dx^2} = -\frac{q\rho(x)}{\varepsilon_0\varepsilon_s} \quad \text{I-1}$$

ε_0 is the vacuum permittivity, ε_s is the semiconductor, dielectric constant.(x) is the space charge density, given by:

$$\rho(x) = p(x) - n(x) + N_d \quad \text{I-2}$$

The free carrier densities are defined by the intrinsic carrier concentration, n_i, and the separation of the Fermi level from the intrinsic level, i.e.:

$$p(x) = n_i exp\left(\frac{q(V_F - V)}{kT}\right) \quad \text{I-3}$$

$$n(x) = n_i exp\left(\frac{-q(V-V_F)}{kT}\right) \qquad I\text{-}4$$

$$p(x) - n(x) = 2n_i sh\left(q\frac{V_F - V}{kT}\right) \qquad I\text{-}5$$

Where T is the temperature, and k is Boltzmann's constant. At the surface, $V = V_s$, and the in the bulk, where $V = 0$:

$$\begin{cases} p_0 = n_i exp\left(\frac{qV_F}{kT}\right) \\ n_0 = n_i exp\left(\frac{-qV_F}{kT}\right) \end{cases}$$

From charge neutrality,

$$n_0 - p_0 = N_d = 2n_i sh\left(q\frac{V_F}{kT}\right) \qquad I\text{-}6$$

$$\frac{d^2V}{dx^2} = -\frac{2n_i q}{\varepsilon_0\varepsilon_s}\left\{sh\left(\frac{q(V_F-V}{kT}\right) - sh\left(\frac{qV_F}{kT}\right)\right\} \qquad I\text{-}7$$

Using $\frac{d^2V}{dx^2} = \frac{1}{2}\frac{d}{dV}\left(\frac{dV}{dx}\right)^2$, and integrating equation I-7 from the bulk ($V = 0$, and $\frac{dV}{dx} = 0$) to the surface($V = V_s$, and $\frac{dV}{dx} = -F_s$):

$$\left(\frac{dV}{dx}\right)^2_{V=Vs} \equiv F_s^2 = \frac{4n_i q}{\varepsilon_0\varepsilon_s}\left\{\frac{kT}{q}ch\left(\frac{q(V_F-V_s)}{kT}\right) - \frac{kT}{q}ch\left(\frac{qV_F}{kT}\right) + V_s sh\left(\frac{qV_F}{kT}\right)\right\} \qquad I\text{-}8$$

From Gauss' Law, the surface field,F_s, is related to the total areal charge, Q_s, contained within the surface by:

$$Q_s = -\varepsilon_0\varepsilon_s F_s \qquad I\text{-}9$$

Hence, the relationship between Q_s and V_s is given by

$$Q_s = \pm\sqrt{4n_i q\varepsilon_0\varepsilon_s}G(V_s, V_F) \qquad I\text{-}10$$

Where $G(V_s, V_F)$ is given by:

$$G(V_s, V_F) = \mp\sqrt{\left\{\frac{kT}{q}ch\left(\frac{q(V_F-V_s}{kT}\right) - \frac{kT}{q}ch\left(\frac{qV_F}{kT}\right) + V_s sh\left(\frac{qV_F}{kT}\right)\right\}} \qquad I\text{-}11$$

Given the positive and negative values of $Q_s$in equation *I-10*, the appropriate sings of V_s,$F_s$and Q_s are given in Table I-1, and the correct value of Q_s is given by:

$$Q = -\frac{V_s}{|V_s|}\,|Q_s| \qquad \textit{I-12}$$

Table I-1: Polarity relationship between band bending, surface field and space charge in an MIS

V_s	F_s	Q_s	**Free carrier conditions**
-Ve	-Ve	+Ve	Reduction of electrons and/or increase of hole
+Ve	+Ve	-Ve	Reduction of hole and/or increase of electrons

When the volume concentration of free electrons at the surface, n_s is equal to the volume concentration of acceptors N_a ($V_s = V_F$), the surface is intrinsic ($n_s = p_s = n_i$), and the band bending regime beyond this, and up to strong inversion, is referred as weak inversion ($p_s < n_s < N_a$).

In the depletion/inversion regime, the band bending V_s is positive, and for V_s and $V_F > KT/q$, i.e., more than KT from the flat band position, equation.10 can be simplified to

$$Q_s \cong -\sqrt{2q\varepsilon_0\varepsilon_s}\left\{n_i\frac{kT}{q}\,exp\left(\frac{q(V_s-V_F)}{KT}\right)+N_aV_s\right\}^{0.5} \qquad \textit{I-13}$$

The first term in brackets relates to the free electron concentration and the second term to the ionized acceptor space charge density. When the ionized acceptor space charge dominates equation 13 can be further reduced to

$$Q_s \cong -\sqrt{2q\varepsilon_0\varepsilon_sN_aV_s}\;\equiv Q_b \qquad \textit{I-14}$$

Where Q_b is the areal acceptor space charge denꞓsity. Equation I.14 is the same as directly calculated from Poisson's equation using the depletion approximation, i.e. from

$$\frac{d^2V}{dx^2} = \frac{qN_a}{\varepsilon_0\varepsilon_s} \qquad \textit{I-15}$$

And integrating this with respect to x or if equation I.15 is integrated with respect to V, then:

$$Q_s = -qN_ax_d \qquad \textit{I-16}$$

Where x_d is the width of the space charge depletion region at V_s. At inversion when $V_s = 2V_F$, further increase in the band bending causes such large increase in Q_s, due to exponentially increasing free electron density. To a first approximation, the fixed space charge can be regarded as having reached a limiting maximum value, Q_{max}. This can be obtained by substituting $V_s = 2V_F$ into equation I.14

$$Q_{bmax} = -\sqrt{2q\varepsilon_0\varepsilon_s N_a 2V_F} \qquad \textit{I-17}$$

And from equation I.16

$$Q_{bmax} = -qN_a x_{dmax} \qquad \textit{I-18}$$

Where x_{dmax} is the maximum width of the depletion region, and, from equation I-18 and I-19, x_{dmax} is given by:

$$x_{dmax} = \sqrt{\frac{2\varepsilon_s\varepsilon_s 2V_F}{qN_a}} \qquad \textit{I-19}$$

Q_s in equation I.13 can be represented by the sum:

$$Q_s = Q_n + Q_b \qquad \textit{I-20}$$

Where Q_b is the extended depletion layer charge, and Q_n is the areal density of inversion layer electron.

I.3.2 Gate bias and threshold voltage

Back to Figure I-10, the gate voltage, V_G is dropped partially across the dielectric, V_i and partially across the semiconductors, V_s so that:

$$V_G = V_i + V_s \qquad \textit{I-21}$$

And for charge neutrally, the charge on the gate, Q_G , equals the charge in the semiconductors Q_s and

$$Q_G = \varepsilon_0\varepsilon_i F_i = \varepsilon_0\varepsilon_i {}^{V_i}/_{d_i} = C_i V_i = -Q_s \qquad \textit{I-22}$$

Where F_i is the field in the gate dielectric, and C_i is the capacitance/unit area of the gate dielectric. Hence

$$V_G = V_s - {}^{Q_s}/_{C_i} \qquad \textit{I-23}$$

Equation I.23 can be used to relate the voltage on the gate of an MIS capacitor to the induced charge density in the semiconductor, Q_s and to the associated band bending, V_s. It can also be used to calculate the threshold voltage, V_{th} of the structure i.e the gate voltage necessary to induce band bending of $2V_F$ at the semiconductor surface:

$$V_{th} = 2V_F + \frac{\sqrt{2q\varepsilon_0\varepsilon_i N_a 2V_F}}{C_i} \qquad \textit{I-24}$$

For the real behavior the work function influence and fixed charge in insulators and charge in the interface have to be taken inti account to properly establish the threshold formula

$$V_{th} = 2V_F + \frac{\sqrt{2q\varepsilon_0\varepsilon_i N_a 2V_F}}{C_i} + V_{FB} + \frac{Q_{SS}(V_S=2V_F)}{C_i} \qquad \textit{I-25}$$

$Q_{ss}$is charge in semiconductor surface. A at inversion is given by:

$$Q_{ss}(A) = qN_{SS}q(2V_F - V_F) = qN_{ss}qV_F \qquad \textit{I-26}$$

Where V_{FB} equal

$$V_{FB} = \Phi_{MS} - \frac{Q_{ieff}}{C_i} - Q_{ss}(V_s = 0)/C_i \qquad \textit{I-27}$$

Φ_{MS} is metal–semiconductor work function difference. Q_{ieff} is effective charge. will be determined, as though it were located at the dielectric/semiconductor interface.

I.3.3 MOSFET operation

Figure I-11 shows a schematic diagram of an n-channel MOSFET, in which there are n^+ doped source and drain regions, separated by a distance L, which defines the channel length. The width of the channel W, is in the z-direction (which is perpendicular to the page). Surface band bending, perpendicular to the Si/SiO_2 interface, is in the x-direction. In the on state, positive biases V_D and V_G are applied to the drain and gate contacts, respectively, with respect to the ground source contact. There is a fourth contact in MOSFET, which is the p-type substrate connection, which is

under reverse bias. For TFT, this connection to the device layer will generally not be available. The device to be described is the long channel model, in which the field along the channel (control of the on current) is much smaller than the vertical field (determining the inversion layer concentration), and the two are effectively decoupled. This means that 2D phenomena is to be considered. The band bending and energy level conventions are those used in MOS.

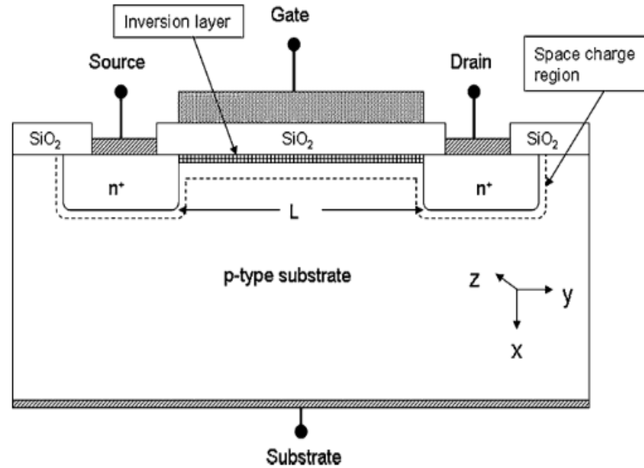

Figure I-11. 2 D illustration cross section of a MOSFET

The first situation shown in the Figure I-12.a , in which there is an inversion layer induced by the gate bias, V_G (larger than V_T), and at zero drain bias, the inversion layer will be uniform along the channel. The real charge densities within an inverted surface can be represented by the free electron inversion charge density, Q_n and the underlying ionized acceptor space charge density, Q_b where Q_n, Q_b and V_T are given by: $Q_n = C_i(V_G - V_T)$, $Q_b = qN_a x_{damx} = \sqrt{(2q\varepsilon_0\varepsilon_s N_a 2V_F)}$; $V_T = 2V_F + \sqrt{(2q\varepsilon_0\varepsilon_s N_a 2V_F)}/C_i$

Positive bias, $+V_D$ applied to the drain contact will reverse the n^+ drain region with respect the p-type substrate, and the current flow between the two is limited to the leakage current of the junction.

When the drain bias, V_D is low (i.e less than $V_G - V_T$), then V_D will be uniformly dropped along the channel inversion layer, resulting in both a constant field V_D/L and the flow an ohmic electron current, I_d between the source and drain contacts. This is defined as the linear regime of

device behavior. As V_D is increased, the ohmic channel current increases, and eventually, V_D reaches a value where, is still less than $V_G - V_T$. As this happens, the potential at the drain end the channel needs to be considered when computing the inversion charge density along the channel. For instance, at the drain end of the channel, the voltage drop across the oxide between the inversion layer and the gate electrode is now $V_G - V_T - V_D$, while it remains at $V_G - V_T$ at the source end to maintain current continuity. There will be a corresponding field redistribution along the channel, it increases more at the drain than the source as V_{DS} is increased. The current now no longer increase linearly with V_D, but becomes sub-linear. This situation is shown in Figure I.12b. In addition, in order to maintain charge neutrality between the charge on gate, Q_G and the charge in the semiconductor, the reduction in Q_n will be balanced by an increase in Q_b such that the thickness of the ionized acceptor space charge layer increases beyond the thermal equilibrium value of x_{dmax} (equation 19). This is shown qualitatively, in Figure I.12.b. Hence, for the depletion width to increase beyond this value, the amount of band bending has to increase beyond $2V_F + V_D$ at the drain. The qualitative changes in the charge distribution and the band bending, is at the source and drain ends of the channel. The bias at the drain results in a non-thermal equilibrium situation, with the thermal equilibrium Fermi level splitting in separate hole and electron quasi Fermi levels, E_{Fp} and E_{Fn},respectively which are separated by V_D. Hence, this diagram shows physically why the band bending, V_s, must increase to $2V_F + V_D$ at drain: it is to bring the intrinsic level at the surface to qV_F below the electron quasi-Fermi level at the drain. This is the condition required to invert the p-type surface of a reverse-biased gated $n^+ - p$ diode. This is the direct analogue of the thermal equilibrium situation, in which inversion occurs when the intrinsic level is qV_F below the equilibrium Fermi level.

Finally, as shown in Figure I-12.c, when $V_D = V_G - V_T$, Q_n is reduced to zero at the drain and channel is *pinched-off*. However, as all electrons arriving at the edge of the drain space charge region are swept through into the drain, this does not pinch-off the current, but it saturates, and the device operation moves into the *saturation regime.* The voltage at which this happen is the *saturation voltage*, V_{Dsat}. The current saturation occurs because, in principle, the maximum possible potential difference, V_{Dsat}, has been dropped along the channel, and the pinch-off voltage remains at V_{Dsat} even when V_D is increased. However, in reality, as V_D is increased the drain space charge region grows and the pinch-off point moves towards the source. Hence, even though the

total voltage drop along the channel remains at V_{Dsat}, the effective channel length shortens, and the mean channel field increases. This is show in Figure I.12d and this increase in field leads to a corresponding increase in the saturation current. Since pinch-off occurs at $V_D = V_{Dsat} = V_G - V_T$, increasing V_G leads to a corresponding increase in V_{Dsat}. This makes the saturation current to increase as $(V_G - V_T)^2$, due to the correlation of V_{Dsat} with V_G.

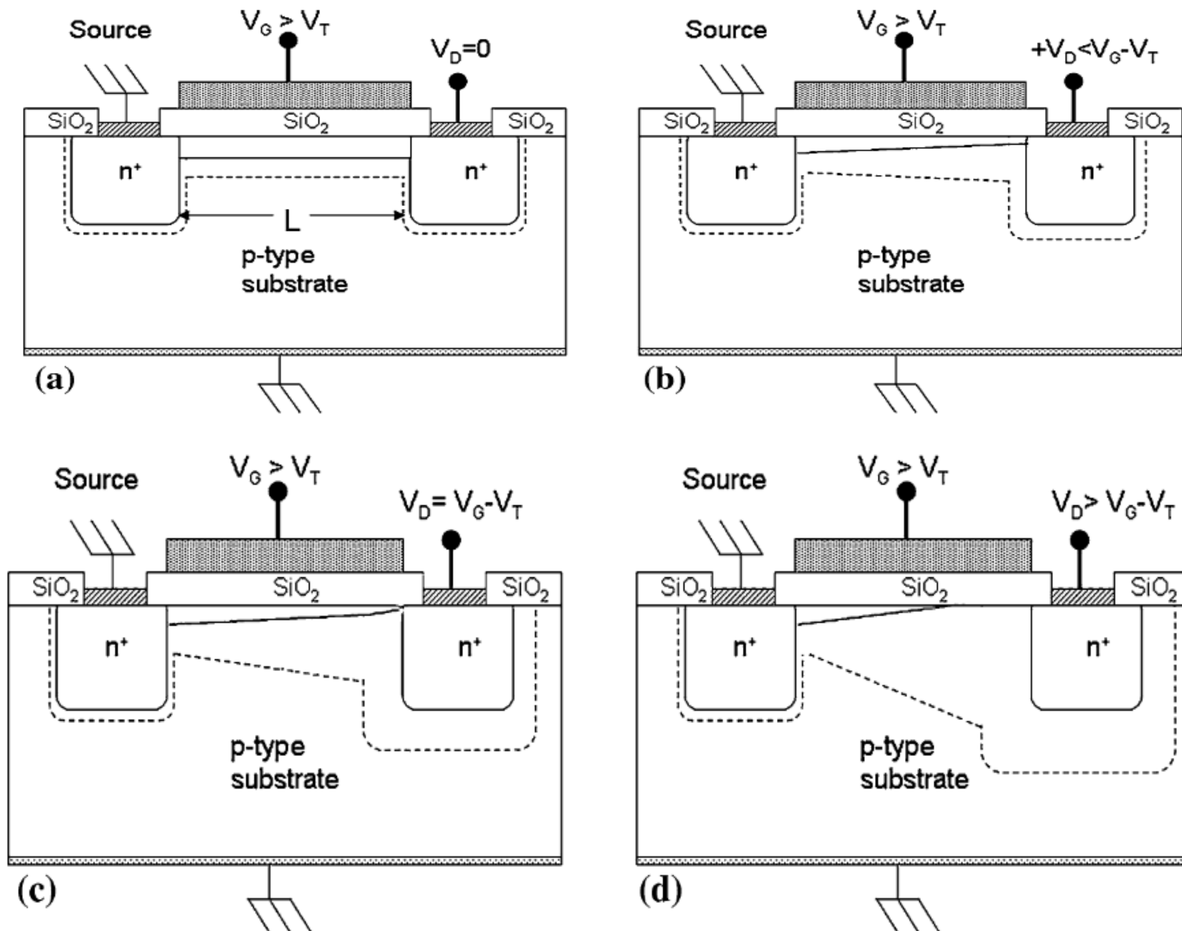

Figure I-12 Cross-section of MOSFET, in the on-state, for different values of drain bias V_D: a) $V_D = 0$, b) $V_D < V_G - V_T$, c) at pinch-off, with $V_D = V_G - V_T = V_{D(sat)}$, and d) $V_D > V_{D(sat)}$ showing channel shortening.

The MOSFET output characteristics in Figure I.13 illustrate the key features described above: in particular, the linear and saturation regimes, the increasing values of the saturation voltage, V_{Dsat} , with increasing V_G.

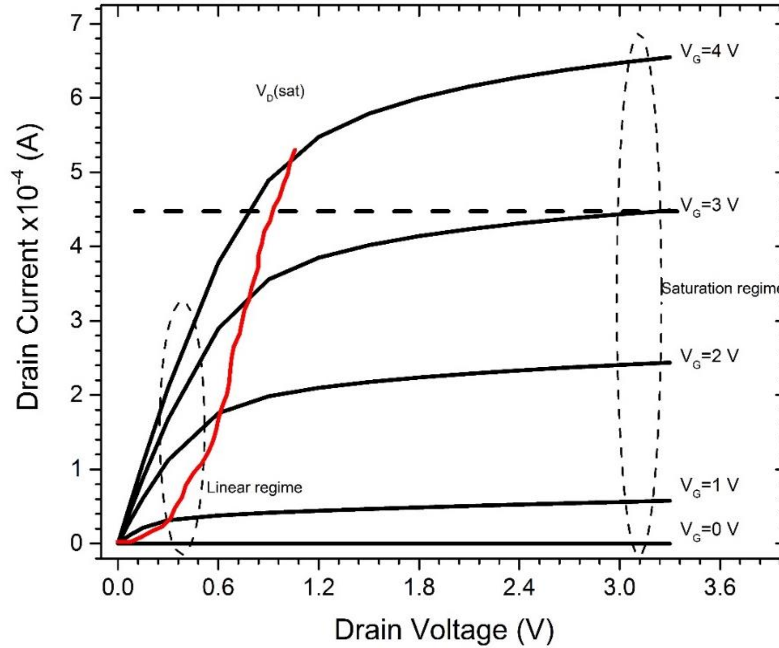

Figure I.I-13. Measured MOSFET output characteristics showing the linear and saturation operating regimes.

I.3.4 Current-Voltage modulation

As shown the Figure I.12 b-d, the current density J_D at any point x, y in the channel given by:

$$J_D = \sigma_n(x, y)F(y) \qquad \text{I-28}$$

Where y is the direction of current flow, x is the direction perpendicular to the Si/SiO_2interface, σ_n is the local electron conductivity, and F is the local field in the direction of current flow. The conductivity, σ_n is given by:

$$\sigma_n(x, y) = q\mu_n n(x, y) \qquad \text{I-29}$$

The current $I_d(y)$ at a position y is given by the integration the electron density, n over the depth of the channel and across the width the channel W

$$I_d(y) = W \int_0^{x_i} \sigma_n(x, y)F(y) = -W \int_0^{x_i} q\mu_n n(x, y) \frac{dV(y)}{dy} dx \qquad \text{I-30}$$

$$I_d = -Wq\mu_n \frac{dV(y)}{dy} \int_0^{x_i} (x, y)dx \qquad \textit{I-31}$$

Where it is assumed that the electron mobility is independent of the field in both the x and y directions and $V(y)$ is the potential in the channel at a point y. For an inverted surface the areal charge in the inversion layer can represented by Q_n where Q_n is the integral of the volume electron concentration through the depth of the channel

$$Q_n(y) = q \int_0^{x_i} n(x, y)dx \qquad \textit{I-32}$$

Q_n is also related to gate bias V_G by:

$$Q_n(y) = -C_i[V_G - V_T - V(y)] \qquad \textit{I-33}$$

By replacing the Q_n formula in equation 34

$$I_d = -\mu_n W \frac{dV}{dy} Q_n(y) = \mu_n W \frac{dV}{dy} C_i[V_G - V_T - V(y)] \qquad \textit{I-34}$$

Integrating y along the channel from 0 to L and V(y) from 0 to V_D

$$\int_0^L I_d d_y = \mu_n W C_i \int_0^{V_D} \{V_G - V_T - V(y)\}dv \qquad \textit{I-35}$$

For current continuity I_d is independent of position within the channel, hence:

$$I_d = \frac{\mu_n W C_i}{L} \{(V_G - V_T)V_D - 0.5V_D^2\} \qquad \textit{I-36}$$

This is the classical, simplified MOSFET equation, which is widely used to interpret TFT behavior

Linear Regime

For $V_D \ll V_G - V_T$ equation I.36 reduces to

$$I_d = \frac{\mu_n W C_i (V_G - V_T) V_D}{L} \qquad \textit{I-37}$$

This equation describes the current-voltage characteristics in the linear regime.

Saturation Regime

For $V_D\, V_G - V_T = V_{Dsat}$ the current saturation at I_{dsat} and equation 35 reduces to:

$$I_{dsat} = \frac{\mu_n W C_i (V_G - V_T)^2}{2L} \equiv \frac{\mu_n W C_i V_{Dsat}^2}{2L} \qquad \textit{I-38}$$

Hence, in saturation the current increases quadratically with $V_G - V_T$ because the inversion charge increase by this amount, as does the maximum potential drop along the channel.

I.4 Thin film Transistor

Thin film transistor is a kind of MOSFET. That is it has a similar structure to MOSFET. The difference between TFT and MOSFET is that the active layer can be any type of semiconductor and the active layer is deposited as a thin film on a different material substrate (glass for example) as shown in Figure I.14. Because the semiconductor layer is formed by deposition, the material has more defects and imperfections than in single crystalline semiconductor. The transport processes become complicated in TFT. In a TFT, the leakage current is always higher due to defects, the current is limited resulting in a lower mobility. To improve device performance, reproducibility, and reliability, the bulk and interface trap densities must be reduced to reasonable levels.

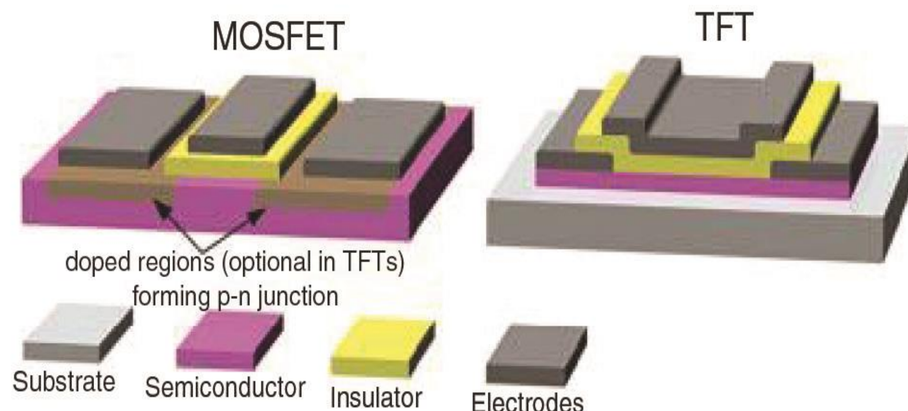

Figure I-14 Schematics showing show the difference between MOSFET and TFT

In addition, MOSFETs have p-n junctions at the source-drain regions, which are absent in TFTs. This is another important difference in device operation: even if both TFTs and MOSFETs rely on the field effect to modulate the conductance of the semiconductor close to its interface with

the dielectric. In TFTs this is achieved by an accumulation layer, while in MOSFETs an inversion region has to be formed close to that interface, i.e., a n-type conductive layer is created in a p-type silicon substrate (inversion) [42].

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Chapter II

a-IGZO thin films transistors

II.1 Introduction

Transparent conductors are neither 100% optically transparent nor metallically conductive. Over recent years intense research has been carried on n-type transparent conducting and semiconducting oxides (TCOs and TSOs, respectively). From the band structure point of view, the combination of the two properties in the same material is contradictory a transparent material and an insulator which processes fully filled valence and empty conduction bands. While metallic conductivity appears when the Fermi level lies within a band with large density of states to provide high carrier concentration. Crystalline Zinc oxide and indium oxide have been two of the most commonly used binary compounds in transparent electronics. More recently, ternary and quaternary compounds such as indium-zinc oxide (IZO) or gallium-indium-zinc oxide (IGZO) have also started to be explored. IGZO is an amorphous oxide semiconductor (AOS) is an alternative of crystalline oxide semiconductor. Now it is expected to be most promising material for transparent electronics due to the opportunity to combine low processing temperatures, amorphous structures and remarkable optical and electrical performance. This interest is due to the properties of AOS, which make them well suited for channel materials of thin film transistors (TFTs). TFTs based on IGZO have wide application but the most important application is in next generation flat panel displays (FPDs) such as active matrix, electronic papers (e-papers) and flexible, large area electronic devices [1].

This chapter is dived to two parts. The first presents the properties of TCO and AOS in general and specifically those of IGZO. In addition, the deposition of a-IGZO thin films by sol gel and characterization methods will be discussed. In the second part the fabrication and characterization TFT are presented.

II.2 IGZO properties

The AOS a-IGZO material is composed from three binary oxide In_2O_3, Ga_2O_3 and ZnO. Binary oxide has crystalline phase but when mixed to form multi-component oxide, an amorphous phase is obtained as shown Figure II-1.a. In AOS multi-component each oxide affects the mobility as summarized in Figure II-1.b. As shown each fraction of the three oxide gives different properties. In_2O_3, increases the mobility and the free electron density, Ga_2O_3 makes the material more stable and enhances its amorphization while ZnO forms the matrix for the other oxides [2].

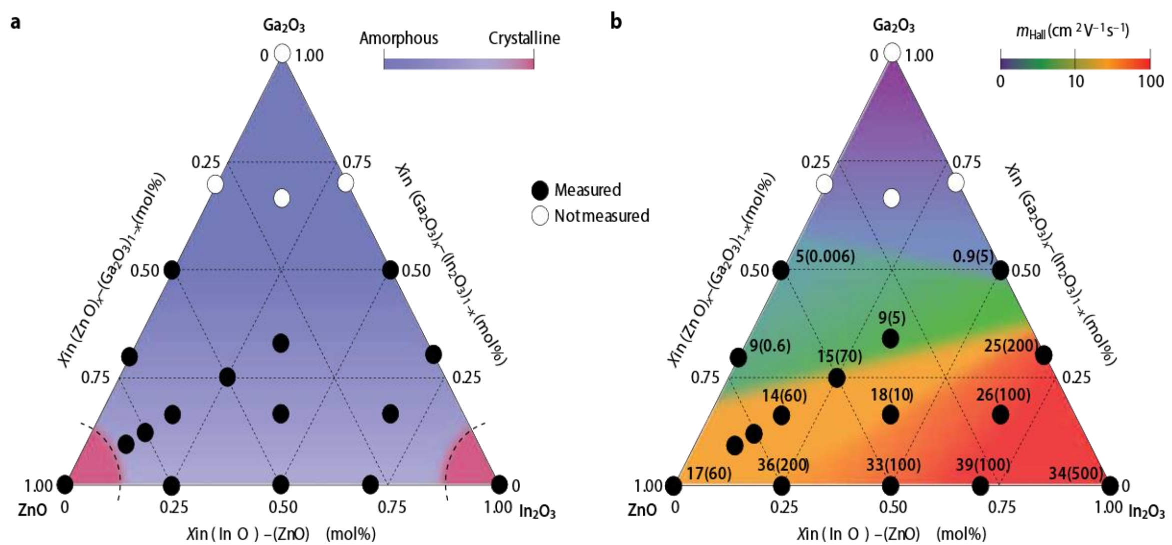


Figure II-1 (a) Amorphous formation and (b) electron transport properties In_2O_3, Ga_2O_3 thin films. The values in (b) denote the electron Hall mobility (cm^2V^{-1} s^{-1}) with density (10^{18} cm^{-3}) in parentheses [3].

II.2.1 Atomic structure

Figure II-2 shows the structure characterization by X-Ray Diffraction (XRD). In XRD result of IGZO films show any diffraction peaks assignable to crystalline phase. Those results can be used for determining the amorphous phase of IGZO. In general, mixing of two or more cation having different ionic charge and size is effective for enhancing the formation of an amorphous phase and destroy crystallization phase; this is the reason why AOSs are basically multi-component system [4].

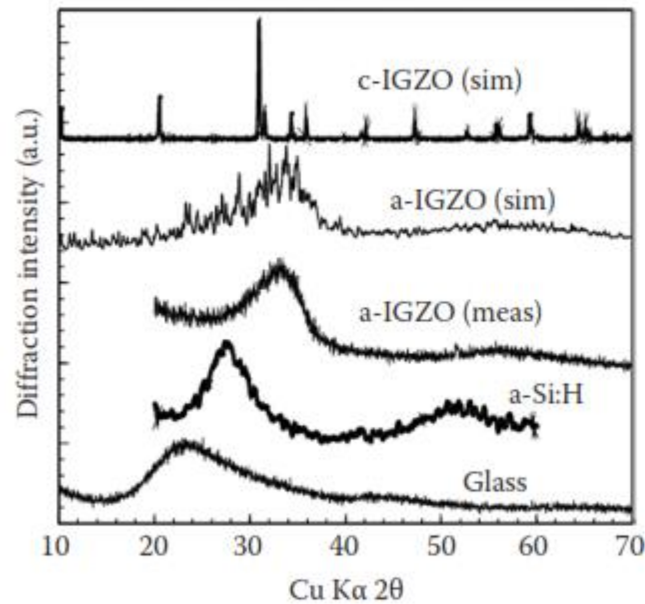


Figure II-2 XRD result[5]

II.2.2 Electronic structure of oxide

The difference between oxide semiconductors and conventional covalent semiconductors such as Si and GaAs can be understood from their electronic structures. This is important also for understanding the drawback and the advantage of oxides. This difference results in an important fact that it is easy to obtain good N-type electron conduction, but P-type hole conduction is difficult in oxide semiconductors; in fact, there have been a limited number of P-type oxides such as TCOs. Figure II-3 shows crystal structures of representative semiconductors, Si, GaAs, and ZnO, which are superimposed by iso-surfaces of wave functions $|\psi|^2$ of conduction band minimums (CBMs) and valence band maximums (VBMs).

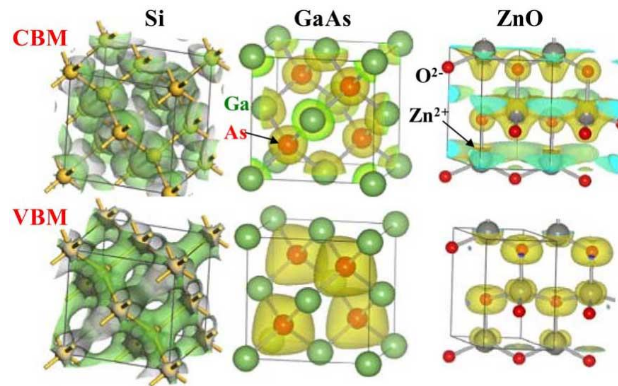


Figure II-3 Wave functions of representative semiconductors such as Si, GaAs and ZnO.

In silicon, the conduction band minimum (CBM) and valence band maximum (VBM) are made of anti-bonding ($sp^3\sigma^*$) and bonding ($sp^3\sigma$) states of Si sp orbitals, and its band gap is formed by the energy splitting of the $\sigma^* - \sigma$ levels (Figure II-4.a). By contrast, oxides have strong ionicity and charge transfer occurs from metal to oxygen atoms (Figure II-4.b), and the electronic structure is stabilized by the Madelung potential formed by these ions, raising the electronic levels in cations and lowering the levels in anions. Consequently, the CBM is primarily formed by the unoccupied s orbitals and the VBM of cations by fully occupied O 2p orbitals, as represented in Figure II-4.c [5].

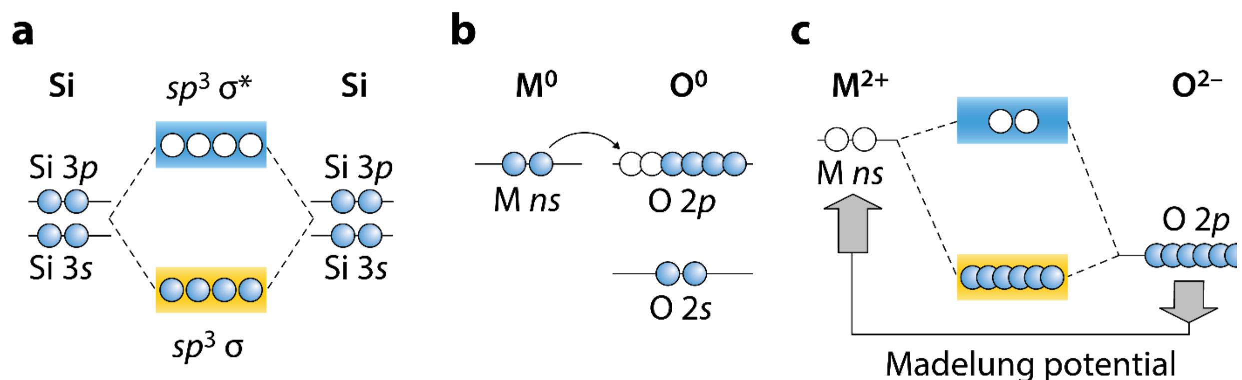


Figure II-4 Schematic electronic structures of silicon and ionic oxide semiconductors (a–c) Bandgap formation mechanisms in (a) covalent and (b,c) ionic semiconductors[3].

Different formation mechanisms of bandgaps in covalent (a) and ionic (b,c) semiconductors. (a) Bandgap of Si is formed of the energy splitting $\sigma^* - \sigma$ of levels. (b) Oxygen and metal (M) atoms are neutral in vacuum, but (c) ionized to O^{-2} and, e.g.M^{+2} respectively, when they come near due to the Madelung potential.

II.2.3 Band structure

There have been several works on the theoretical calculation of electronic structure and defects for IGZO. Those of c-IGZO and a-IGZO have been reported in Refs [6]–[9]. The pseudo-band structure of $\mathrm{a-InGaZnO_4}$ is shown in Figure II-5.b compared with of $\mathrm{c-InGaZnO_4}$ in Figure II-5.a. The band structure of c-Si and a-Si shown in Figure II-6.

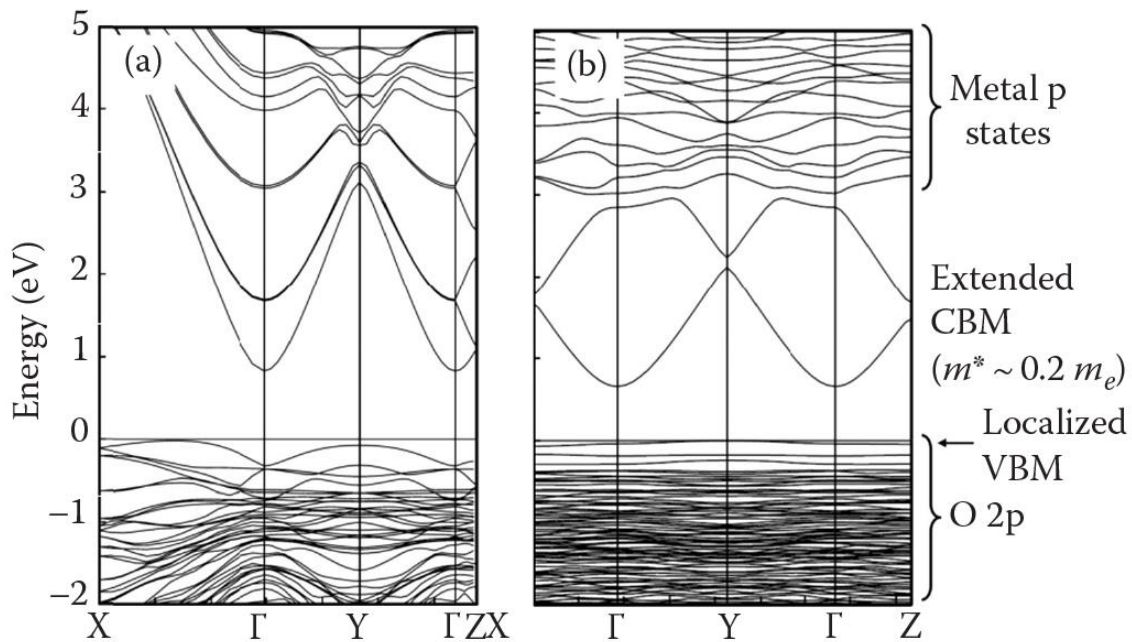


Figure II-5 (Pseudo-)band structures of (a) c-InGaZnO 4 and (b) a-InGaZnO4 [4].

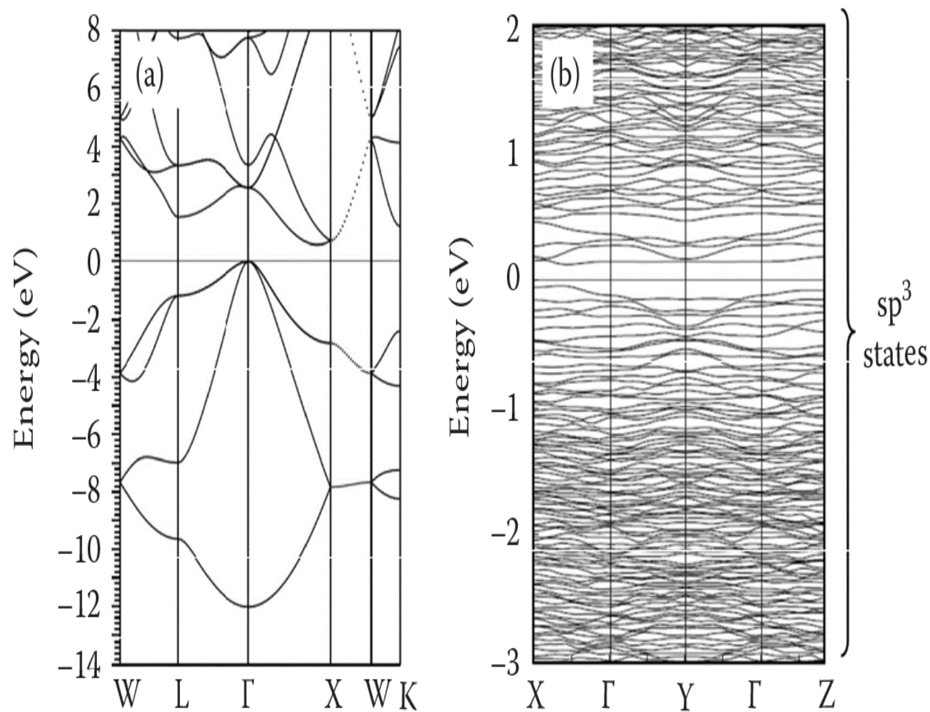


Figure II-6 (Pseudo-)band structures of (a) c-Si and (b) a-Si.

The term "pseudo-band structure" is used because an amorphous material does not have a periodic structure and the band theory is not applied in exact sense. The pseudo-periodic calculations are effective to find band dispersion and effective mass. The band structure show similarity between c-IGZO and a-IGZO. Definitely, the effective masses are $0.28m_e$ for c-IGZO and $0.30\ m_e$ for a-IGZO. For Si it is clear that all bands become almost flat in a-Si indicating that electrons and holes are strongly localized. Same thing is observed in IGZO. This implies that IGZO is insensitive to disordered amorphous structure but Si very sensitive to a disordered structure [4].

II.2.4 Origin large Electron mobility in AOS

It is supposed that the properties of amorphous semiconductors are greatly degraded compared with their corresponding crystalline phases, which is actually the case for silicon because intrinsic crystalline silicon exhibits an electron mobility of $1500\ cm^2V^{-1}s^{-1}$, which deteriorates to less than 2 $cm^2V^{-1}s^{-1}$ in a-Si. On other hand, AOSs exhibit large electron mobility

of greater than 10 $cm^2V^{-1}s^{-1}$ even in amorphous structures [5]. To understand this behavior, two cases are defined (1) covalent semiconductor and (2) ionic semiconductor. In case (1), the magnitude of the overlap between, the empty orbital of the neighboring atoms is very sensitive to the variation in bond angles and forms different energy electronic states at different position. As a result, rather deep localized states would be created at somewhat high concentrations and in that way the drift mobility would be largely degraded due to cattier scattering/trapping by defects. In contrast, the magnitude of the overlap in case (2) is different largely depending on the choice of metal if the spatial spread of the s orbital is larger than the inter-cation distance, the magnitude of the wave function overlaps is insensitive to the bond angle distribution and the s orbitals are isotropic in shape. As a consequence, it is anticipated that these ionic amorphous materials consisting of heavy post transition cations have large band dispersion, small carrier effective mass and large mobility comparable to those in the corresponding crystals. Thus, candidates for good TOS having large electron mobilities comparable to those of ions with an electronic configuration $(n-1)d^{10}ns^0$ where $n \geq 5$ [10].

Figure II-7 illustrates the comparison of orbitals in Si (Figure II-7.a and Figure II-7.b) and amorphous oxide semiconductor r(Figure II-7.c and d). Figure II-7.a and b show crystalline states while Figure II-7.b and d show amorphous states. From Figure II.3.a and b it may be understood intuitively degradation in electron mobility while we can notice the mobility less effected in AOS. Convectional amorphous semiconductors such as a-Si:H and a-Si show much deteriorated carrier transport properties than associated crystalline materials. This is because the chemical bonds in the covalent semiconductors are made of sp^3 or p orbitals that have strong spatial directivity. Therefore, the strained chemical bonds in amorphous structures from rather deep and high-density localized states below CBM and above VBM producing carrier trapping. By contrast, as CBMs of oxides are made of spherically spread s orbitals are not altered largely by disordered amorphous structures; therefore, electronic levels of CBM are insensitive to local strained bonds and electron transport is not largely affected. This is the reason why AOSs exhibit large electron mobilities even amorphous structures.

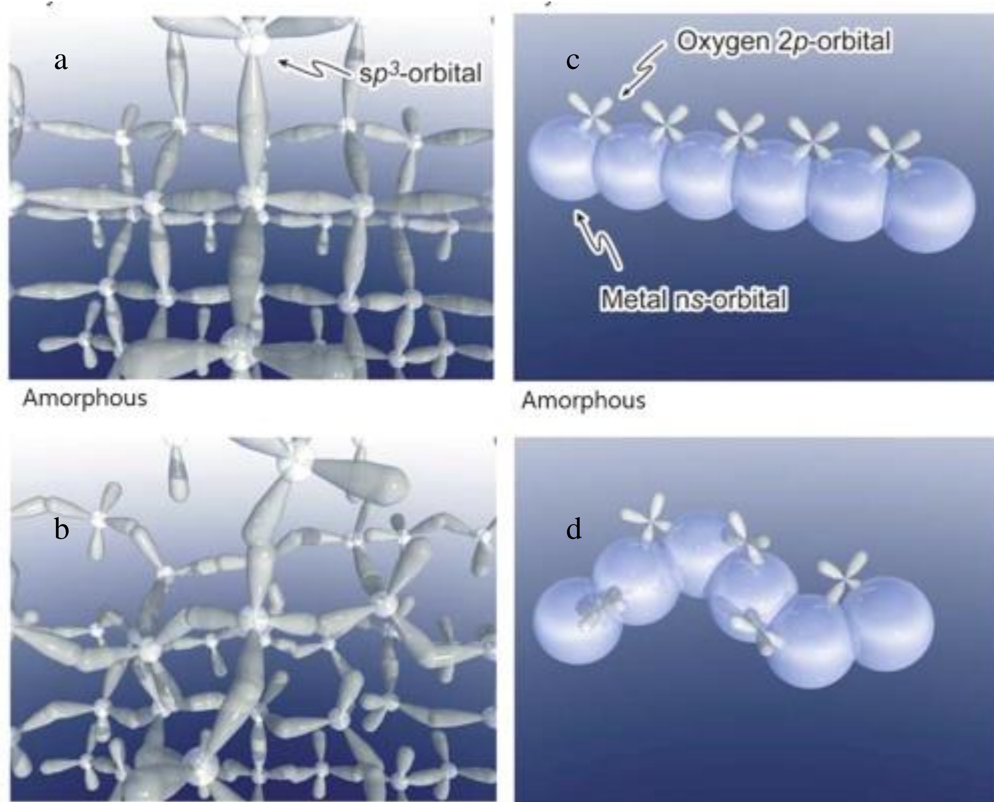


Figure II-7 Schematic orbital drawings of carrier pathways in (a) crystalline Si, (b) amorphous Si, (c) crystalline oxides, and (d) amorphous oxides [11].

II.2.5 Optical properties of a-IGZO

a-IGZO have wide band gap and high transmittance. The transmittance characterized by UV-VIS technique. a-IGZO thin films show high transmittance about 90%. Figure II-8 shows measured transmittance of a-IGZO thin films [12].

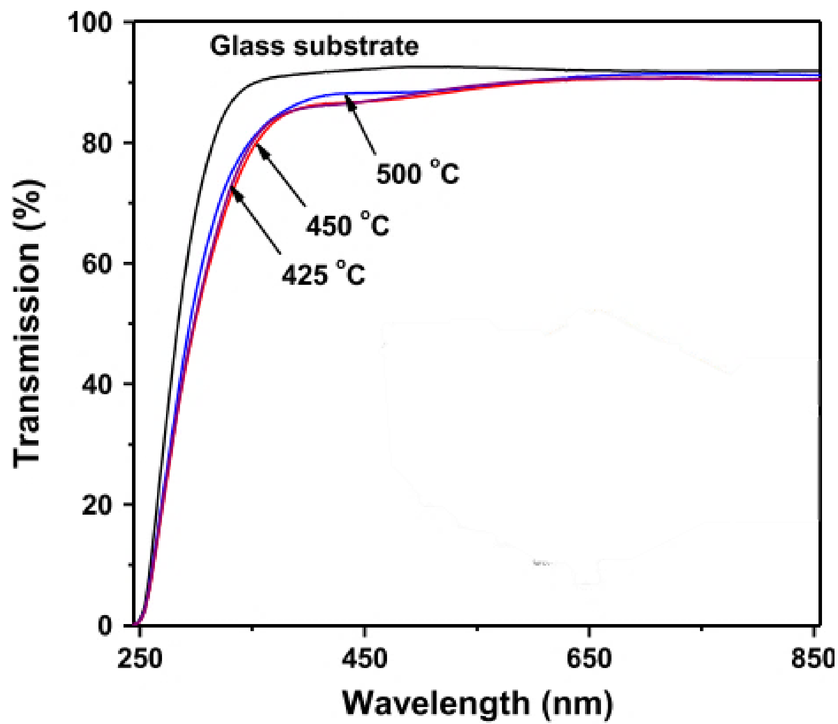


Figure II-8 Optical transmittance spectra of glass substrate and glass/a-IGZO thin film samples [12].

Band gap values of a-IGZO are usually estimated by Tauc's plot [13], which has the form of $\alpha E = [B(E - E_a]^r$ where α is the absorption coefficient, E the photon energy and B and r constants. Supposing parabolic bands and distinction of the k-selection rule for optical transition, r=2 is generally employed as plotted in Figure II.9. It has been found that the estimated bandgaps (Tauc's gaps) are 3.0-3.2 eV for a-IGZO and expected to be larger for high-quality films. It may be worth to notice that optical spectra also provide information about subgap density of states.

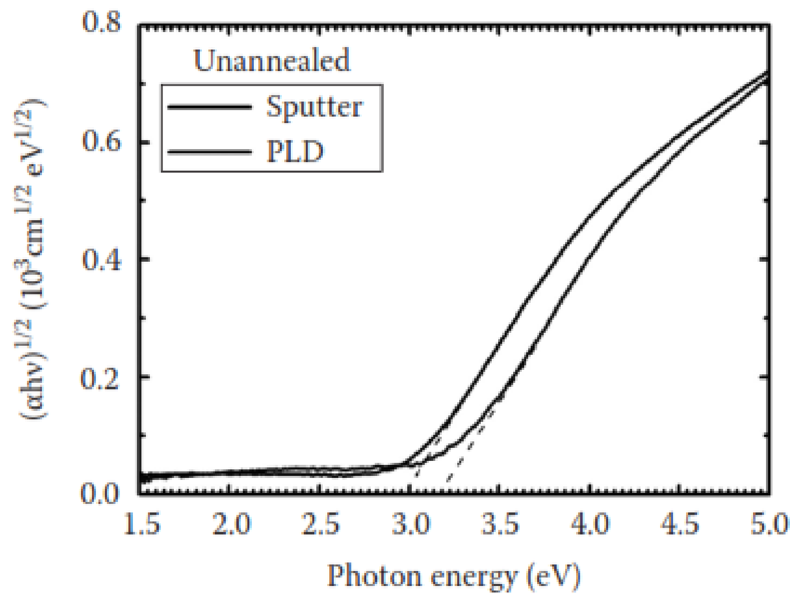


Figure II-9 Optical. absorption. spectra. of. a-IGZO. films. deposited. by. RF. magnetron. sputtering. and. PLD at RT plotted. in. terms of Tauc's plot [13].

II.2.6 Defect levels in IGZO

The incorporation of IGZO semiconductors in electronic devices necessitates a study of their new and unique properties. For semiconductor device application, the electronic structure in the bandgap is also important because defect states in the band gap deteriorate the device performance particularly in TFTs and other a-IGZO applications. However, amorphous semiconductor, carrier transport properties and mechanisms are strongly influenced by structural randomness. Figure II-10 shows a schematic view of density of states (DOS) in the bandgap $\mathrm{D(E)}$ for a-IGZO and a-Si:H. Amorphous materials characterized by tail states below the conduction band minimum (CBM) and above the valance band maximum (VBM). tails bands which is the result of disorder in the structure. a-Si:H has different charges due to donor and acceptor levels. The different charge states are labeled as $\mathrm{D^-}$ $/\mathrm{D^0}$ / $\mathrm{D^+}$. A similar subgap DOS has been revealed for a-IGZO as shown Figure II-10.a. There are some differences because the type of chemical bounds in the two materials. The $D(E)$ are smaller in a-IGZO compared to a-Si:H [14].

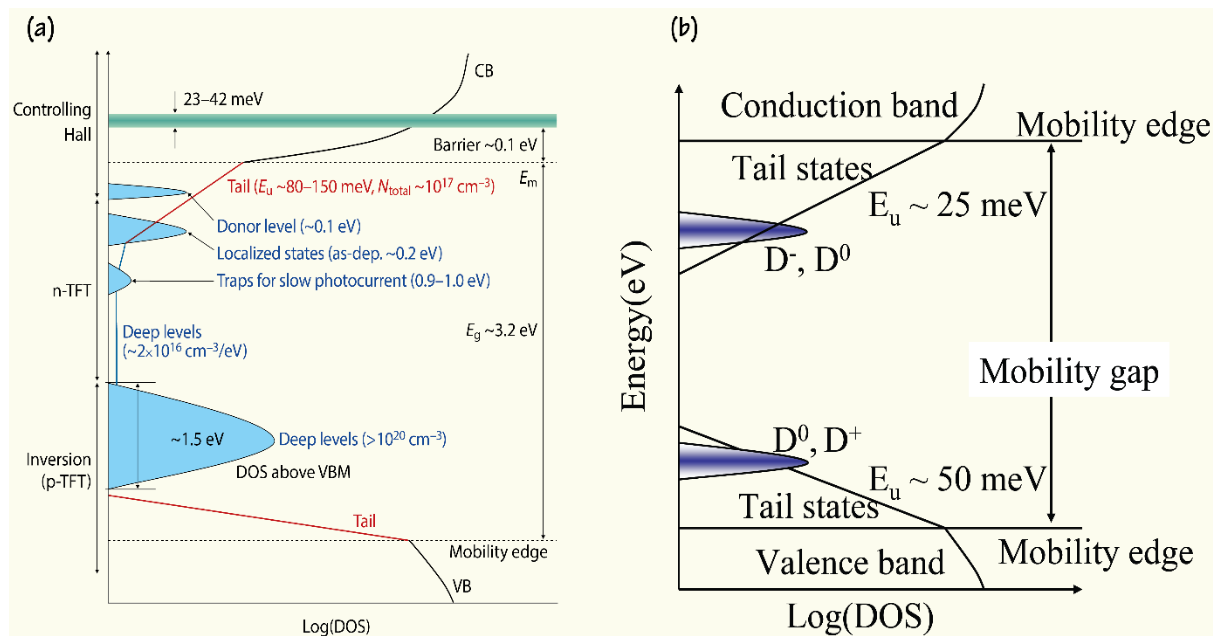


Figure II-10 Schematic models of subgap DOS in (a)a-IGZO and (b) a-Si:H [14].

Many works investigated the origin the defect states in band gap. They use several methods to characterize and modulate sub-gap states. Their defect origin was confirmed by density function theory (DFT) calculations) and optical and electrical analyses of deep defect levels by different techniques such as deep-level transient spectroscopy (DLTS), isothermal capacitance transient spectroscopy (ICTS), and photothermal deflection spectroscopy (PDS). These techniques can provide detailed information on defects while hard X-ray photoelectron spectroscopy (HX-PES) gives additional insight into defect levels inside the bandgap [15].

II.2.6.a Oxygen vacancy

The oxygen vacancy (OV) formation in AOS results in partial reduction of the material where the two electrons, left when removing a neutral O atom, reduces OV to OV $^{2+}$. It is clear when the defect equation for an OV is written in a Kröger–Vink notation as $OV \rightarrow OV^{+2} + 2e^{-}$ [6]. Therefore, OV acts like a donor and is double positively charged when fully ionized. There are two ways for formation oxygen vacancy. (1) oxygen atom absence during film deposition. (2)

the existence of H atoms in AOS forming $O-H$. React two $O-H$ with each other and cause additional OV, like the following equation $M-O-H+M-O-H \rightarrow OV^{+2}+M-O-M+H_2O+2e^-$ [16], [17]. OV is very difficult to characterize directly but its effects on the electronic state and optical properties are measurable. Their origin was confirmed by DFT, TCAD Simulation. CPM and C-V characterization are used to estimate the OV defect position near CBM. While this proposition needs more study, HX-PES gives additional perception into defect levels inside the bandgap. HX-PES results indicate that hydrogen atoms occupying OV sites in IGZO are the main donors in this semiconductor deep states near VBM [18].

II.2.6.b Deep States

HAXPES is useful to observe these subgap defects and provides more reliable information from a deep bulk region. Figure II-11 shows HAXPES spectra around the band gap region. Since the report of the near-VBM states in a-IGZO by HAXPES, many groups have investigated the origins of the near- VBM states [19], [20]. Some groups firstly indicated that oxygen deficiencies with free space (voids) would be a plausible origin based on density functional theory (DFT) calculation. While, weakly bonded (in other words, undercoordinated or disordered) O is also considered as another origin based on experimental results and beyond-DFT calculations [19]. On the other hand, some groups have reported that the usual a-IGZO films contain hydrogen impurity at concentrations [H]>10^{20}cm^{-3}, and it exists in the –OH form. The hydrogen impurity causes different effects; some hydrogen atoms passivate shallow traps and improve TFT performance, while others cause extra threshold voltage (V_{th}) shift (ΔV_{th}) and temperature instability. Therefore, it is proposed that the hydrogen impurity atoms in a-IGZO work as shallow donors, but the generated free electrons are trapped and compensated by excess oxygen atoms/molecules incorporated during the film deposition and/or thermal annealing [19]. Therefore, OH is probable the most plausible origin for the near- VBM state [20].

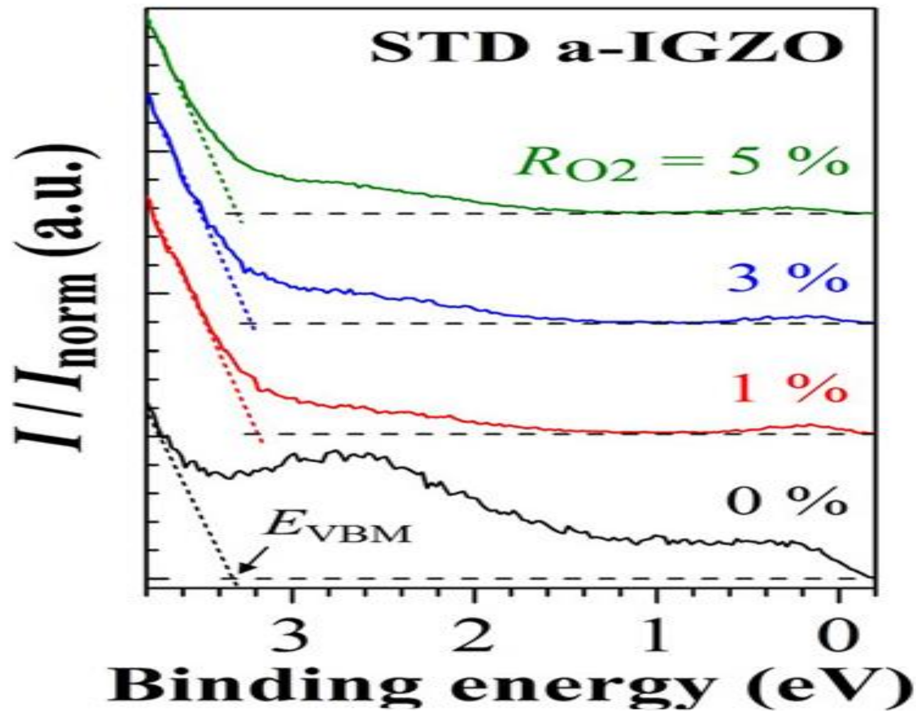


Figure II-11 HAXPES spectra around the band gap region [19]

II.3 Growth a-IGZO thin films by sol-Gel

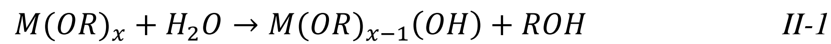
The sol-gel process is a chemical synthesis technique for preparing gels, glasses, and ceramic powders. The sol-gel process generally involves the use of metal alkoxides, which undergo hydrolysis and condensation polymerization reactions to give gels. The production of glasses by the sol-gel method permits preparation of glasses at far lower temperatures than is possible by using conventional melting. It also makes possible synthesis of compositions that are difficult to obtain by conventional means because of problems associated with volatilization, high melting temperatures, or crystallization. In addition, the sol-gel approach is a high-purity process that leads to excellent homogeneity and is adaptable to producing films and fibers as well as bulk pieces [21].

The sol-gel process is typically based on the use of alkoxide starting reagents and alcohol solvents. Depending on the material system and starting reagent reactively common alcohols, such as methanol and ethanol, may used, however more reactive alkoxide starting reagents, less

common alcohols such as 2-methoxyethanol and propanediol have also found widespread utilization. Consideration in selection of reagents and solvent are to exert control over the hydrolysis and condensation reaction that lead to oligomerization, i.e, the development of short polymeric species.

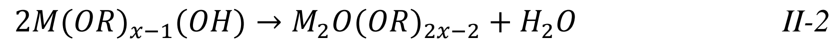
The reaction in the sol-gel process that lead to formation of oligomeric species with $M - O - M$ bonds are as follows [22]:

Hydrolysis



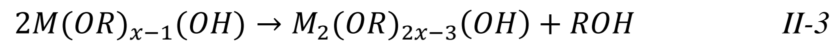
$$M(OR)_x + H_2O \rightarrow M(OR)_{x-1}(OH) + ROH \qquad \textit{II-1}$$

Condensation (water elimination)



$$2M(OR)_{x-1}(OH) \rightarrow M_2O(OR)_{2x-2} + H_2O \qquad \textit{II-2}$$

Condensation (alcohol elimination)



$$2M(OR)_{x-1}(OH) \rightarrow M_2(OR)_{2x-3}(OH) + ROH \qquad \textit{II-3}$$

The Figure II-12 summarized and explain processing stages in chemical solution deposition of thin films.

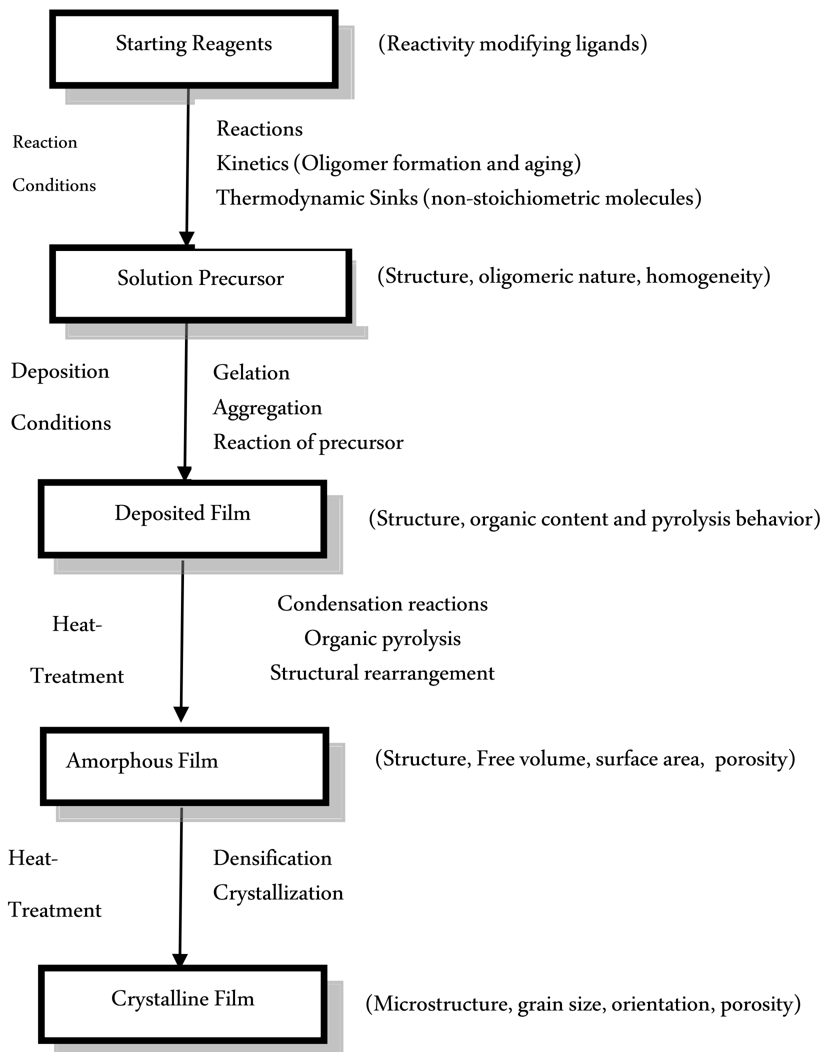


Figure II-12 Processing stages in chemical solution deposition of thin films. Controllable parameters are shown on the left.

II.3.1 Spin coating

Spin coating has been used to deposit ultrathin to relatively thick coatings on flat substrates for several decades. Various materials, including resin, epoxy polymers and sol-gel stock solution, have been successfully coated on metal, glass, ceramic, plastic, paper and semiconductor substrates in different industries.

This technique normally uses the material to be coated in its liquid from or dissolved in a liquid solvent. Typically, the substrate to be coated in held in place using a motor-driven vacuum

chuck, as show Figure II-13, and the coating solution is dispensed on the substrate either manually or by an automated robotic arm. The substrate is then accelerated to very high angular velocities ($\sim 300\ to\ 10{,}000\ rpm$) during which the excess liquid spun off from the substrate leaving a thin uniform coating. Thicknesses of less than 30 nm to few microns per layer can be easily achieved. The centrifugal forces created by equilibrium between the centrifugal forces created by the rapid spinning and the viscous forces determined by the viscosity of liquid. The film thickness can be varied by controlling the spin and time, as well as the viscosity of the solution.

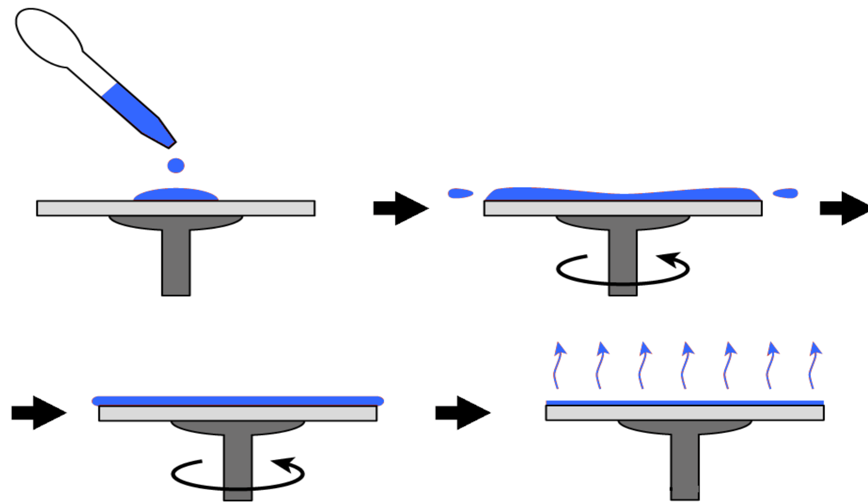


Figure II-13 Spin coating method.

TableII-1: Summary of film deposition sol-gel spin coating.

Technique	Thickness	Advantage	Limitations	Application
Spin coating	10nm-5µm	Uniformity, reproducibility, excellent, thickness control, low cost	Requires flat substrate, high material loss	Photoresists, dielectric layers, flat panel displays

II.4 Characterization a-IGZO thin films

II.4.1 X-Ray Diffraction characterization

This very important experimental technique has long been used to address all issues related to the crystal structure, lattice constants and crystallography, identification of unknown materials, orientation of single crystals and preferred orientation of polycrystals, defects, stresses, etc [23].

The basic principles associated with diffraction (in reflection, transmission or glancing angle geometry) are generally introduced with reference to X-ray scattering and interference. X-rays are a form of energetic electromagnetic radiation of wavelength $\approx 10^{-10}- 10^{-11}m$ of comparable size to the spacing of atoms within a solid. A crystal lattice comprises a regular array of atoms; the electron clouds around these acts as point sources for spherical X-ray wavelets, through a process of absorption and re-emission, when interaction with an incident beam of X-ray occurs. The positions of the resultant maxima in scattering intensity may be used to deduce crystal plane spacing and hence the structure of an unknown sample. Geometrical considerations show that the scattering angles corresponding to diffracted intensity maxima can be described by the Bragg equation [24]:

$$n\lambda = 2dsin\theta \qquad II\text{-}4$$

This equation (Sometimes expressed as $\lambda = 2d_{hkl}sin\theta_{hkl}$) describes the minimum condition for the coherent diffraction of a monochromatic X-ray beam from a set of planes of a primitive lattice. Figure II.14 illustrates the geometrical conditions associated with Bragg diffraction from a set of $\{hkl\}$ planes spaced d_{hkl} apart, with X-rays incident at a Bragg angle θ being diffracted through an angle 2θ. The path difference between the X-rays ‘reflected’ from successive planes must be equivalent to an integer number of wavelengths n for constructive interference to occur [23].

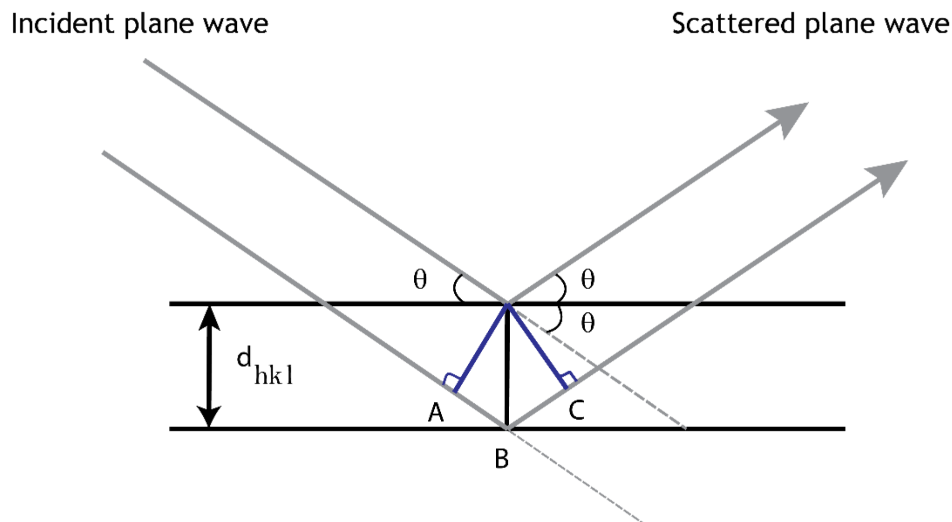


Figure II-14 Geometric illustration of Bragg diffraction. For constructive interference, $n\lambda = AB + BC = 2d\sin\theta$.

Since amorphous materials do not exhibit long-range order, their diffraction profiles show diffuse intensities rather than well-defined maxima [25].

Figure II-15 shows an X-ray diffractometer. An X-ray diffractometer comprises a source of X-rays, the X-ray generator, a diffractometer assembly, a detector assembly and X-ray data collection and processing systems. The diffractometer assembly controls the alignment of the beam, as well as the position and orientation of both the specimen and the X-ray detector. An X-ray spectrum is usually recorded by rotating an X-ray detector about the sample, mounted on the diffractometer goniometer stage. The goniometer allows the sample to be rotated about one or more axes [24].

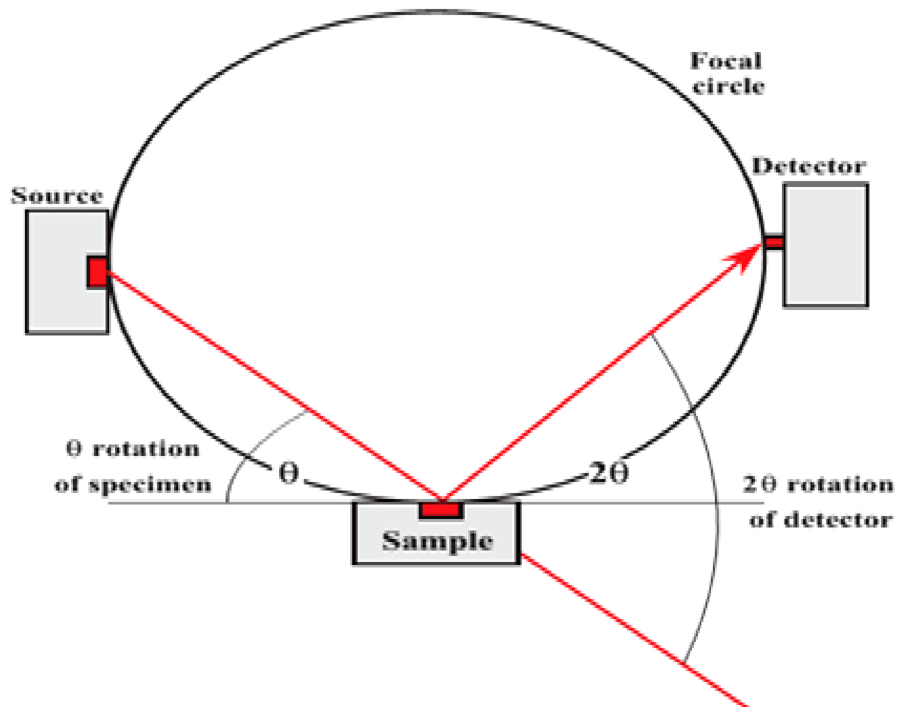


Figure II-15 A sample mounted on a goniometry which can be rotated about one or more axis, and a detector which travels along the focusing circle in the Bragg–Brentano geometry.

II.4.2 UV-VIS Spectroscopy

Optical transmission or absorption measurements determines the optical absorption coefficient [26]. The absorption coefficient is usually measured via the transmission coefficient of the electromagnetic radiation through the sample. When the electromagnetic field with intensity I_0 hits the sample, only part of it, TI_0 , is transmitted, the other part RI_0 being reflected as shown Figure II-16.

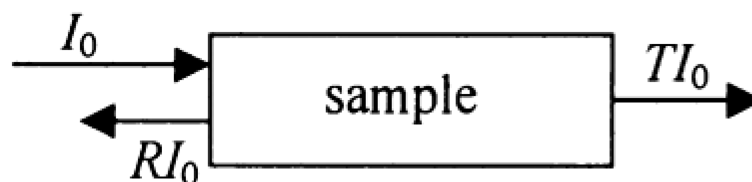


Figure II-16 Light transmission and reflection from a sample.

On propagation through bulk materials, the transmitted intensity of the radiation with frequency ω is given by [26].

$$I(\omega) = T(\omega)I_0(\omega) = [1 - R(\omega)]I_0(\omega)exp\,(-\alpha_{tot}(\omega)d) \quad \text{II-5}$$

Where d is the thickness of the sample, $[1 - R(\omega)]I_0(\omega)$ is the fraction of incident radiation intensity which enters the sample, and the total absorption (called sometimes extinction) is $\alpha_{abs} = \alpha_{abs} + \alpha_{scat}$. The transmission coefficient is defined as

$$T(\omega) = I(\omega)/I_0(\omega) \quad \text{II-6}$$

A spectrometer for measuring $I(\omega)$ in the visible and UV consists of light source, a monochromator or polychromator, and a detector as shown Figure II-17.

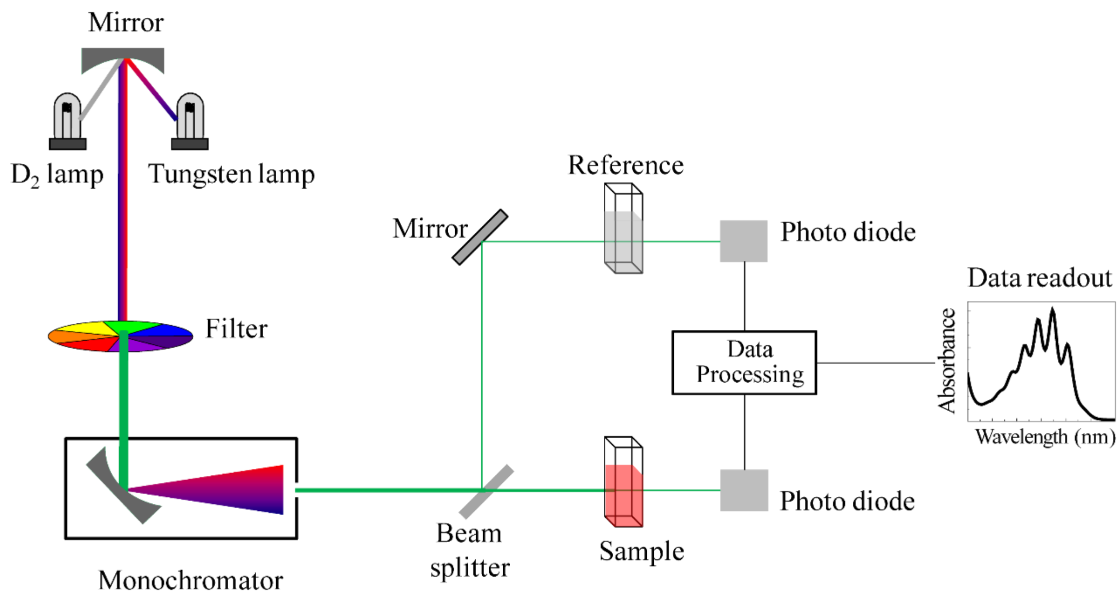


Figure II-17 Schematic of UV- visible spectrophotometer.

Light from the source is first dispersed by a monochromator, and the resulting monochromatic light is sent to the sample and recorded by a detector. The spectra at the far right depicts the components of typical visible-UV spectrometer and how they are used to measure $I(\omega)$. Tow lamps send a beam of light from a visible and UV light source. Monochromators (single wavelength) are instruments that disperse the different component of the light emitted by the source.

Optical elements such as mirrors and beam splitter are used to manipulate the light beams. One beam, the sample beam, passes through a small transparent container (cuvette) containing a solution of the compound being studied in a transparent solvent. The other beam, the reference, passes through an identical cuvette containing only the solvent. The intensities of these light beams are then measured by electronic detectors and compared. The intensity of the reference beam, which should have suffered little or no light absorption, is defined as I_0. The intensity of the sample beam is defined as I. Over a short period of time, the spectrometer automatically scans all the component wavelengths in the manner described. The ultraviolet (UV) region scanned is normally from 200 to 400 nm, and the visible portion is from 400 to 800 nm. Near infrared beam may be used for extra information. Various types of UV-Vis spectrometers, which contain the above optical components and a control computer, are commercially available [27].

II.5 Fabrication a-IGZO TFT

II.5.1 TFT structure

This section describes transistors with a-IGZO as an active layer in TFT. a-IGZO TFT control the electron current across source and drain (S/D) regions formed in a-IGZO, using a gate field through an insulating film. Structures of a-IGZO TFT can be roughly classified into the following four categories, depending on the positions of the active layer, gate electrode, and S/D electrodes and to classify them into combinations of top/bottom gate and top/bottom contact [15]:

- Top gate top contact
- Bottom gate top contact
- Inverted staggered (etch stopper)
- Inverted staggered (channel etch)

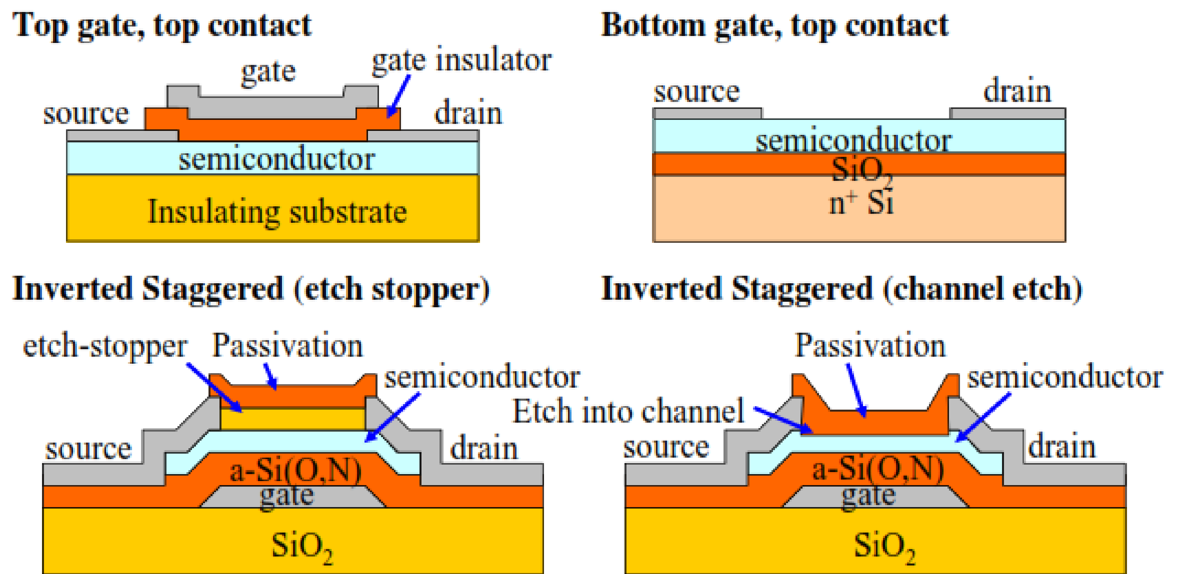


Figure II-18 of the four different TFT structures.

1. Top gate top contact

The top-gate structure was used for TFTs using epitaxial layers in which it is difficult to form a bottom electrode. This structure has other advantages. For example, it requires only two patterning mask steps at minimum, and the upper gate insulator and electrode act as passivation layers that protect the channel layer from degradation due to atmospheric exposure. Compared with other structures, the parasitic capacitance between S/D and gate electrodes is reduced. Moreover, the channel region in top gate, top contact is not exposed to any etching damage, which improves the transistor characteristics. Being a top-gate-type structure, it can easily employ a thin gate insulator and scale down the channel length [28].

2. Bottom gate top contact

Bottom-gate structures are common in laboratory research because commercially available SiO_2/Si wafers can be used for the gate insulator and electrode, respectively, and TFT structures are easily formed by the deposition of a channel layer with a single mask step to form the source

and drain electrodes This structure is, of course, not applicable to practical displays, and it has various disadvantages. For example, (i) the back-channel surface is exposed to the atmosphere, and therefore the TFT characteristics can be affected by the adsorption, desorption and diffusion of atmospheric gases, causing instability. (ii) The gate—source/drain overlaps are very large and result in a large parasitic capacitance, which slows the response of devices and circuits. Both gate structures can employ either top-contact or bottom-contact structures. An advantage of the top-contact structure for oxide TFTs is that it can minimize the oxidation of the source/drain electrodes at the semiconductor channel interface, and geometrically accurate contacts can easily be formed. On the other hand, using a bottom-contact structure, more care is required to make good contacts with the upper channel layer, such as by forming taper-edge structures in the electrodes [28].

3. Inverted staggered (etch stopper /channel etch)

The inverse-staggered structure used in a-Si TFT backplanes in flat-panel displays such as LCDs. This structure is often adopted for research and development of oxide semiconductors, because of the availability of production lines, equipment, and processes. One reason for this is that the same structures are used for a-Si:H TFTs. These structures employ bottom-gate and top-contact configurations, which are further classified by the structure above the channel layer. One is an etch-stopper structure, where an etching protection layer is formed before forming the source and drain; the latter are patterned by etching. The other is a channel-etch structure where a part of the channel layer is removed when the source and drain are formed by etching. The channel-etching procedure damages the back- channel surface and can cause the degradation of TFT characteristics; it also requires a thick channel to stop etching in the channel layer. The etch-stopper structure is free from these problems but requires an extra patterning mask. Both structures have been employed for the mass production of a-Si:H TFTs and are also used for AOS TFTs [28].

II.5.2 TFT process fabrication

In this section we focus on the process fabrication of the two structures: bottom gate top contact and staggered inverted.

II.5.2.a Bottom gate top contact structure

We use commercial substrate Si n+ (work as gate and substrate) with SiO_2 layer (dielectric). The substrate cleaned by acetone, propanol and deionized water. After dry with nitrogen gas if possible. The a-IGZO layer deposited after cleaning process. Next shadow mask to define source and drain electrodes. Widely known make annealing step after source and drain disposition. The Figure II-19 summarized fabrication Bottom gate top contact on Si/SiO_2 substrate

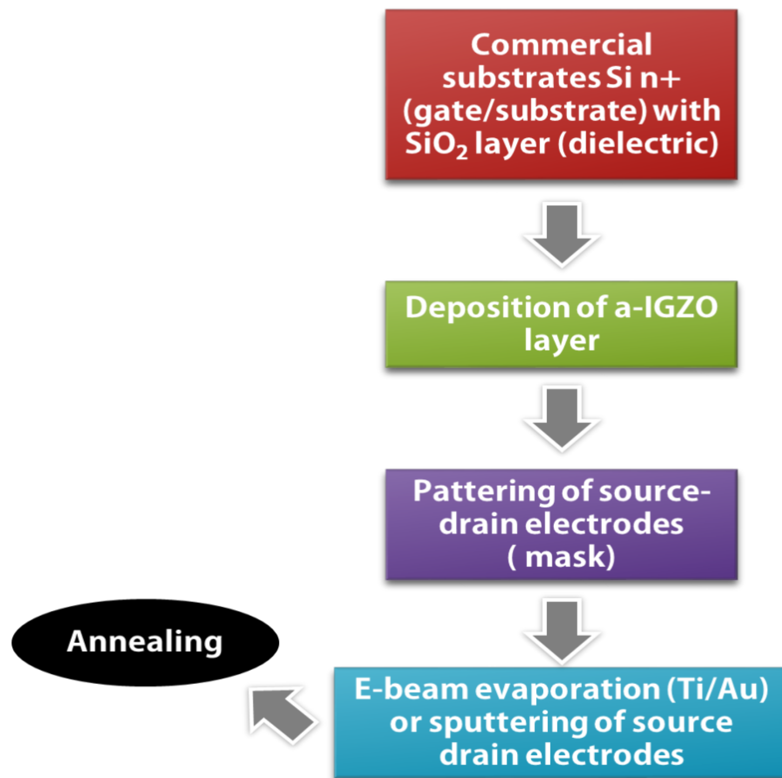


Figure II-19 Process flow used to produce oxide TFTs bottom gate using commercial Si/SiO_2

II.5.2.b Staggered inverted structure

In this structure we can use many types of substrate flexible and glass. First step is cleaning by acetone and IPA(ISO propyl Alcohol) and use a mask#1 for define gate electrode. Sputtering of dielectric. Secondly using mask#2 to define dimensions of gate insulator. Etching of dielectric by RIE (Reactive-ion etching). After use mask#3 for determine width and length of active layer. Sputtering a-IGZO. Disadvantage this structure need vacuum equipment plus high clean chamber. Next lift of semiconductors and use mask#4 for pattering of source/drain electrodes finally sputtering of source and drain life off of source electrodes favorable make annealing as last step. The *Figure II-20* show illustration to descript process of fabrication Staggered structure.

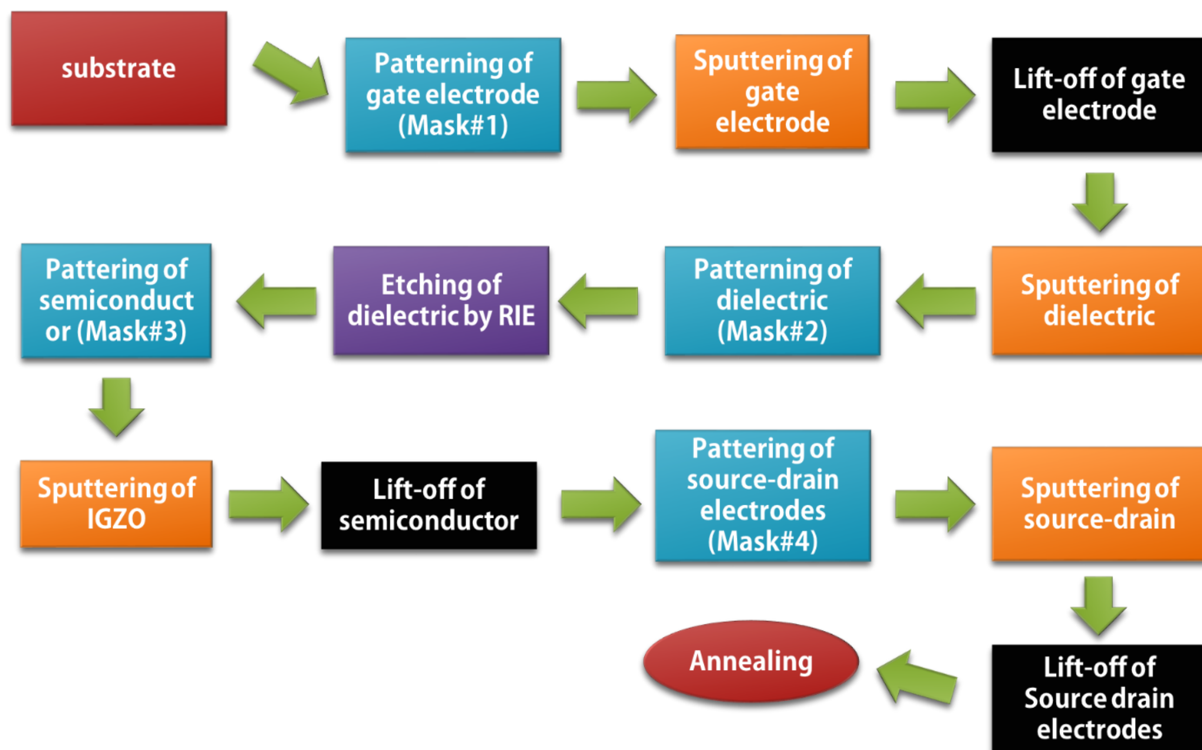


Figure II-20 Process flow used to produce oxide TFTs Inverted staggered gate using employing glass substrates

II.6 TFT characteristics and performance indexes

TFTs are three terminal field-effect devices. The ideal operation of an n-type TFT depends on the existence of an electron accumulation layer at the dielectric/semiconductor interface. This is achieved for a gate voltage (V_{GS}) higher than a certain threshold (V_T), corresponding to downward band-bending of the semiconductor close to its interface with the dielectric [28], [29].

II.6.1 I-V characteristics

TFT indexes are usually deduced from the output characteristics, where the source-to-drain current (I_{DS}) is plotted against the source-to-drain voltage (V_{DS}) for various gate-to-source voltages (V_{GS}), and from the transfer characteristics, where I_{DS} is plotted against V_{GS} for various V_{GS}, as shown in Figure II-21.

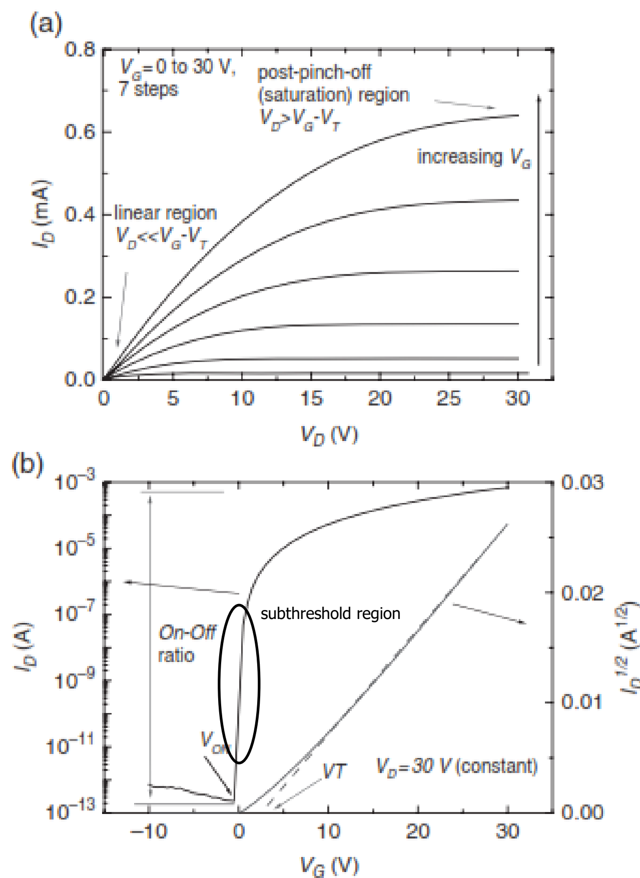


Figure II-21 Typical a) output and b) transfer characteristics of a n-type oxide TFT[29].

As a simple analytical model, analytical formulas on gradual channel approximation are used. As explained in chapter.I I_{DS}, the drain current of a MOSFET is expressed as the sum of the diffusion and drift currents. For $V_{GS} > V_T$, provided that positive drain (V_{DS}) is applied, current flows between the drain and source electrodes (I_{DS}), corresponding to the *on-state* of the TFT. For $V_G < V_T$, regardless of value of V_{DS} the upward band-bending of the semiconductor close to the interface with dielectric is verified, resulting in a low I_{DS} that corresponds to the TFT *off-state.*

Depending on V_{DS}, different operation regimes can be observed during on state as given by the following equation:

$$I_{DS} = \begin{cases} C_i \mu_{FE} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] & \text{for } (V_{GS} - V_T > V_{DS}) \\ C_i \mu_{sat} \frac{W}{2L} (V_G - V_T)^2 & \text{for } (V_G - V_T \leq V_{DS}) \end{cases} \quad \text{II-7}$$

Where C_i is the gate capacitance per unite area, W is the channel width and L is the channel length. μ_{FE} is the field-effect mobility and μ_{sat} is the saturation mobility.

- Pre-pinch-off regime or linear regime for $V_{DS} < V_{GS} - V_T$ for low V_{DS}. The quadratic term can be neglected.
- Post-pinch-off or saturation regime for $V_{DS} > V_{GS} - V_T$.

The measured output characteristics, $I_{DS} - V_{DS}$, of the TFT are shown in Figure II-21.a. The measurement is performed for different gate bias voltages and for each gate bias voltage the drain bias voltage V is swept from 0 to 30 V to show clearly the pre- and post-pinch-off regimes defined above. Different qualitative information can be assessed from the output characteristics. A decreasing separation between I_{DS}– V_{DS} curves for increasing $V_G$is indicative of μ degradation for that V_{GS} range and the flatness of the I_{DS}– V_{DS} curves at the post-pinch-off regime permits to evaluate if the channel layer can be fully depleted close to the drain electrode for the range of V_{GS} and V_{DS} used. The saturation region are important for the operation of OLED displays and should be as horizontal as possible. The low V_{DS} region (linear) also provides useful information regarding the contact resistance.

Transfer characteristics, where V_{GS} is swept for a constant V_{DS}, permit to extract a large number of measurable electrical parameters, which are summarized in the next sub-sections [14], [29], [30].

• I_{On}/I_{off} this is simply defined as the ratio of the maximum to the minimum I_{DS}. The minimum I_{DS} is generally given by the noise level of the measurement equipment or by the gate leakage current, while the maximum I_{DS} depends on the semiconductor material itself and on the effectiveness of capacitive injection by the field effect. I_{On}/I_{off}*On/off* above 10^6 are typically obtained in TFTs and a large value is required for their successful usage as electronic switches.

• **V_T and turn-on voltage (V_{on}):** V_T corresponds to the V_{GS} for which an accumulation layer or conductive channel is formed close to the dielectric/semiconductors interface, between the source and drain electrodes. For an n-type TFT, depending upon whether V_T is positive or negative, the devices are designated as enhancement or depletion mode, respectively. A simple method to determine V_T is to use a liner extrapolation of the $I_{DS} - V_{GS}$ plot for low V_{DS} or of the $I_{DS}^{1/2} - V_{GS}$ for high V_{DS}. The concept of V_{on} is widely used in the literature, simply corresponding to the V_{GS} at which I_{DS} starts to increase as shown in Figure II-21.

• **Subthreshold swing (S):** Another important TFT parameter is the subthreshold voltage swing (S value), which reflects the value of V_{GS} required to obtain 10 times larger I_{DS} in the subthreshold region. It is defined as the inverse of the maximum slope of the transfer characteristic.

$$S = \left(\frac{dlog(I_{DS})}{dV_{GS}}|max\, I_{DS}\right)^{-1} \quad \text{II-8}$$

The importance of S is that it determines the minimum V_{GS} required to turn a TFT from the off state to the on state, roughly estimated as $\Delta V_{GS,min} = S \times R_{on/off}$. It also provides important information about the quality of a TFT. It is related to the trap density in the band gap (subgap traps) at the Fermi level (D_{sg}) as

$$S = ln10 \times \frac{k_bT}{e}\left(1 + \frac{eD_{sg}}{C_i}\right) \quad \text{II-9}$$

K_b,T , e are the Boltzmann constant, the temperature and the electron charge respectively.

• **Mobility (μ)** this is related to the efficiency of carrier transport in a material, affecting directly the I_{DS} maximum. Based on the analytical formulas, the mobility in each region can be

calculated separately for the two regions. The mobility in linear and saturation regions are called field effect mobility and given by the following formulas.

Field effect mobility

$$\mu_{FE} = \frac{L}{WC_i}\frac{1}{V_{DS}}\frac{\partial I_{DS}}{\partial V_{GS}} \quad \text{II-10}$$

- *Saturation mobility*

$$\mu_{sat} = \frac{2L}{Wc_i}\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)^2 \quad \text{II-11}$$

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Chapter III

Simulation and fabrication of a-IGZO thin film transistors

III.1 Introduction

Physics of thin film transistors (TFT) attract many groups to understand its working phenomena. Accumulation, electron recombination…etc are amongst many phenomena. In this chapter, TFT simulation and fabrication are detailed. The simulation of the TFT is carried out using Silvaco Atlas. The simulation of TFT is based on defining its structure and the physics models used and solving equations that describe the transport phenomena in semiconductors. The output of simulation are current-voltage characteristics and internal parameters such as electron concentration and electrics field, defects…etc. Fabrication of TFT by sol gel is common for easy fabrication of TFT. A fabricated TFT bottom structure by sol gel method is demonstrated.

III.2 Simulation IGZO thin film transistors

Simulation is the process of using a computer to solve complicated equations that describe involved phenomena. Solution of equations can give behavior prediction of a real experience. Semiconductor simulation involves the numerical solution of equations describing the physics of semiconductor materials. In the present case, a computer software is used to solve equations that describe phenomena in semiconductor materials such as drift diffusion, Poisson equation and carrier continuity equations. An available commercial tool SILVACO TCAD. SILVACO TCAD is the abbreviation of **Sil**icon **Va**lley **Co**rporation Technology Computer Aided Design is used to simulate TFTs.

III.2.1 Fundamentals of Device Simulation

Device simulation has two main purposes: to understand and to depict the physical processes in the inside of a device, and to make reliable predictions of the performance of devices. The quality of physical models is vital for understanding of the physical processes in semiconductor devices and for reliable prediction of device characteristics. Many years of research into device physics has resulted in a mathematical model describing the operation of many semiconductor devices. This model consists of a set of fundamental equations that link together the electrostatic potential and the carrier densities within a simulation domain. These equations consist of Poisson's equation, current continuity equations, and transport equations. The analyses of most semiconductor devices include the calculation of the electrostatic potential within the device as a function of the charge distribution [1].

To calculate the electrical behavior of a semiconductor device we use fundamental electrostatic properties. Those equations are [1]:

$$\frac{dE}{dx} = \frac{q}{\varepsilon_s}(p - n + N_d - N_a) \quad \text{III-1}$$

and

$$E = -\frac{d\psi}{dx} \quad \text{III-2}$$

Where E is electrical field while q and ε_s are electron charge and dielectric constant of the semiconductor's material. The total carries concentration expressed by hole (p) concentration minus electron concentration (n) plus the sum of difference between donor density (N_d) and acceptor density (N_a). Replacing equation III-2 into III-1 give Poisson equation [1]:

The continuity equation describes a basic concept, namely that a change in carrier density over time is due to the difference between the incoming and outgoing flux of carriers plus the generation and minus the recombination. The continuity equation for electron and holes expressed by [2]:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla J_n \mp G_n - R_n \quad \text{III-3}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q}\nabla J_p \mp G_p - R_p \qquad \text{III-4}$$

Here J_n and J_p are the electron and hole current densities respectively; G_n and G_p are the generation rates for electron and holes respectively and R_n and R_p are recombination rates for electron and holes respectively. There are several of transport models express transport charge in semiconductor devices such as drift-diffusion, the energy balance model and the hydrodynamic model.

The simplest model of charge transport is the drift-diffusion model. It can give a very close prediction to experimental results in TFT devices. The current densities in the continuity equation can be written according to drift-diffusion model as

$$J_n = -q\mu_n n \nabla\varphi_n \qquad \text{III-5}$$

$$J_p = -q\mu_p p \nabla\varphi_p \qquad \text{III-6}$$

Here μ_n and μ_p are the electron and the hole mobilities, respectively, and φ_n and φ_p are the quasi-Fermi levels of the electron and holes, respectively. The quasi-Fermi levels are then linked to the carrier concertation and the potential through the two Boltzman approximation where

$$n = n_i exp\left(\frac{q(\psi-\varphi_n)}{KbT}\right) \qquad \text{III-7}$$

$$p = n_i exp\left(\frac{-q(\psi-\varphi_p)}{KbT}\right) \qquad \text{III-8}$$

Here n_i is the effective intrinsic concentration T is the temperature. Thus [3]:

$$J_n = qn\mu_n E_n + qD_n\nabla n \qquad \text{III-9}$$

$$J_p = qp\mu_p E_p - qD_p\nabla p \qquad \text{III-10}$$

Where D_n and D_p represent the electron and hole diffusion constant expressed by Einstein relationship

$$D_n = \frac{kbT}{q}\mu_n \qquad \text{III-11}$$

$$D_p = \frac{kbT}{q}\mu_p \qquad \text{III-12}$$

If Fermi-Dirac statistics is assumed, D_n becomes [3]:

$$D_n = \frac{\frac{KbT}{q}\mu_n F_{1/2}(\frac{1}{kbT}(E_{F_n} - E_C)}{F_{-1/2}(1/KbT(E_{F_n} - E_C)} \qquad \text{III-13}$$

Where $F_{1/2}$ is the Fermi-Dirac integral of order $\alpha = \frac{1}{2}$ and written as:

$$F_\alpha(\eta_s) = \frac{2}{\sqrt{\pi}}\int_0^\infty \frac{\eta^\alpha}{1+exp\,(\eta+\eta_s)}d\eta \qquad \text{III-14}$$

Here η_s takes the from $\eta_C = (E_{F_n} - E_c)/K_bT)$ for electron or $\eta_V = (E_{F_n} - E_V)/K_bT)$ for holes and η is the electron energy.

One of the most important physical processes resulting in the generation and recombination of carriers is the capture and emission of carriers through localized energy states, generally termed traps, located in the energy band gap. These traps typically occur due to the presence of lattice defects or impurity atoms that introduce energy levels near the center of the energy band gap

In this process, these localized states act as stepping stones for an electron from the conduction band to the valence band. A model that formulates this process adequately is the Shockley–Read–Hall theory where the recombination R_{srh} is given by [1], [3]:

$$R_{srh} = \frac{np - n_i}{\tau_p\left\{n - n_i\,exp\left(\frac{E_{trap}}{KbT}\right)\right\} + \tau_n\left\{p - n_i\,exp\left(\frac{E_{trap}}{KbT}\right)\right\}} \qquad \text{III-15}$$

Here E_{trap} is the difference between the trap energy level and the intrinsic Fermi level, T is the lattice temperature, and $\tau_n$and τ_p are the electron and hole lifetimes, respectively

Another type of recombination observed in semiconductor material is Auger recombination. Auger recombination is a nonradiative recombination event, which involves three particles. Typically, an electron and a hole will recombine in a band to-band transition and will give off the resulting energy to another electron or hole. Eventually, this energized particle will lose energy through phonon emission within the atomic lattice. The involvement of a third particle affects the recombination rate such that Auger recombination needs to be treated differently from typical band-to-band recombination. R_{Auger} is expressed as[1]–[3]:

$$R_{Auger} = C_n(pn^2 - nn_i^2) + C_p(np^2 - pn_i^2) \qquad \text{III-16}$$

$C_n$and C_p are Auger parameters.

III.2.2 Simulation by SILVCO TCAD

SILVCO TCAD includes many modules for the simulation of semiconductor devices such as ATHENA and ATLAS. ATHENA is used to simulate the fabrication process while ATLAS is for the electrical device performance. ATHENA and ATLAS work under platform called DECKBUILD. DECKBUILD is an interactive, graphic runtime environment for developing process and device simulation input decks. Figure III-1 shows the DECKBUILD window. It is considered as the principle window of SILVACO where all simulators can be controlled [3], [4]

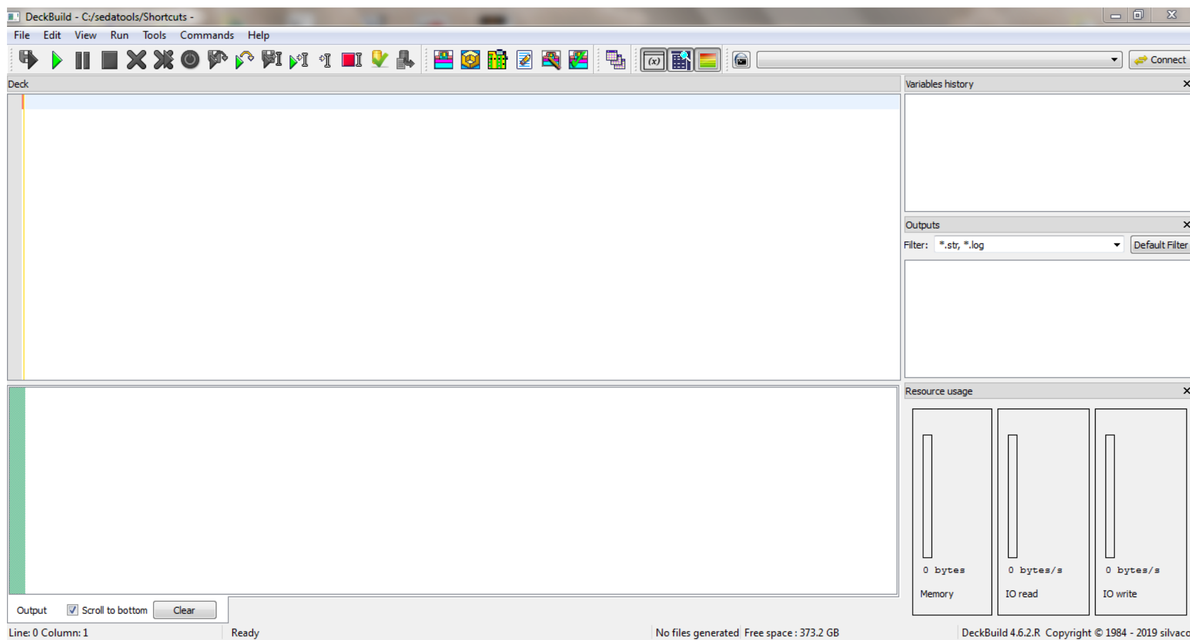

Figure III-1 DECKBUILD window

The obtained results plotted and analyzed by another tool named TONYPLOT. TONYPLOT is a visualization tool which plots the results obtained from simulation. It provides scientific visualization capabilities including xy plots with linear and logarithmic axes, polar plots, surface and contour plots. Figure III-2 shows process SILVACO simulation steps by and the module used for each step

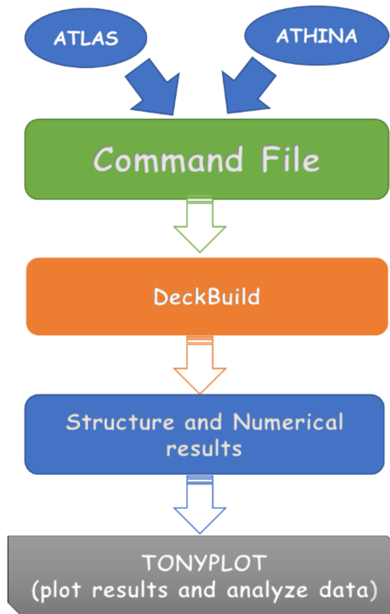

Figure III-2 Process of simulation by SILVACO

III.2.3 Commands File

Command file or Atlas input is a file which contains commands and statements for simulation. This file can be written in the DECKBUILD environment or another program but must run by DEKBUILD. The order in which statements occur in an ATLAS input file is important. There are five groups of statements that must occur in the correct order (see Table III-1). Otherwise, an error message will appear which may cause incorrect operation or termination of the program [3].

Table III-1The order of Atlas commands

Groups	Statements
Structure specification	MESH REGION ELECTRODE DOPING
Material and models specification	CONTACT MATERIAL INTERFACE MODELS
Numerical method selection	METHOD
Solution specification	SOLVE SAVE
Results analysis	TONYPLOT

1. **Structure specification**

Each Atlas run inside DECKBUILD should start with the line: `go atlas`

`<n>.MESH` specifies the location of grid lines along the <n>-axis in a rectangular mesh for 2D or 3D simulation.

Syntax `X.MESH LOCATION=<l> (NODE=<n> [RATIO=<r>])| SPACING=<v>`

`WIDTH` Specifies the extent of a mesh section in the X direction.

`X.MIN/Y.MIN` Specify the location of the beginning of a given mesh section (should only be specified for the first section).

`X.MAX/Y.MAX` Specify the location of the end of a given mesh section (should not be specified if DEPTH/WIDTH is specified).

Region Parameters Device coordinates may be used to add regions to both rectangular and irregular meshes. In either case, boundaries must be specified with the `X.MAX`, `X.MIN`, `Y.MAX`, `Y.MIN`, `Z.MAX`, and `Z.MIN` parameters.

Once the mesh is specified, every part of it must be assigned a material type. This is done with REGION statements:

REGION number=<integer> <material_type> <position parameters>

Region numbers must start at 1 and are increased for each subsequent region statement. A large number of materials is available. The position parameters are specified in microns using the X.MIN, X.MAX, Y.MIN, and Y.MAX parameters.

`MATERIAL` Specifies what material from atlas know materials the statement should apply. If a material is specified, then all regions defined as being composed of that material will be affected.

To define mesh and structure of TFT a-IGZO with 16 nm on SiO_2. And n-poly Si as gate, Al was used as source and drain. Use the following code source

```
go atlas
mesh width=1000 outf=tft.str master.out
x.m l=0 s=3
x.m l=210 s=3
y.m l=0 s=0.001
y.m l=0.016 s=0.0005
y.m l=0.116 s=0.05
# The device is composed of a 16 nm layer of IGZO
# 100 nm oxide on a n++ substrate that acts as the gate.
region num=1 material=igzo y.min=0 y.max=0.016
region num=2 material=sio2 y.min=0.016 y.max=0.116
elec num=1 name=gate bottom
elec num=2 name=source y.max=0.0 x.min=0.0 x.max=5.0
elec num=3 name=drain y.max=0.0 x.min=205.0 x.max=210.0
```

Figure III-3 and Figure III-4 show mesh and structure of 2D a-IGZO TFT generated by using the above code source.

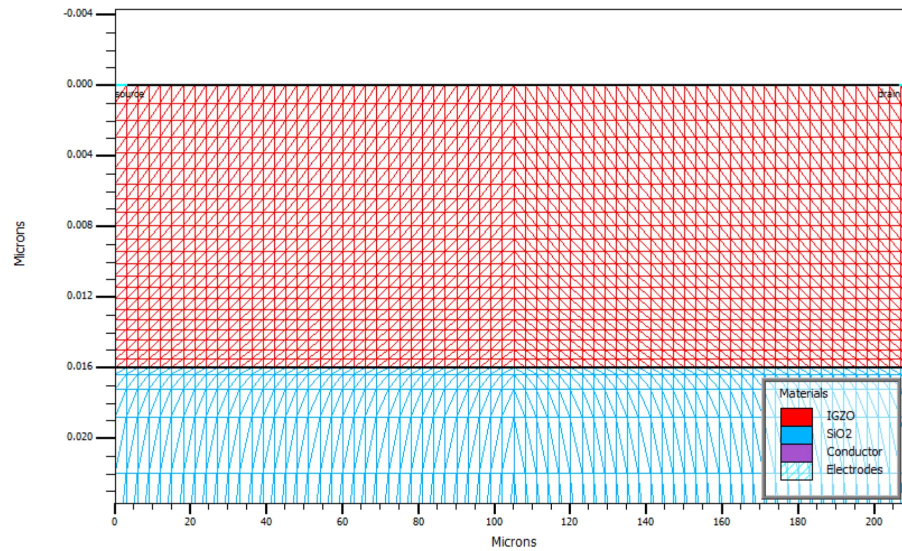

Figure III-3 2D mesh a-IGZO TFT

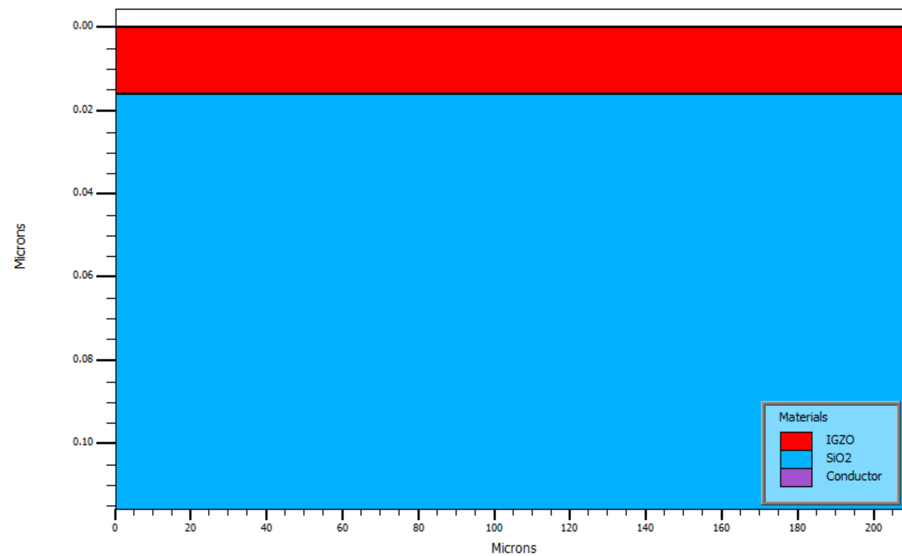

Figure III-4 2D structure of a-IGZO TFT

2. **Material and model's specification**

In this part physical parameters of each material must be specified. Some materials are already known by SILVACO ATLAS but some other material need definition or adjusting their parameters.

The CONTACT statement is used to specify the metal work function of one or more electrodes. The NAME parameter is used to identify which electrode will have it is properties modified. The WORKFUNCTION parameter sets the work function of the electrode. Example:

CONTACT NAME=gate WORKFUNCTION=4.08

The statement of the work function for a n-type polysilicon gate contact is: CONTACT NAME=gate N.POLYSILICON

The following statement "MATERIAL MATERIAL=" is used to adjust physical parameters of material.

The DEFECTS statement is used to describe the density of defect states in the band gap. One can specify up to four distributions, two for donor-like states and two for acceptor-like states. Each type of state may contain one exponential (tail) distribution and one Gaussian distribution.

DEFECTS activate the band gap defect model and sets the parameter values. This model can be used when thin-film transistor simulations are performed using the TFT product. The Syntax DEFECTS [<parameters>]

Egd: Specifies the energy that corresponds to the Gaussian distribution peak for donor-like states. This energy is measured from the valence band edge.

Ngd: specifies the total density of donor-like states in a Gaussian distribution.

Nta: Specifies the density of acceptor-like states in the tail distribution at the conduction band edge.

Ntd: Specifies the density of donor-like states in the tail distribution at the valence band edge.

Wgd: Specifies the characteristic decay energy for a Gaussian distribution of donor-like states.

Wta: Specifies the characteristic decay energy for the tail distribution of acceptor-like states.

Wtd: Specifies the characteristic decay energy for the tail distribution of donor-like states.

SIGGAE: Specifies the capture cross-section for electrons in a Gaussian distribution of acceptor-like states.

SIGGAH: Specifies the capture cross-section for holes in a Gaussian distribution of acceptor-like states.

SIGGDE: Specifies the capture cross-section for electrons in a Gaussian distribution of donor-like states.

SIGGDH: Specifies the capture cross-section for holes in a Gaussian distribution of donor-like states.

SIGTAE: specifies the capture cross-section for electrons in a tail distribution of acceptor-like states.

SIGTAH: Specifies the capture cross-section for holes in a tail distribution of acceptor-like states.

SIGTDE: Specifies the capture cross-section for electrons in a tail distribution of donor-like states.

SIGTDH: Specifies the capture cross-section for holes in a tail distribution of donor-like states.

The a-IGZO TFT regions, materials, electrodes and work function definition are as follows:

```
# We define the gate as N.POLY
contact num=1 n.poly
# We also define a workfunction for the source and drain that
# is very close to the conduction edge
contact num=2 ALUMINUM workf=4.08
contact num=3 ALUMINUM workf=4.08
MATERIAL MATERIAL=igzo EG300=3.2 MUN=9
models fermi
# Key to the characterization of amorphous materials is the
# definition of the states within the band gap.
defects region=1 nta=2.60e20 ntd=1.55e20 wta=0.013 wtd=0.12 \
      nga=0.0 ngd=1e17 egd=3.1 wgd=0.12 \
      sigtae=1e-15 sigtah=1e-15 sigtde=1e-15 sigtdh=1e-15 \
      siggae=1e-15 siggah=1e-15 siggde=1e-15 siggdh=1e-15 \
      dfile=tftdon.dat afile=tftacc.dat numa=128 numd=128
```

3. **Numerical method selection**

Several different numerical methods can be used for calculating the solutions of semiconductor device problems. Numerical methods are given in the `METHOD` statement of the input file. Some guidelines for these methods will be given here. Different combinations of models will require ATLAS to solve up to six equations. For each of the model types, there are basically three types of solution techniques: (a) decoupled (GUMMEL), (b) fully coupled (NEWTON) and (c) BLOCK.

If any one of the methods is not choosen , ALTAS will use newton method to solve the equations.

Specification of the solution method is carried out as follows:

```
METHOD GUMMEL BLOCK NEWTON
```

4. **Solution specification**

An initial state without any voltage applied is assumed by usine the “solve init” command;

Secondly, for an applied voltage between source and drain, the equation is solved using the” `solve vdrain” command`.

Finally, variation of gate voltage is simulated by the following statement

solve vgate=0 vstep=-0.2 vfinal=-05.0 name=gate

the command outf and save used to save solution in file or structure respectively.

```
# From here we simply extract the Id-Vg characteristic
solve init
solve prev
solve vdrain=20
save outf=tft.str
log outf=tfa.log
solve vgate=0 vstep=-0.2 vfinal=-05.0 name=gate
log off
load inf=tft.str master
solve prev
log outf=tfb.log
solve vstep=0.5 vfinal=30.0 name=gate
 log off
```

5. **Results analysis**

The statement tonyplot is used to plot Id-Vg characteristic

```
#Plotting Id-Vg characteristic
tonyplot -overlay tfta.log tftexb.log
```

Figure III-5 shows the resulting graph by tonyplot command

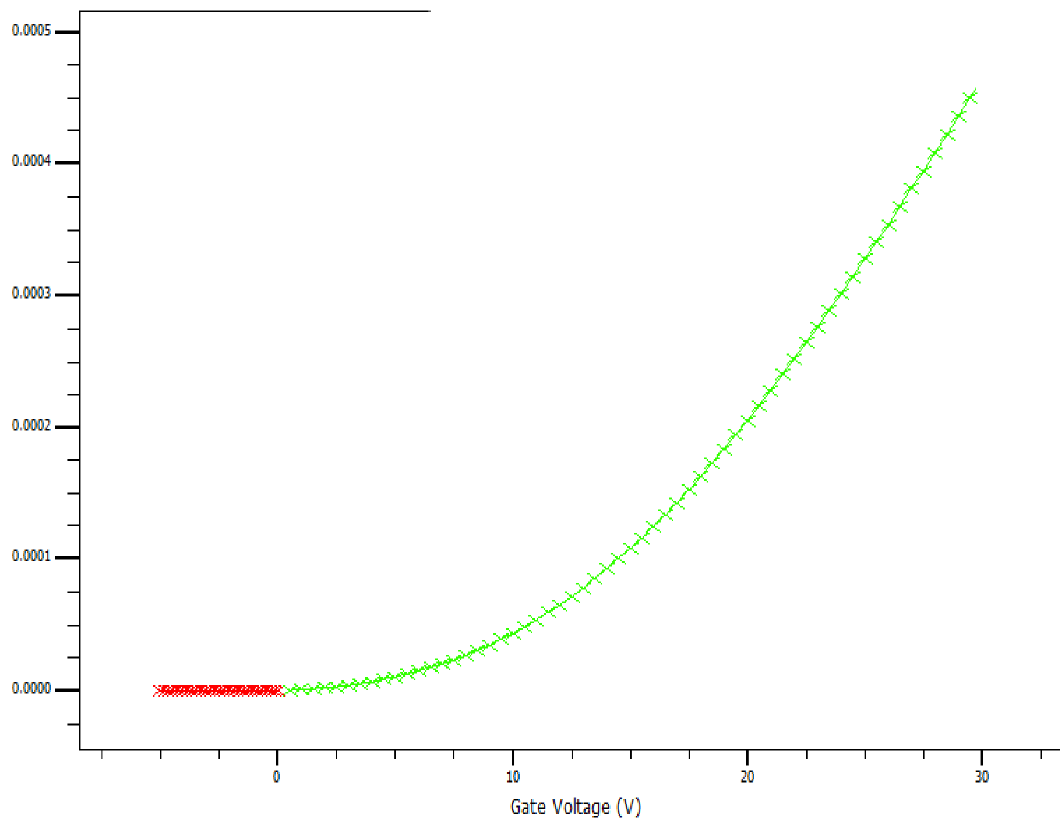

Figure III-5 I_{DS}-V_{GS} characteristics

III.3 Fabrication of thin film transistors by solution process

III.3.1 Cleaning

Before thin films deposition the substrate must be carefully cleaned to achieve better adherence and homogeny films. The cleaning steps used for glass or Si/SiO2 substrate are presented below.

Step 1 Soap cleaning

A liquid soap is used to remove oil, fingerprint from substrate.

Step 2 Acetone cleaning

Acetone is used for removing any organic compound. The glass substrate is put in warm (less than 55°C) Acetone for 10 minutes. The glass substrate is placed in methanol for 2-5 minutes.

Step 3 Cleaning by Isopropanol or isopropyl alcohol (IPA).

The substrate is immersed in Isopropanol for 10 mins.

Step 3 Deionized Water cleaning

The substrate is immersed in deionized water of 10 min.

Between each step we should put substrate in DI water for 1 mn and

it is blow dried with nitrogen gas or air flow.

Each solution can be made on a heated bath or ultrasonic bath to improve the cleaning effect.

III.3.2 Deposition a-IGZO thin films

The InGaZnO (IGZO) precursor solution was prepared by dissolving indium (III) acetate hydrate ($In(NO_3)_3 \times H_2O$ 99.99% Alfa easer), gallium(III) nitrate hydrate($Ga(NO_3)_3 \times H_2O$ 99.99% Sigma-Aldrich), and zinc acetate dihydrate($Zn(Ac)_2 \cdot 2H_2O$) 99.99% Sigma-Aldrich) 2-methoxyethanol (2-ME) solvent, and then ethanolamine (MEA) and acetylacetone (Acac) were

added to the mixed solution as sol-stabilizers to improve the solubility of the solution. The resultant solution was stirred at 60 °C for 2 h to yield a clear and transparent precursor solution. The molar ratio of In:Ga:Zn was maintained at 2:1:1. The total concentration of metal ions in the resultant solution was 0.6 M. The as-synthesized precursor solution was aged for 24 h to increase the partially homogenized solution before it was used as the coating solution. The solution was deposited on P-Si/SiO_2 substrate by spin-coating (Holmarc Ho-th-05) at a rotation speed of 3000 rpm for 30 s. The liquid film was dried at 150 °C on a hot plate for 10 min to evaporate organic compounds. The whole procedure was then repeated for 5 times. The dried film was then annealed in an oven at 350 °C for 2 h. Figure III-6 shows an illustration of the deposited a-IGZO thin films by spin coating

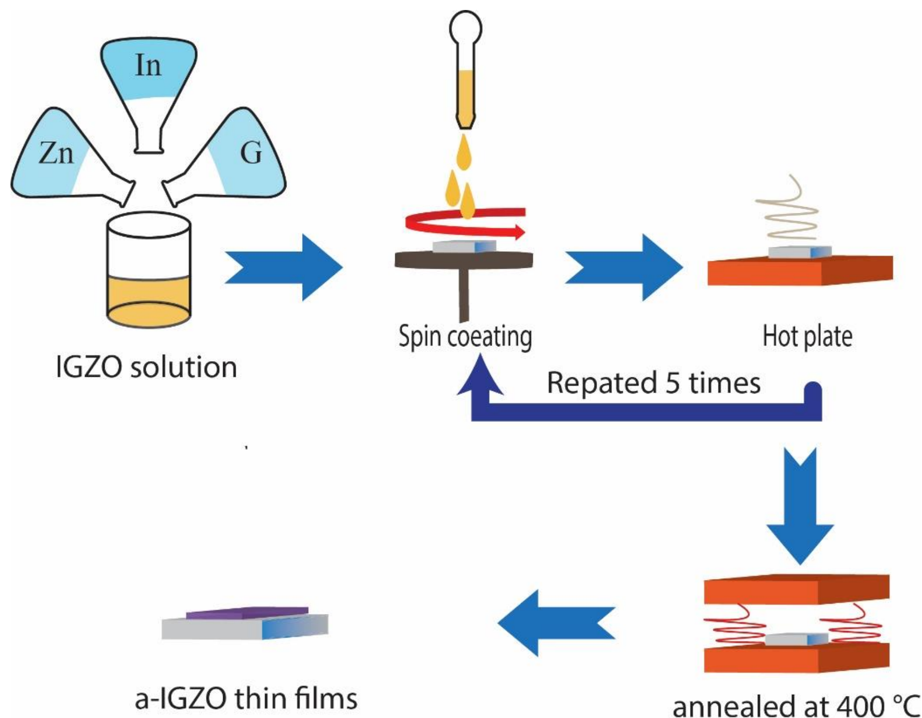

Figure III-6 Deposition a-IGZO thin films by Spin coating

III.3.3 Electrode deposition

After deposition of a-IGZO on SiO_2, a shadow mask is laid on top of the semiconductor. This mask is also used to define length and width of channel (L and W). Many methods can used to deposit the metallic contact. Thermal evaporation and DC sputtering are two methods widely used for deposited metallic contact. Figure III-7 is an illustration to show how shadow mask is used to define length and width of the metallic contact.

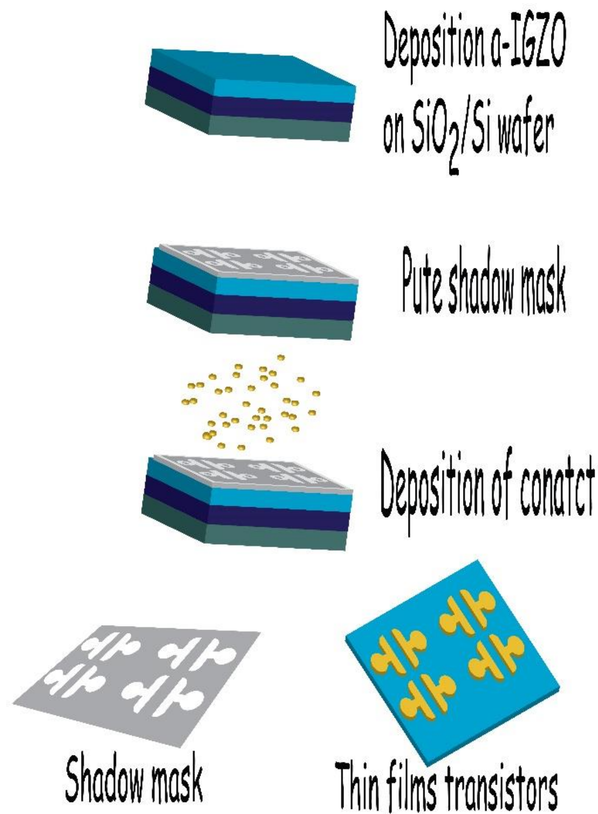

Figure III-7 The illustration showing how shadow mask is used.

III.4 References

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Chapter IV

Results and discussion

IV.1 Introduction

Amorphous oxide semiconductors (AOS) are new materials generation which can replace binary crystalline oxide semiconductors like ZnO, In_2O_3 and SnO_2. Amorphous oxide semiconductors (AOSs) such as amorphous In-Ga-Zn-O (a-IGZO) are promising for developing thin film transistors (TFTs) because of their large electron mobilities, small threshold voltage, and low temperature fabrication process. a-IGZO TFTs are expected to be used in high-resolution active-matrix organic light-emitting diode displays (AMOLEDs) and liquid crystal displays (AMLCD) [1],[2]. For design of reliable a-IGZO TFT a particular focus is required on the properties of its channel and gate insulators.

In this chapter the effect of the quality of the channel and the insulator on the TFT performance is clarified. Section 2 presents the structure, studied in this work, as well as its parameters. For the defects, their effect of on the performance of the a-IGZO TFT is detailed in section 3, especially those defects created by hydrogen which is always present, whether in the atmosphere or in the water vapor, during preparation of a-IGZO. Choosing of suitable insulator is discussed in section 4 as well as its relation to a-IGZO TFT degradation. The thickness of the channel is investigated in section 5 and its relation to degradation is clarified. In that last section we show optical and structure of a-IGZO thin films by sol-gel methods.

IV.2 TFT Structure and physical model

A 2D inverted-staggered a-IGZO TFT structure was defined in this work. Figure IV-1 shows the structure. It consists of an a-IGZO active layer (20 nm thick), an SiO_2 insulator layer (100 nm thick) and a silicon wafer substrate (n^{++}) as a gate. The length (L) and the width (W) of the channel are 30 and 180 μm, respectively. The source and the drain are 5 nm thick and made of titanium (Ti).

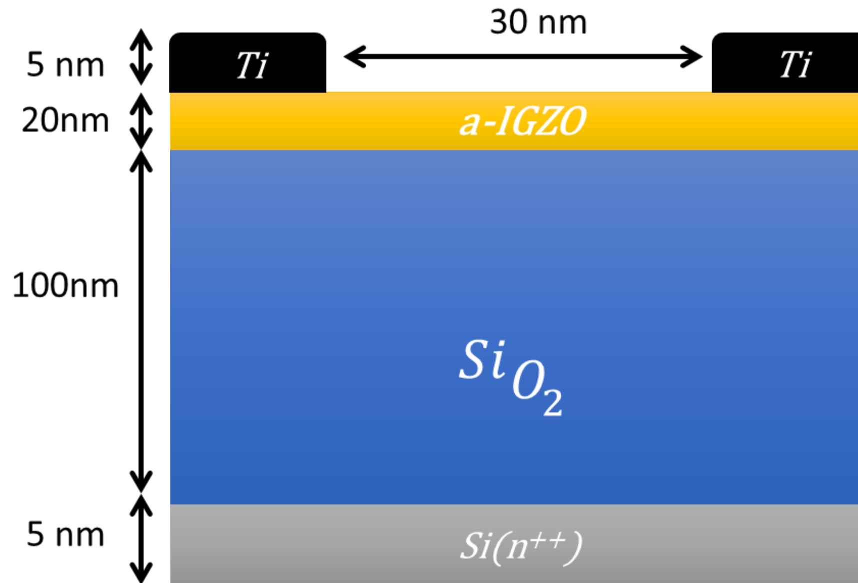


Figure IV-1: A two-dimension schematic view of the TFT structure.

Numerical simulation is a powerful tool to understand the physics of electronic devices and materials. It is also a cheap and effective tool to optimize semiconductor device design and operating mode. The Poisson and the continuity equations describe the electronic phenomena inside semiconductors and the electrical transport mechanisms involved. The numerical resolution is the best way to solve the Poisson and the continuity equation system and study the effect of the various parameters. The Poisson equation relates the electrostatic potential to the space charge density and is given by [3]:

$$div(\varepsilon \nabla \psi) = -\rho = -q(p - n + n_T - p_T + N_d) \quad \text{IV-1}$$

Where ψ is the electrostatic potential, ε is the local permittivity, ρ is the local space charge density, n and p are the free carriers densities, N_d is the n-channel doping concentration, n_T and p_T the total charge in the band gap and which will be defined later.

In the drift-diffusion model, the current densities are expressed in terms of the quasi Fermi levels ϕ_n and $\phi_p$as:

$$\vec{j_n} = q\mu_n \nabla \phi_n \quad \text{IV-2}$$

$$\vec{j_p} = q\mu_p \nabla \phi_p \quad \text{IV-3}$$

Where μ_n and μ_p are electron and hole mobilities, respectively. The quasi-Fermi levels are linked to the carries concentration and the potential through $n = n_i \exp\left(\frac{\psi-\phi_n}{K_b T}\right)$ and $p = n_i \exp\left(\frac{\psi-\phi_p}{K_b T}\right)$ where n_i is the effective intrinsic concentration and T is the lattice temperature.

The continuity equations for both electrons and holes, are expressed in the dynamic regime as [4]:.

$$\frac{\partial n}{\partial t} = \frac{1}{q} div\vec{j_n} + G_n - R_n \quad \text{IV-4}$$

$$\frac{\partial p}{\partial t} = \frac{-1}{q} div\vec{j_p} + G_p - R_p \quad \text{IV-5}$$

In the stationary regime $\frac{\partial n}{\partial t} = \frac{\partial p}{\partial t} = 0$

$\vec{j_n}$ and $\vec{j_p}$ are the electron and hole current densities, G_n and G_p are the generation rates for electrons and holes which are neglected in this study (no external generation). R_n and R_p are the total recombination rates for electrons and holes in Gaussian and tail states, and q is the electron charge. The physical parameters of the different layers of the a-IGZO TFT are presented in Table IV-1 [5].

Table IV-1: The physical parameters of the different layers of the a-IGZO TFT used in this work

Layer	Parameters	Designation	Value
a-IGZO (channel, n-type)	$N_C(cm^{-3})$	Effective DOS in the conduction band	5×10^{18}
	$N_V\ (cm^{-3})$	Effective DOS in the valence band	5×10^{18}
	$E_g\ (eV)$	Band gap	3.05
	$\chi\ (eV)$	Electronic affinity	4.16
	ε	Relative permittivity	10
	$L(\mu m)/W(\mu m)/T(nm)$	Length/Width/Thickness	30/180/20
	$\mu_n\ (\frac{cm^2}{V\ s})$	Free electron mobility	15

	$\mu_p\ (\frac{cm^2}{V\ s})$	Free hole mobility	0.1
SiO_2 (Insulator)	$E_g(eV)$	Band gap	9
	ε_{ox}	Relative permittivity	3.9
	$d_{ox}\ (nm)$	Thickness	100
Source and drain contacts (Ti)	$d(nm)$	Thickness	5
	$\Phi_{Ti}(eV)$	Work function	4.33
Gate Si ploy (n^{++})	$d(nm)$	Thickness	5
	$\Phi_{p-Si}(eV)$	Work function	4.58

IV.3 Effect of deep defects on the performance of amorphous indium gallium zinc oxide thin film transistor

The stability of a-IGZO TFTs, defined by the threshold voltage shift (ΔV_{th}), is a crucial issue for its practical applications. There is an intense ongoing research work investigating possible causes of the threshold voltage shift (ΔV_{th}). One of such possible causes is oxygen vacancies near the conduction band minimum (CBM) states [6]–[8]. The oxygen vacancies are the reason for negative V_{th} shift. The presence of hydrogen creates defect states near the valance band maximum (VBM) [9], [10]. The oxygen disorder is origin of deep defects states [11]. The high density subgap defects in a very deep energy region just above the valance band maximum (near-VBM states) may be another cause of the instability. However, it is not yet known what kind of influence defect near VBM states have on the device performance such as threshold voltage shift. In this section a detailed numerical simulation is carried out to understand the effect of defects near VBM on the a-IGZO TFT performance. In particular each possible defect type supposed to be created is introduced in the a-IGZO channel (channel material of the TFT) and its effect on the electrical TFT characteristics is studied. This is carried out by numerical simulation using ATLAS software of SILVACO (detailed in chapter 3).

The validity of these assumptions is based on the shape found in the TFT transfer characteristics compared to experimental measurements by other workers. The aim of this work is to establish the nature of near VBM defects created by hydrogen and oxygen disorder. The applied gate voltage ranges from -5 to 20 V for a 0.1 V drain voltage and the transfer characteristics ($I_{DS} - V_{GS}$) are plotted in a semi-logarithmic scale.

n_T and p_T (of equation IV.1) are defined by n_{tail}, p_{tail}, n_{ga} and p_{gd}.The different charge states (negative and positive) at tail states and other gap states are given by [3]:

$$n_T = n_{tail} + n_{ga} = \int_{E_v}^{E_c} g_{ct}^A f_{ct}^n(E)dE + g_G^A f_{AG}^n(E)dE \quad \text{IV-6}$$

$$n_T = p_{tail} + p_{gd} = \int_{E_v}^{E_c} g_{vt}^D f_{vt}^p(E)dE + g_G^D f_{DG}^p(E)dE \quad \text{IV-7}$$

Where the occupancies by the different charge states are given by [12], [13]:

$$f_{t_{TD}}(E,n,p) = \frac{v_p\sigma_{TDH}p + v_n\sigma_{TDE}n_i\exp\left(\frac{E-E_i}{kT}\right)}{v_n\sigma_{TDE}(n+n_i\exp\left(\frac{E_i-E}{kT}\right) + v_p\sigma_{TDH}(p+n_i\exp\left(\frac{E_i-E}{kT}\right)} \quad \text{IV-8}$$

$$f_{t_{GD}}(E,n,p) = \frac{v_p\sigma_{GDH}p + v_n\sigma_{GDE}n_i\exp\left(\frac{E-E_i}{kT}\right)}{v_n\sigma_{GDE}(n+n_i\exp\left(\frac{E_i-E}{kT}\right) + v_p\sigma_{GDH}(p+n_i\exp\left(\frac{E_i-E}{kT}\right)} \quad \text{IV-9}$$

$$f_{t_{TA}}(E,n,p) = \frac{v_n\sigma_{TAE}n + v_p\sigma_{TAH}n_i\exp\left(\frac{E_i-E}{kT}\right)}{v_n\sigma_{TAE}(n+n_i\exp\left(\frac{E-E_i}{kT}\right) + v_p\sigma_{TAH}(p+n_i\exp\left(\frac{E_i-E}{kT}\right)} \quad \text{IV-10}$$

$$f_{t_{GA}}(E,n,p) = \frac{v_n\sigma_{GAE}n + v_p\sigma_{GAE}n_i\exp\left(\frac{E_i-E}{kT}\right)}{v_n\sigma_{GAE}(n+n_i\exp\left(\frac{E-E_i}{kT}\right) + v_p\sigma_{GAH}(p+n_i\exp\left(\frac{E_i-E}{kT}\right)} \quad \text{IV-11}$$

For amorphous materials the gap states are composed of tail states acceptors and donors of which the energy distribution decreases exponentially. Extended states and other gap states, acceptors and donors $g_{ct}^A(E)$, $g_G^A(E)$, $g_{vt}^D(E)$, $g_G^D(E)$ have Gaussian energy distribution. Usually the a-IGZO density of gap states is formed by donor tail state $g_{vt}^D(E)$ with exponential decay from E_v, a donor a Gaussian distribution $g_G^D(E)$ with a maximum located at 2.9 eV from E_v and another narrow acceptor tail state $g_{ct}^A(E)$ near E_c [5], [14].For an exponential tail distribution, the DOS is

described by its valance edge intercept densities N_{TD}, characteristic decay energy W_{TD}. These distributions are expressed as follows:

$$g_{vt}^{D}(E) = N_{td} \exp\left(\frac{E_v - E}{W_{TD}}\right) \tag{IV-12}$$

$$g_{G}^{D}(E) = N_{gd} \exp\left(\frac{-(E - Egd)^2}{W_{GD}}\right) \tag{IV-13}$$

$$g_{ct}^{A}(E) = N_{ta} \exp\left(\frac{E - E_c}{W_{TA}}\right) \tag{IV-14}$$

Figure IV-2 shows the different components of the density of states in a-IGZO.

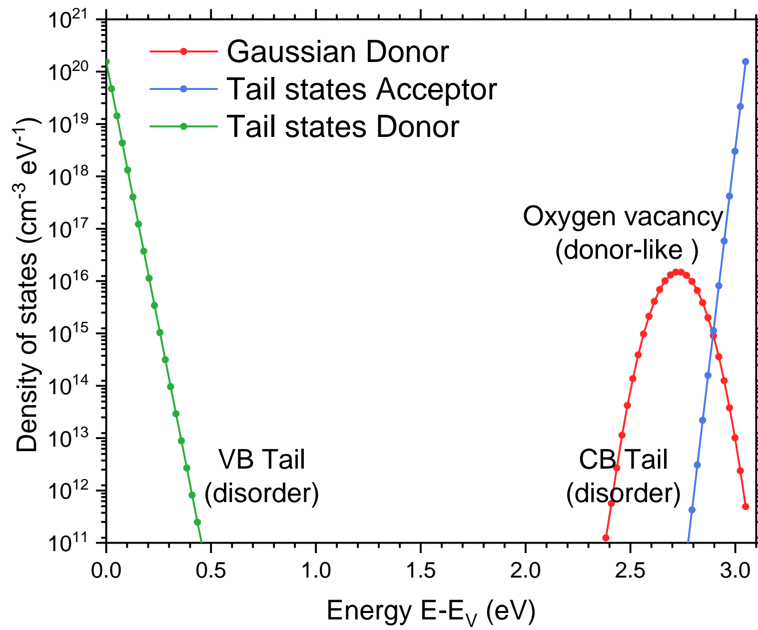


Figure IV-2: Density of states in a-IGZO

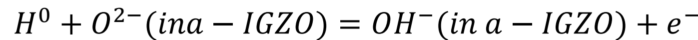
R_n and R_p (equation IV.15) are supposed to be equal, for simplicity, and are given by [15]:

$$R_n = R_p = \int_{E_v}^{E_c} (np - n_i^2) \left\{ \frac{v_n \sigma_{TAE} n + v_p \sigma_{TAH} n_i \, exp\left(\frac{E_i - E}{kT}\right)}{v_n \sigma_{TAE} (n + n_i \, exp\left(\frac{E - E_i}{kT}\right) + v_p \sigma_{TAH} (p + n_i \, exp\left(\frac{E_i - E}{kT}\right))} \right\}$$
$$+ \left\{ \frac{v_n \sigma_{GAE} n + v_p \sigma_{GAE} n_i \, exp\left(\frac{E_i - E}{kT}\right)}{v_n \sigma_{GAE} (n + n_i \, exp\left(\frac{E - E_i}{kT}\right) + v_p \sigma_{GAH} (p + n_i \, exp\left(\frac{E_i - E}{kT}\right))} \right\}$$
$$+ \left\{ \frac{v_p \sigma_{TDH} p + v_n \sigma_{TDE} n_i \, exp\left(\frac{E - E_i}{kT}\right)}{v_n \sigma_{TDE} (n + n_i \, exp\left(\frac{E_i - E}{kT}\right) + v_p \sigma_{TDH} (p + n_i \, exp\left(\frac{E_i - E}{kT}\right))} \right\}$$
$$+ \left\{ \frac{v_p \sigma_{GDH} p + v_n \sigma_{GDE} n_i \, exp\left(\frac{E - E_i}{kT}\right)}{v_n \sigma_{GDE} (n + n_i \, exp\left(\frac{E_i - E}{kT}\right) + v_p \sigma_{GDH} (p + n_i \, exp\left(\frac{E_i - E}{kT}\right))} \right\} \quad \text{IV-15}$$

IV.3.1 Near valance band defects

The presence of hydrogen as an impurity in a-IGZO has not received much attention although it was recently found that its concentration may be as high as $10^{17} cm^{-3}$ [10]. Evidently, this high value will have a significant effect on the TFT performance and hence cannot be neglected.

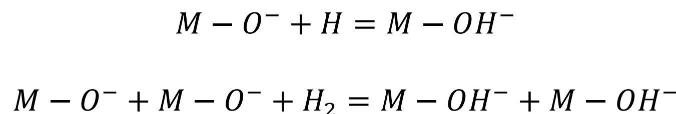
Initially it was supposed that the presence of hydrogen plays a dopant role and hence increases the free electron density in a-IGZO [16]. When hydrogen reacts with charged oxygen; free electrons are created in a-IGZO according to the reaction [16], [17]:



$$H^0 + O^{2-}(ina - IGZO) = OH^-(in\, a - IGZO) + e^-$$

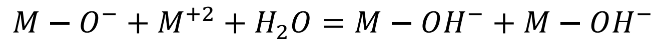
This can enhance the conductivity and hence the threshold voltage.

The presence of hydrogen may induce threshold instability of the TFT since it creates defect states near VBM. Takatoshi Orui and co-workers suggested that the origin of the near VMB states is the OH bond [18]. OH may originate from the presence of H, H_2 or H_2O in the deposition chamber. The adsorption/desorption of hydrogen atom (H), hydrogen gas (H_2) or water (H_2O), at the surface of the a-IGZO results from the following chemical reactions [19]–[22]:



$$M - O^- + H = M - OH^-$$

$$M - O^- + M - O^- + H_2 = M - OH^- + M - OH^-$$



$$M - O^- + M^{+2} + H_2O = M - OH^- + M - OH^-$$

In the three previous reactions M is the metal which may be indium (In), zinc (Zn) or gallium (Ga).

a-IGZO have amorphous structure when the atoms have random position the local variation in the oxygen plus weak band of oxygen create deep defects by expansion tail valance band [11], [18].

To study effect near VB defects we have supposed three possible processes. In the first one, expansion in tail creates donor defect states near VBM. The second possible effect is exitance near VB defects a decrease in the free carrier mobility. The third assumption is that hydrogen creates acceptor defect states near VBM.

IV.3.1.a Effect of donors near the valance band (donor tail band):

In the first assumption it is assumed that disorder in oxygen atoms creates a donor defect near VMB. This means expansion in the tail donor. The tail donor is defined by its energy decay (W_{td}) and its density (N_{td}). We examine the effect of W_{td} and N_{td} on the transfer characteristics and the output parameters.

IV.3.1.b Effect of the decay energy

We examined how is the a-IGZO TFT affected by the decay energy (W_{td}). W_{td} is varied from 0.01 to 0.20 eV. The obtained transfer characteristics are presented in Figure IV-3. The transfer characteristics are not affected by the decay energy (W_{td}). The threshold voltage V_{th}, the on-current I_{on}, the ratio I_{on}/I_{off} and the sub-threshold swing SS are 1.7V, 4.28×10^{-06}A, 3.26×10^{11} and 0.13 Vdec^{-1} respectively. Those results are close to measured values of [5], [23], [24]. It is observed that the simulated off-state current is much smaller than the experimental value which is around 0.1-1 pA. This may be due to interface states which were not considered in this work [25].

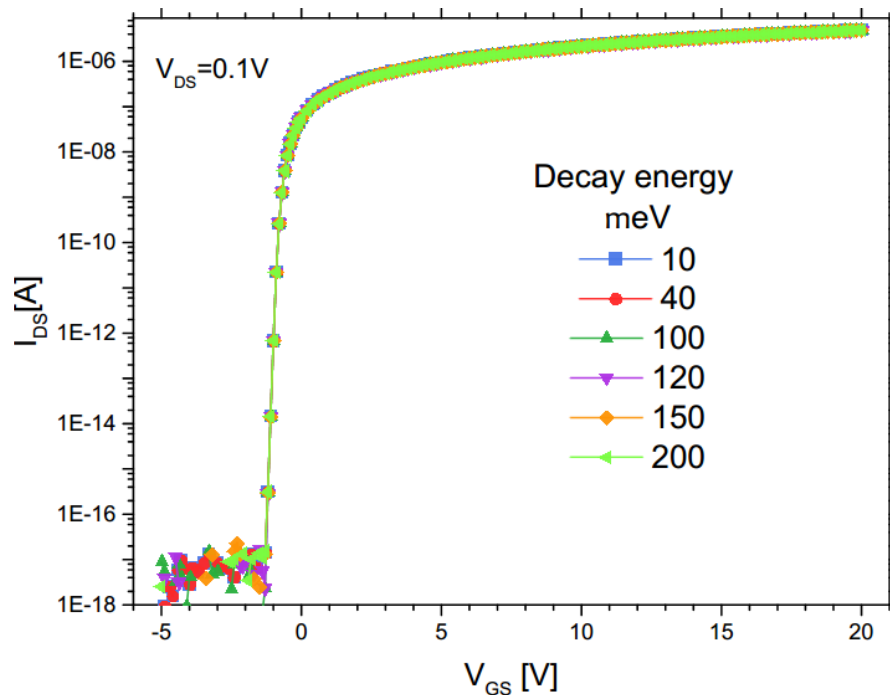


Figure IV-3: The transfer characteristics for different decay energies.

IV.3.1.c Effect of the tail donor density

The value of the tail donor density N_{td} was varied from 1.55×10^{16} to 1.55×10^{22} cm^{-3}eV^{-1} by a step of a decade. The transfer characteristics are presented in Figure IV-4. The transfer characteristics are not affected by the tail donor density (N_{td}). The threshold voltage V_{th}, the on-current I_{on}, the ratio I_{on}/I_{off} and the sub-threshold swing SS are 1.7 V, 4.2×10^{-06} A, 3.26×10^{11} and 0.13 Vdec^{-1} respectively. The density of the tail states, again, has no effect on the transfer characteristics and output parameters. In summary, the donor sates near the valance band maximum have no effect on the transfer characteristics and hence the output parameters because the Fermi level is located in the upper energy level approaching the conduction band edge in the n-type IGZO. The clear near the donor states near valence band do not have effect on transfer characteristics.

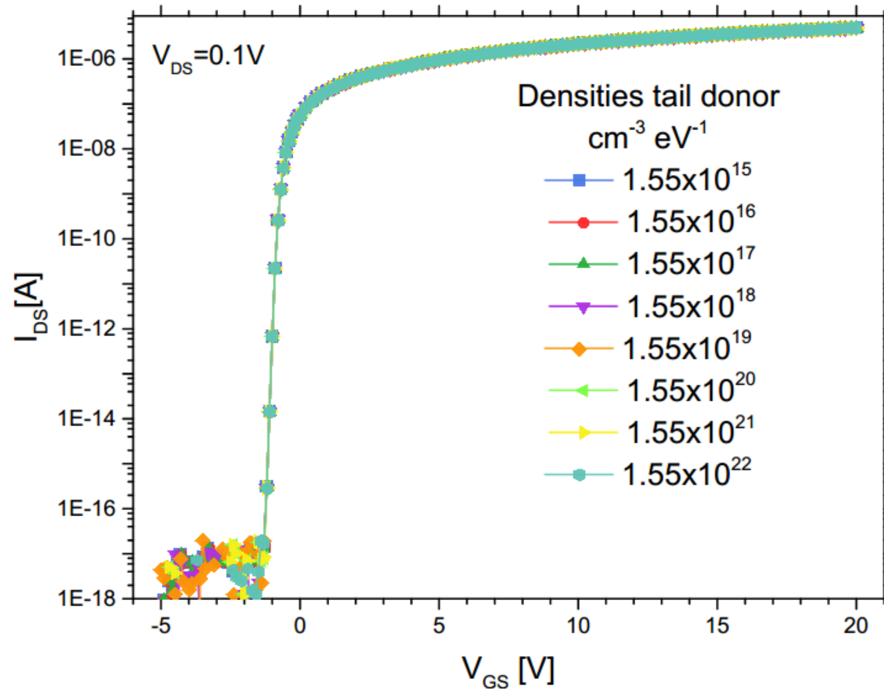


Figure IV-4: The effect of the donor tail densities on the TFT transfer characteristics.

IV.3.1.d Effect of the Gaussian acceptor

Now we suppose that hydrogen creates a Gaussian near VMB. The acceptor like Gaussian is described as:

$$g_G^A(E) = N_{ga} \exp\left(\frac{-(E-E_{ga})^2}{W_{ga}}\right) \qquad \text{IV-16}$$

where $N_{ga}$is the acceptor density, E_{ga} is the energy position and W_{ga} is the energy width. The different parameters of the Gaussian effect on the transfer characteristics and output parameters are examined. Figure IV-5 shows the DOS distribution of defects when hydrogen creates Gaussian acceptors near VBM.

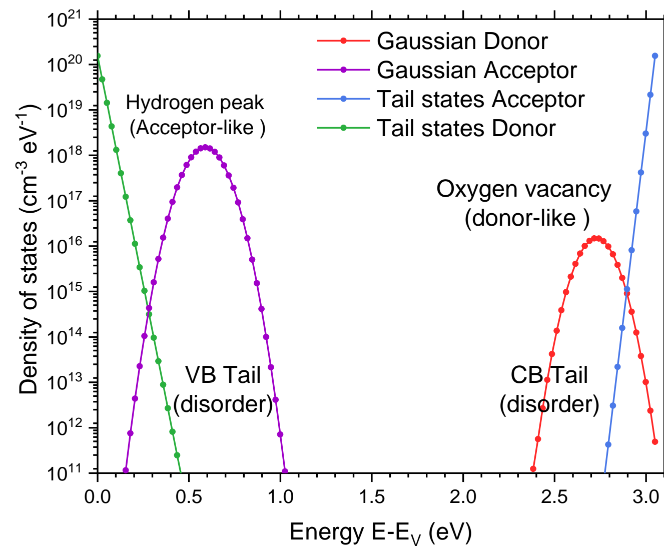


Figure IV-5: Density of states in a-IGZO with Gaussian acceptor states.

IV.3.1.e Effect of the Gaussian acceptor density

In this section the Gaussian acceptor density was varied from 1.55×10^{15} to1.55×10^{19} $cm^{-3}eV^{-1}$ by a step of a decade while the donor band tail density and the decay energy are kept fixed at 1.55×10^{20} $cm^{-3}eV^{-1}$ and 0.12 eV respectively. The effect on the transfer characteristics and output parameters are shown in Figure IV-6 and Table IV-2 respectively.

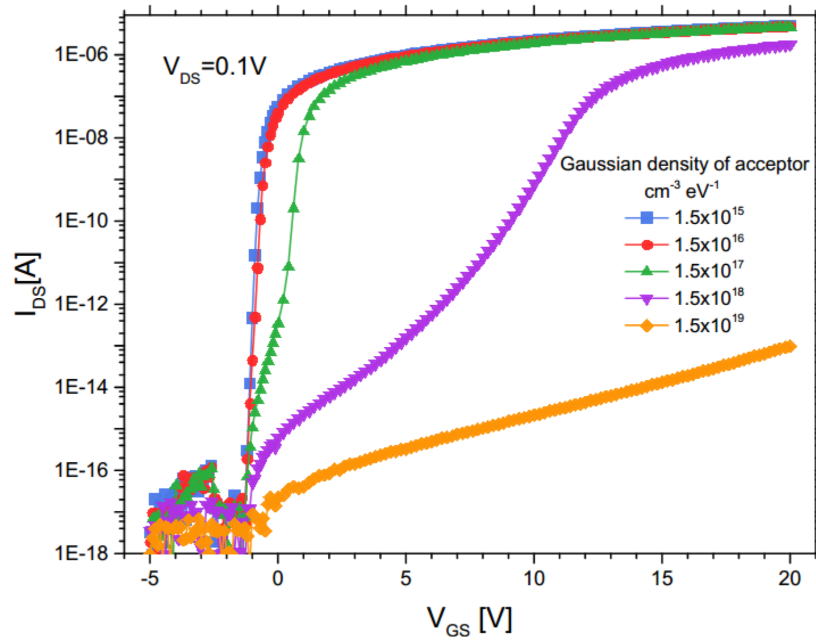


Figure IV-6: The effect of Gaussian acceptor density on the TFT transfer characteristics.

Table IV-2: The effect of the density of the Gaussian acceptor on the output parameters of the TFT.

Density *(cm^{-3}eV^{-1})*	$V_{th}(V)$	$I_{on}(A)$	I_{on}/I_{off}	$SS(Vdec^{-1})$
$\mathbf{1.5\times10^{15}}$	1.8	4.27×10^{-06}	3.47×10^{11}	0.15
$\mathbf{1.5\times10^{16}}$	1.9	4.25×10^{-06}	3.27×10^{11}	0.18
$\mathbf{1.5\times10^{17}}$	2.7	3.97×10^{-06}	3.08×10^{11}	0.3
$\mathbf{1.5\times10^{18}}$	12.5	1.19×10^{-06}	6.54×10^{10}	1.56

The Gaussian acceptor density has an influence on the TFT transfer characteristics and its output parameters. In particular, the threshold voltage positive shift (ΔV_{th}) surpasses 10 V with increasing values of acceptor density defects. SS increases which deteriorates the TFT performance. I_{on} and I_{on}/I_{off} are degraded with the acceptors density increase. The same behavior

was observed in the experimental work of [20], [22], [26]–[29]. This result clearly shows that the origin of positive shift (ΔV_{th}) is acceptors states near VBM. We notice that that density of acceptor states cannot surpass 6.5×10^{18} when a-IGZO has not an ideal behavior. The same result is observed by the experimental work of Kay Domen [30]. He has attributed this to the diffusion of hydrogen in a-IGZO which has an absorption limitation.

IV.3.1.f Effect of the energetic position of the Gaussian acceptor

Measurement by HX-PES [20] shows that the position of a Gaussian can be at 0.3 to 1.5 eV from E_V. We are varied its Gaussian position between 0.3 and 1.5 eV by a step of 0.3 eV while its density is fixed at 1.5×10^{16} cm^{-3}eV^{-1} while the other parameters are the same as in section IV.3.1.d. The results are shown in Figure IV-7. It is observed that the position of the Gaussian acceptor has no effect on the TFT transfer characteristics. The TFT parameters V_{th}, I_{on}, I_{on}/I_{off} and SS are 1:9V, 4.25×10^{-6}A,3.27×10^{11} and 0.18 V dec^{-1} respectively.

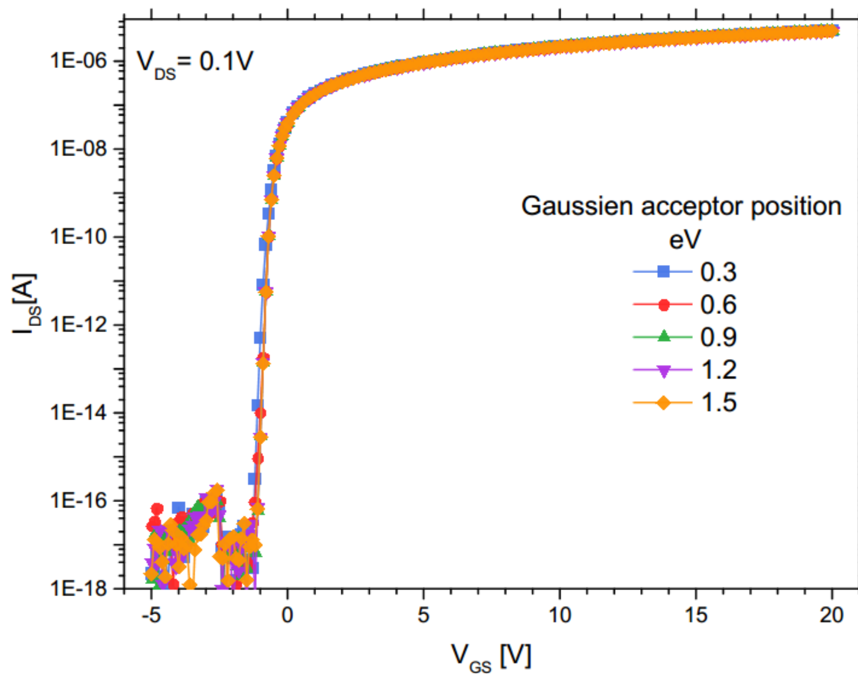


Figure IV-7: The effect of the energetic position of the Gaussian acceptor on the TFT transfer characteristics.

IV.3.1.g Effect of the Gaussian acceptor energy width

The width of the Gaussian acceptor is another important parameter. It was varied from 0.1 to 0.3 eV by a 0.1 eV step while its position is fixed at 0.3 eV from E_V. The other values are the same as in section IV.3.1.f. The results are shown in Figure IV-8. It is observed that the width of the Gaussian acceptor has no effect on the TFT transfer characteristics. The TFT parameters V_{th}, I_{on}, I_{on}/I_{off} and SS are 1.9 V, 4.25×10^{-6}A, 3.27×10^{11} and 0.18 Vdec^{-1} respectively.

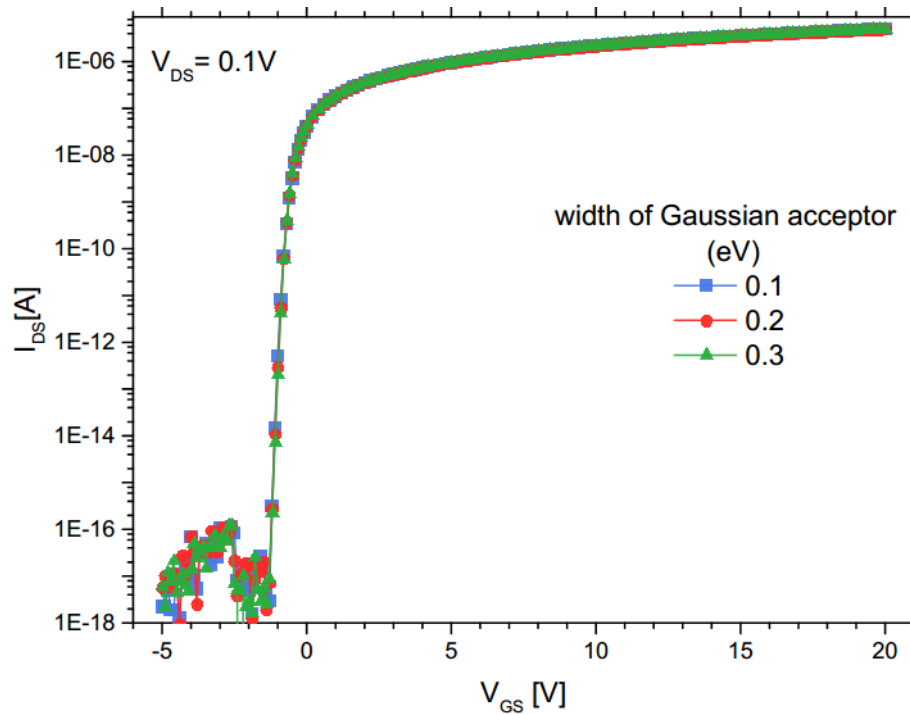


Figure IV-8: The effect of Gaussian acceptor width on the TFT transfer characteristics.

IV.3.2 Effect of the electron mobility

The defect may have an influence on the mobility by improvement or deterioration. Experimental studies show that states near the valance band induce a degradation of the electron mobility [18], [20]. To study the mobility effect on the transfer characteristics and the output parameters, the values in section IV.3.1.a are used to define the defects in the band gap of a-IGZO and the degraded value of the electron mobility was changed from 15 to 07 cm^{2}V^{-1}s^{-1} by a step of 2 cm^{2}V^{-1}s^{-1}. The simulation results are shown in Figure IV-9 and Table IV-3.

Table IV-3: The effect of mobility on the output parameters of the TFT.

Mobility $cm^{-2}s^{-1}V^{-1}$	$V_{th}(V)$	$I_{on}(A)$	I_{on}/I_{off}	$SS(Vdec^{-1})$
15	1.9	4.25×10^{-06}	3.27×10^{11}	0.18
13	1.9	3.43×10^{-06}	2.86×10^{11}	0.18
11	1.9	2.90×10^{-06}	2.42×10^{11}	0.18
09	1.9	2.83×10^{-06}	1.98×10^{11}	0.18
07	1.9	1.85×10^{-06}	1.54×10^{11}	0.18

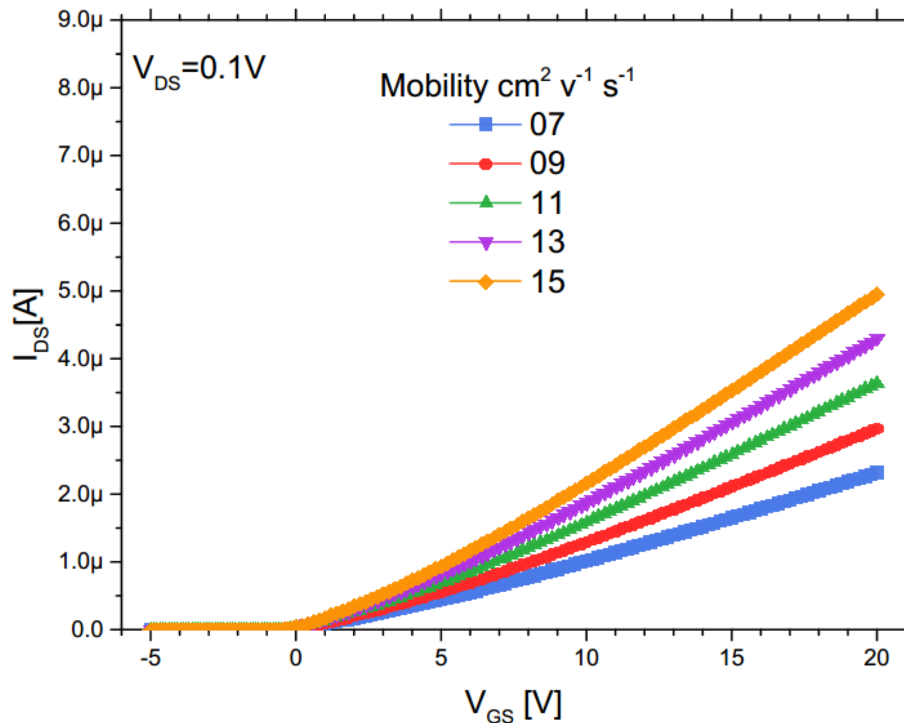


Figure IV-9: The effect of the degradation of the mobility on the transfer characteristics of the TFT.

The transfer and output characteristics are sensitive to the electron mobility degradation. When the electron mobility is degraded from 15 to 07 $cm^2V^{-1}s^{-1}$, I_{on} decreases with decreasing electron mobility. I_{on}/I_{off} ratio follows a similar behavior since I_{on} is reduced. SS and V_{th} are

unaffected by the electron mobility degradation. It is therefore is clear that the mobility degradations are not a critical issue on performance of a-IGZO TFTs.

IV.4 Simulation the influence of the gate dielectrics in amorphous indium-gallium-zinc oxide thin film transistors reliability

Found an optimal insulator of the gate from the channel of the a-IGZO TFT [36]. As an important part of the TFT, the gate insulator plays a crucial role in its performance. Various gate insulators, such as, silicon dioxide (SiO_2) [37], silicon nitride (Si_3N_4) [38], [39] , Aluminum oxide (Al_2O_3) [40], [41], and hafnium oxide (HfO_2) [36], [42] have been investigated for use in TFTs. In this section, the effect of the insulator type on the operation of a-IGZO TFT and the threshold (V_{th}) instability. The insulators compared are SiO_2, Si_3N_4, Al_2O_3 and HfO_2. The other parameters such as on-current (I_{on}), field effect mobility (μ_{FE}), threshold voltage (V_{th}), subthreshold swing (SS), on-to-off current ratio (I_{on}/I_{off}), and threshold shift (ΔV_{th}). The numerical study explains the effect of insulators without contribution of other parameters such as interface states between semiconductors and insulators or fixed charge in insulator material which we cannot control in experimental work. Furthermore, numerical simulation decreases the cost and time required by measurement and it is obvious that a rigorous study of insulators and instability effects is very difficult to be achieved experimentally.

IV.4.1 TFT Structure

Four structures with the same parameters are designed. The difference in the four structures is the insulator layer. SiO_2, Si_3N_4, Al_2O_3 and HfO_2 are the four different insulators. The s a-IGZO TFT structure studied in this work is the same as in Figure IV-1 but the gate insulator is variable. The physical parameters are presented in Table I-1 and Table IV-4 applied in the poison and the

continuity equation. This last is solved for different applied gate voltages ranging from -10 to 20 V. The drain voltage was fixed 0.1 V and the transfer characteristic ($I_{DS} - V_{GS}$) is plotted on a semi-logarithmic scale.

Table IV-4: The physical parameters of the different layers insulators layers for a-IGZO TFT

Layer	Parameters	Designation	Value	Reference
SiO_2	$E_g(eV)$	Band gap	9.0	[43]
	ε_{ox}	Relative permittivity	3.9	[43]
Si_3N_4	$E_g(eV)$	Band gap	5.3	[43]
	ε_{ox}	Relative permittivity	7.5	[43]
Al_2O_3	$E_g(eV)$	Band gap	8.8	[44]
	ε_{ox}	Relative permittivity	9.3	[44]
HfO_2	$(eV)E_g$	Band gap	6.0	[45]
	ε_{ox}	Relative permittivity	22.0	[45]

IV.4.2 The effect of insulator on operation a-IGZO TFTs

To understand the effect of insulator on operation a-IGZO TFTs, the Poisson and continuity equations are solved by TCAD using the materials properties presented in Table IV-1 and Table IV-4. The defects in the band gap have values of $1.55 \times 10^{20}\ cm^{-3}eV^{-1}$ for tail band acceptors and donors, Gaussian donor states have a density/per energy of $5 \times 10^{17} cm^{-3}eV^{-1}$ for an applied gate voltage ranging from -10 to 20 V for 0.1V drain voltage and the transfer characteristic ($I_{DS} - V_{GS}$) is plotted on a linear and semi-logarithmic scales and are shown in Figure IV-10.

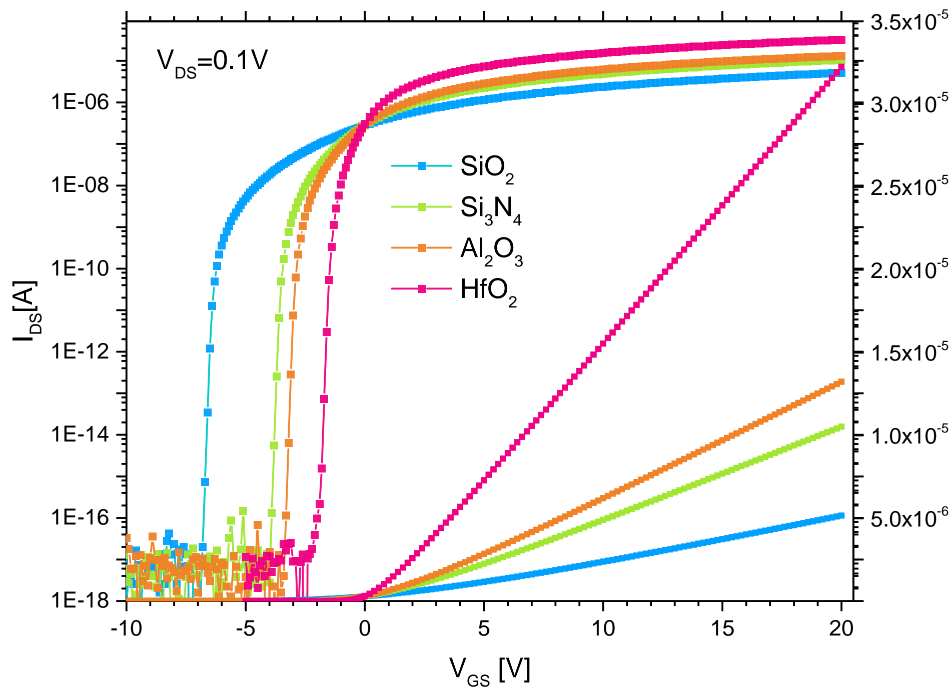


Figure IV-10:The transfer characteristics for different insulators layers

The listed threshold voltage V_{th} and field-effect mobility μ_{eff} were extracted from linear plot

where I_{DS} is the drain current, V_{GS} is the gate bias voltage, V_{DS} is the drain bias voltage, C_{ox} is the gate insulator capacitance per unit area, and W and L are the TFT channel width and length, respectively.

The extrapolated threshold voltages values were -1.07; - 0.68; -0.43 and 0.23 V for SiO_2, Si_3N_4, Al_2O_3 and HfO_2 respectively. All insulators in this work show low V_{th} value. Relatively low gate voltage is required in TFT application. The negative value of V_{th} is due to high donor concentration near the conduction band which is around $5 \times 10^{17} cm^{-3} eV^{-1}$. The most important parameter of TFT performance is channel mobility. Effective channel mobilities μ_{eff}, as calculated from the linear region of the transfer characteristics for typical devices. The field effect mobility for SiO_2, Si_3N_4, Al_2O_3 and HfO_2 is found to be 7.87 , 8.21, 9.50 and 13.73 $cm^2\ s^{-1}\ V^{-1}$ respectively. It is obvious that high value of the field effect mobility means fast and high performance of TFT. The

low gate voltage and high field effect mobility are required and attractive for high speed TFT application.

subthreshold swings of a-IGZO TFTs with SiO_2, Si_3N_4, Al_2O_3 and HfO_2 are estimated to 0.13, 0.11, 0.10 and 0.09 $Vdec^{-1}$, respectively. SS shows a small variation with the type of the insulator. SS related to interface and bulk defects which are both unaffected. This variation explicates by dielectric constants for each layer. I_{on} and I_{on}/I_{off} values are: for IGZO/SiO_2 TFT; $I_{on} = 4.44 \times 10^{-6}$A and $I_{on}/I_{off} = 5.87 \times 10^{11}$, for a-IGZO/$Si_3N_4$ TFT; I_{on}=9.10×10^{-6}A and $I_{on}/I_{off} = 1.43 \times 10^{12}$, for a-IGZO/$Al_2O_3$ TFT; I_{on}=1.5×10^{-5} A and I_{on}/I_{off}=2.07×10^{12}, for a-IGZO/HfO_2; I_{on}=2.81×10^{-6} A and I_{on}/I_{off}=5.06×10^{12}. Both a-IGZO/Al_2O_3 TFT and a-IGZO/HfO_2 show high values of I_{on} and I_{on}/I_{off} which make Al_2O_3 and HfO_2 a better choice compared with SiO_2 and Si_3N_4. The high I_{on} for high k insulators is expected due to high μ_{eff} as shown Equation *II-7*.The TFT with the HfO_2 dielectrics shows superior electrical characteristics compared to the other insulators TFTs, such as field effect mobility, I_{on}/I_{off}-current ratio, and subthreshold swing, which can be seen in Table IV-5.

Table IV-5: The effect of different insulators layer on the output parameters of the TFT.

	SiO_2	Si_3N_4	Al_2O_3	HfO_2
V_{th} (V)	-1.7	-0.6	-0.43	0.23
$\mu_{FE}(cm^2V^{-1}s^{-1})$	7.87	8.21	9.50	13.73
$I_{on}(A)$	4.44×10^{-06}	9.10×10^{-06}	1.15×10^{-05}	2.81×10^{-05}
I_{on}/I_{off}	5.87×10^{11}	1.43×10^{12}	2.07×10^{12}	5.06×10^{12}
$ss\ (Vdec^{-1})$	0.13	0.11	0.10	0.09

It is observed that the insulator type influence on the TFT performance depends on the relative permittivity. When the relative permittivity is higher the TFT performance is better. To understand this influence, internal parameters such the electron concentration and the electric field are extracted. The electron concentration is extracted, for different V_{GS} and V_{DS}=0.1 V, for the different insulators. The electric field is extracted, for different V_{GS} and V_{DS}=0.1 V at the gate-insulator interface, for the different insulators. The extracted electron concentration and field electric are shown in Figure IV-11 and Figure IV-12 respectively.

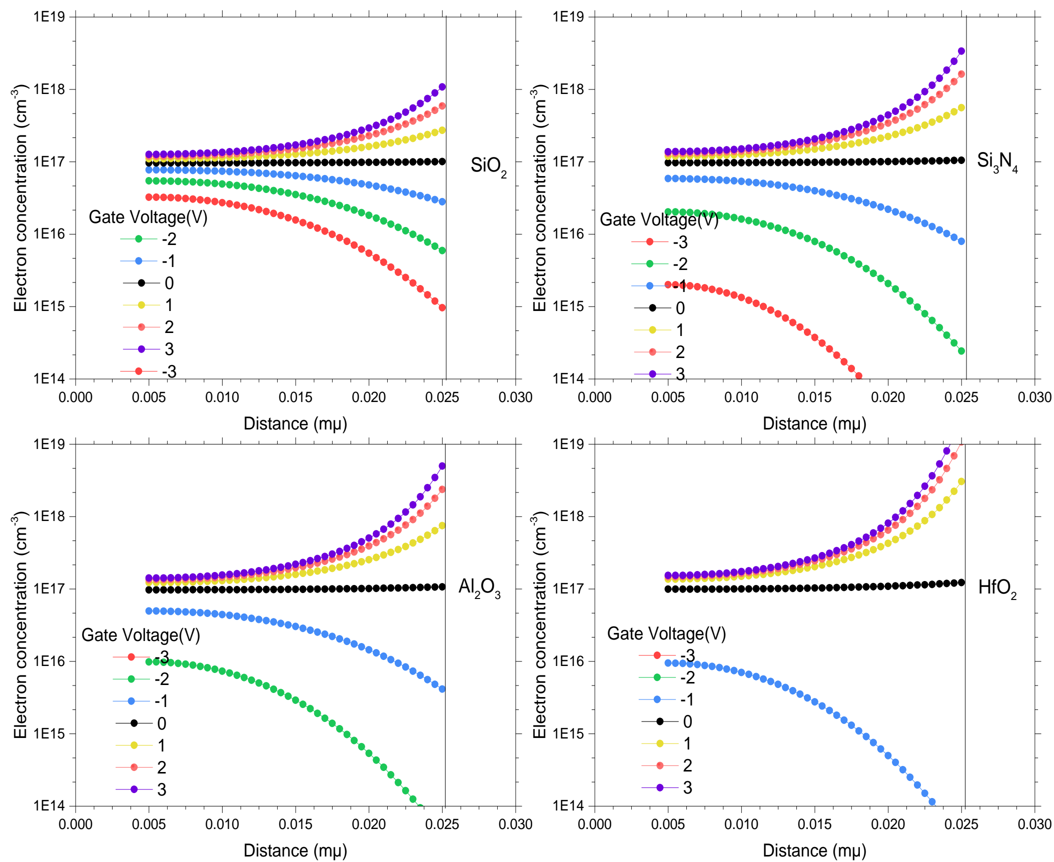


Figure IV-11:The electron concentration, for different gate voltages and V_{DS}=0.1 V, for the insulators

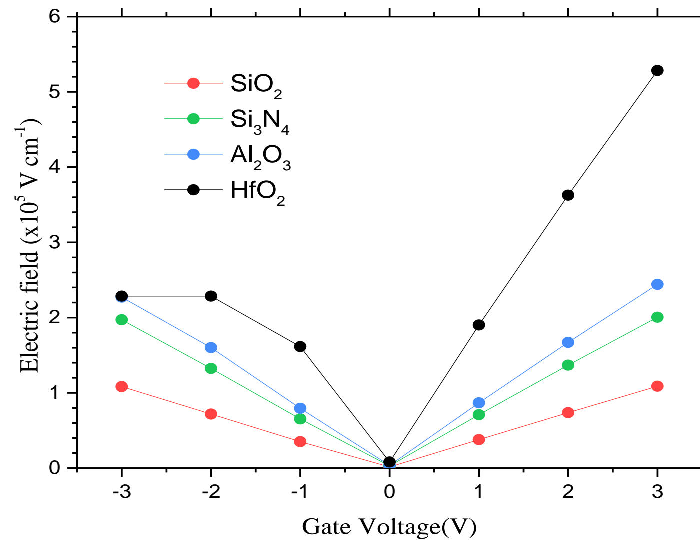


Figure IV-12: The Electric field for different gate insulators.

Figure IV-11 represents the electron concentration in the transistor channel for the four insulators, for several gate voltages and drain voltage of V_{DS}=0.1 V. The effect of the insulator type on electron accumulation at the interface between the semiconductor (a-IGZO) and the insulators (all types) is very apparent. Hence it is expected that it will necessarily have an effect on the threshold (V_{th}) and the on current (I_{on}). When the electron concentration surpasses 1x10^{14} cm^{-3} the TFT passes to an on regime. For SiO_2 insulators the -3V was enough to make electrons accumulate at the interface between the a-IGZO channel and the insulator due to low the electric field as shown in Figure IV-12. This may force the a-IGZO/SiO_2 TFT to work in the negative region of the bias. At a bias of 3 V a low electron concentration at the interface is obtained and makes the a-IGZO/SiO_2 TFT having a smaller I_{on} compared with the other TFTs this work. The a-IGZO/Si_3N_4 TFT work at the on regime at -2 V gate voltage when the electron concentration surpasses 1×10^{14} cm^{-3}. We notice that the electric field shows a higher value than SiO_2. At a bias of 3V the a-IGZO/Si_3N_4 has a higher concentration than the a-IGZO/SiO_2 TFT while less than the a-IGZO/Al_2O_3 and the a-IGZO/HfO_2 TFT. For the a-IGZO/Al_2O_3 TFT works at a bias of -1V

which makes it performing better than the a-IGZO/SiO_2 and the a-IGZO/Si_3N_4. The a-IGZO/HfO_2 TFT achieved the optimal performance in this work when it works at a bias of 0 V gate voltage with higher electron concentration the interface for a positive gate voltage. The low concentration for negative gate voltage may be due to the high electric field. These different values of the electron concentration are related to the effect of the electric flied. The high electric field causes a high electron concentration and makes the I_{on} of the a-IGZO higher while a low value of the electric filed causes the electrons to accumulate near the interface between the semiconductor and the insulator. This makes the TFT works in the negative gate bias region and this in turn mean the TFT is useless for electronic devices.

The calculation of conduction band offsets is illustrated in Figure IV-13. The conduction band offset for a-IGZO/SiO_2 and a-IGZO/Si_3N_4 is 3.26 and 1.56 eV respectively. Si_3N_4 have small band gaps compared with SiO_2 but Si_3N_4 show better performance due to high relative permittivity. Al_2O_3 is a wide band gap. Its band gap of 8 eV approaches that of SiO_2 but with a higher relative permittivity (9.3) than SiO_2. As we seen -IGZO/Al_2O_3 show performance better than SiO_2 and Si_3N_4. The conduction band offset a-IGZO/HfO_2 is 4.19 eV. a-IGZO/HfO_2 TFT show good performance compared with other insulators in this work. The offset band calculation show that insulators was used in this work suitable for TFT application. We concern the band offsets of Semiconductors/Insulators. The major problem with the choose insulators is that some have quite small band gaps. The barrier at each band must be over 1 eV to inhibit conduction by Schottky emission of electrons or holes into their bands [46]. Al_2O_3 and HfO_2 have large band gap and high k insulators which make them ideally for TFT application. We must take account when a dielectric material is used into a TFT structure; the structure related necessities include low defect density, few interfacial trap sites, low fringing capacitive effect, and band engineering possibility.

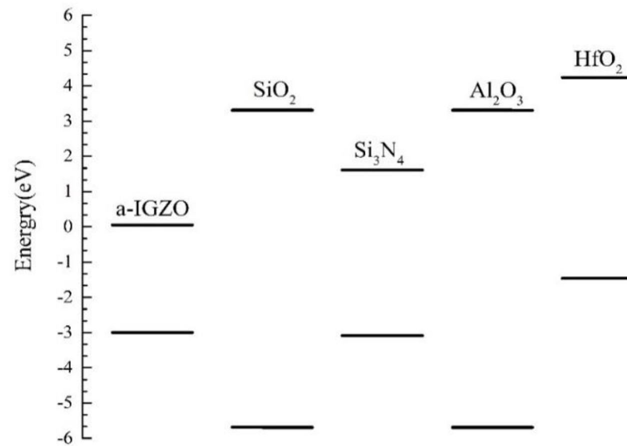


Figure IV-13:Band offsets for dielectrics on a-IGZO.

IV.4.3 Impact of insulators on TFTs V_{th} degradation

V_{th} instability is serious problem face a-IGZO application and industry. The negative bias illumination stress (NBIS) is an important case to the degradation a-IGZO TFT by generation defects on semiconductors channel or semiconductors insulators interface. to clarify the origin of V_{th} instability we test assumption of generation free electron bulk defect is cause negative shift V_{th} instability. The NBIS modulated by the donor Gaussian states near the conduction band when its increase leads to a negative threshold voltage shift [32], [47]–[49]. we simulated the variation in the transfer characteristics under increasing donor defects to evaluate device stability. The value of donor Gaussian varied from $6.5x10^{15}$ to $6.5x10^{17}$ $cm^{-}3$ eV^{-1} and we extracted the V_{th} value for different insulator layers.

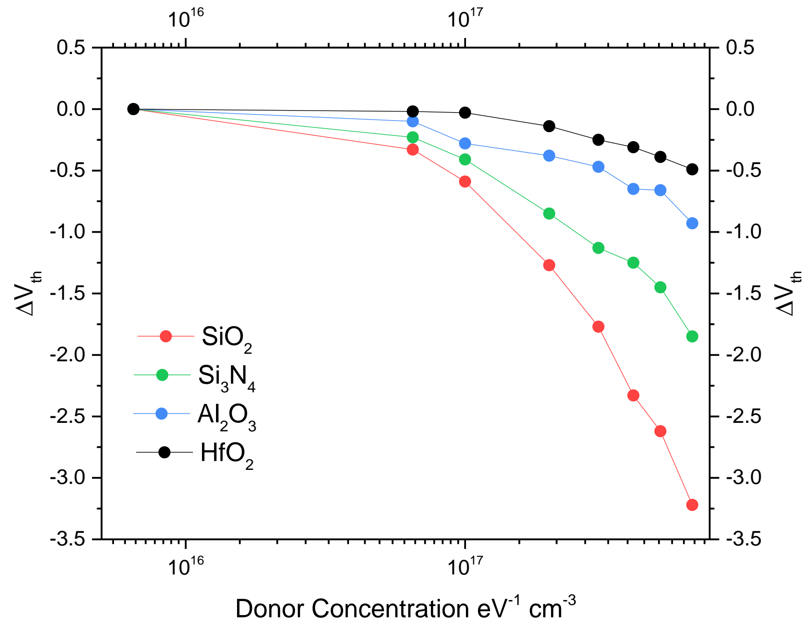


Figure IV-14: The threshold shift ΔV_{th}versus the Gaussian donor density per unit energy for different insulator layers.

Figure IV-14 represents the threshold shift (ΔV_{th}) versus values Gaussian donor density per unit energy for different insulator layers. The a-IGZO/SiO_2 TFT shows a sensitive behavior to the increasing in the donor Gaussian density per unit energy where it is degraded by a shift from 0 to -3.22V. The a- IGZO/Si_3N_4 TFT was less sensitive compared with the a-IGZO/SiO_2 TFT. IGZO/Si_3N_4 TFT is degraded by a shift from 0 to -1.85V. The a-IGZO/Al_2O_3-TFT is more stable than the a-IGZO/Si_3N_4 and the a-IGZO/SiO_2 TFTs where it shows a shift by 0 to -0.93V. The a-IGZO/HfO_2 TFT presents a superior performance compared with other gate insulators materials for which the shift in V_{th} was 0 to -0.43 V. the V_{th} instability was significantly different on the gate dielectric materials, even though all devices have an identical structure including a same physical parameter of a-IGZO layer. This mean that using high k dielectrics layers make a-IGZO TFT stable

then low k dielectrics. It is obvious that that all insulators show same behaviors which demonstrate that NBIS is independent on the type of the insulator where all TFTs show a negative shift. The obtain results indicated that generation of donner defects is origin of V_{th} negative shift instability but Using a high k oxide improves the stability of IGZO TFTs. On the other hand we can say that generation of defects occurs in semiconductor channel. not in semiconductors/insulators interface as suggested in some works [29], [50] but the dominate reason of V_{th} instability in a-IGZO is by generation of free carriers in channel region as mention in [47], [51]. We suppose that strong electric filed in high k dielectric control diffusion of electron on a-IGZO layer. During high electron concertation low k dielectric cannot control electron diffusion which created channel between source and drain this last make current flow even without applied gate voltage. In case high k dielectric, the strong filed electric control electron diffusion which make it more stable. Figure IV-15 shows the total current density in a-IGZO channel for two insulators layer SiO_2 and HfO_2. This indicates the channel formation between the source and the drain for SiO_2 and HfO_2. In case of SiO_2 the formed channel is larger while in the case of HfO_2, it is thinner. This means that the low k dielectric leads an easier degradation of V_{th} (towards to a more negative value).

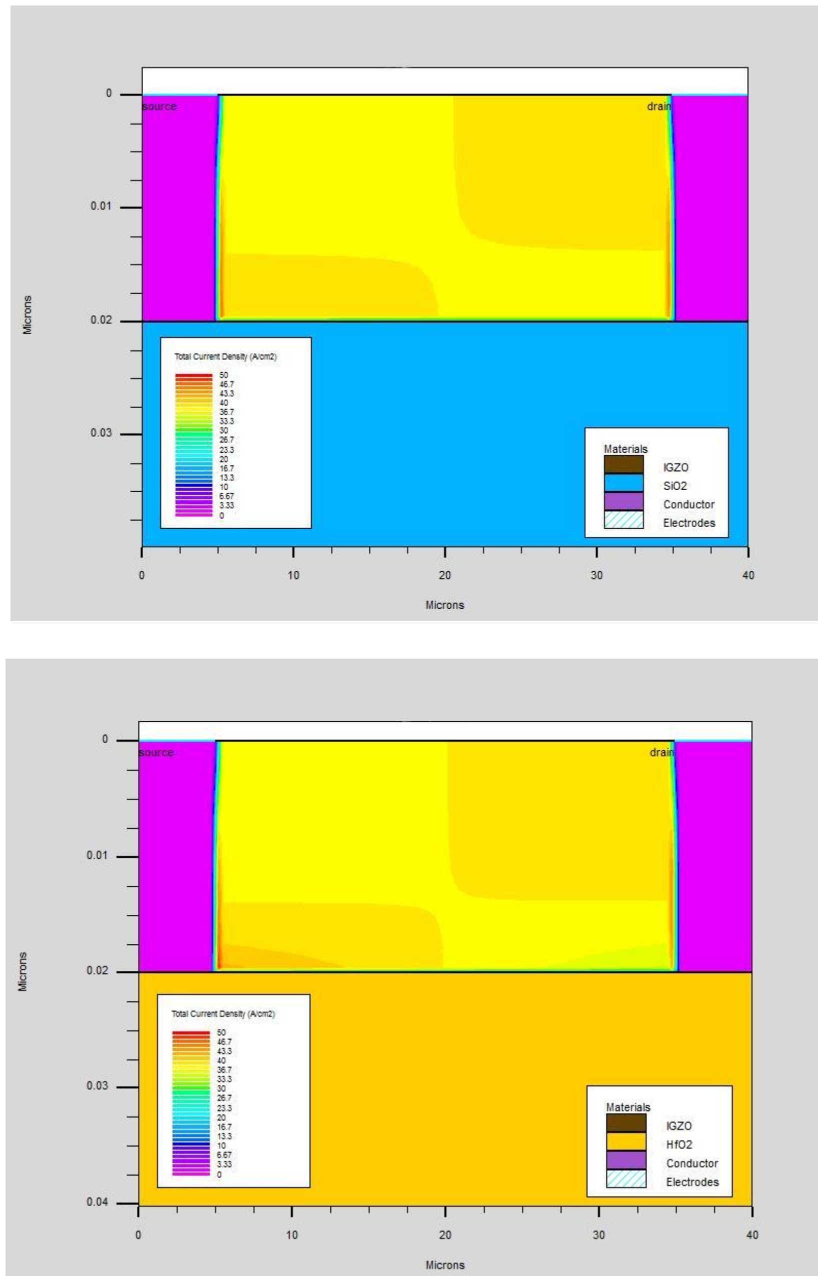


Figure IV-15:The total current density for (a) SiO_2 insulator layers and (b) HfO_2 insulator layers.

IV.4.4 Effect of fixed charge in HfO_2 insulator:

During HfO_2 fabrication there might be the possibility of defect creation. Generally, these defects are a fixed charge. It is well known that an MOS (Metal-Oxide-semiconductor) structure is very sensitive to the fixed charge in the gate insulator. To understand the effect of the fixed charge in HfO_2/a-IGZO TFT, the negative and positive fixed charge are studied. The fixed charge practically is related to oxygen loses and contamination during fabrication. We varied the fixed charge from -3×10^{12} to 3×10^{12} cm^{-2}. Figure IV-16 shows the TFT transfer characteristics with increasing charge density. The transfer characteristics curve moves toward positive for negative fixed charge while theb opposite trend is observed for a positive fixed. The output parameters do not show any variation with fixed charge except I_{on} and V_{th}. The I_{on} variation is due to the curve shift. V_{th} changes from 0.2 to 3.2V for a fixed charge changing from 0 to -3×10^{12}. The positive charge leads to a negative V_{th} shift. When the density of the fixed charge is positive and changes from 1×10^{12} to 3×10^{12}, V_{th} changes from -0.1 to -1.7 V. The negative charge in the oxide reduces the electron density that accumulates at the interface between a-IGZO and HfO_2. This makes the TFT requiring a more positive voltage to turn on. While the positive charge in oxide produces an electron accumulation at the interface even for a negative gate voltage. This requires a more negative voltage to switch OFF the transistor.

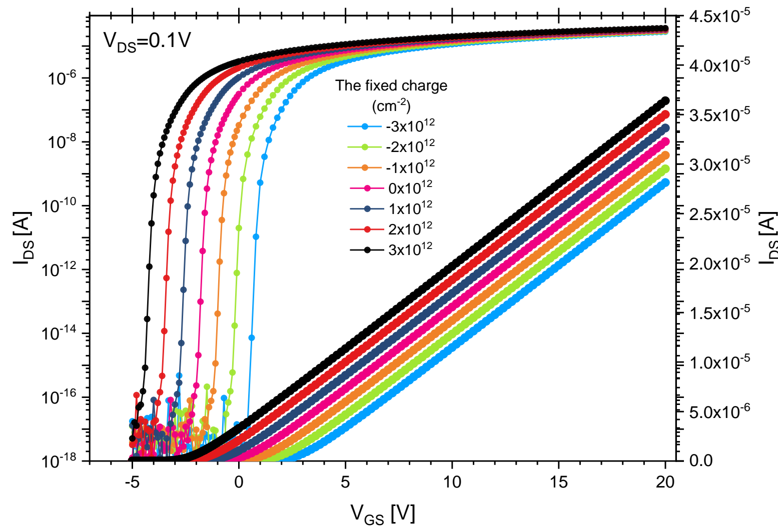


Figure IV-16:Transfer characteristics of the TFT with the fixed charge states in the insulator dielectric (HfO2)

IV.4.5 Effect of HfO_2 thickness:

In this part the effect of HfO_2 thickness on the a-IGZO TFT performance is investigated. The thickness was varied from 60 to 110 nm. Figure IV-17 shows the TFT transfer characteristics for different thicknesses. V_{th} decreases slightly from 0.26 to 0.22 V, which is a negative shift. The field effect mobility decreases from 26.32 to 11.98 $cm^2\ s^{-1}\ V^{-1}$. It is clear that the field effect mobility increases when the thickness is reduced. SS on the other hand does not show any variation with thickness. I_{on} increases with decreasing insulator thickness. This is obvious because the field effect mobility is higher for a thinner insulator. As a result, with thinner gate insulator, the channel area at the same applied gate voltage will induce more carriers. So, even at lower applied gate voltage the conduction channel could be formed in the TFT device and a low driving voltage TFT device would be the result. Devices with thick oxide layer have less gate control on the channel carriers

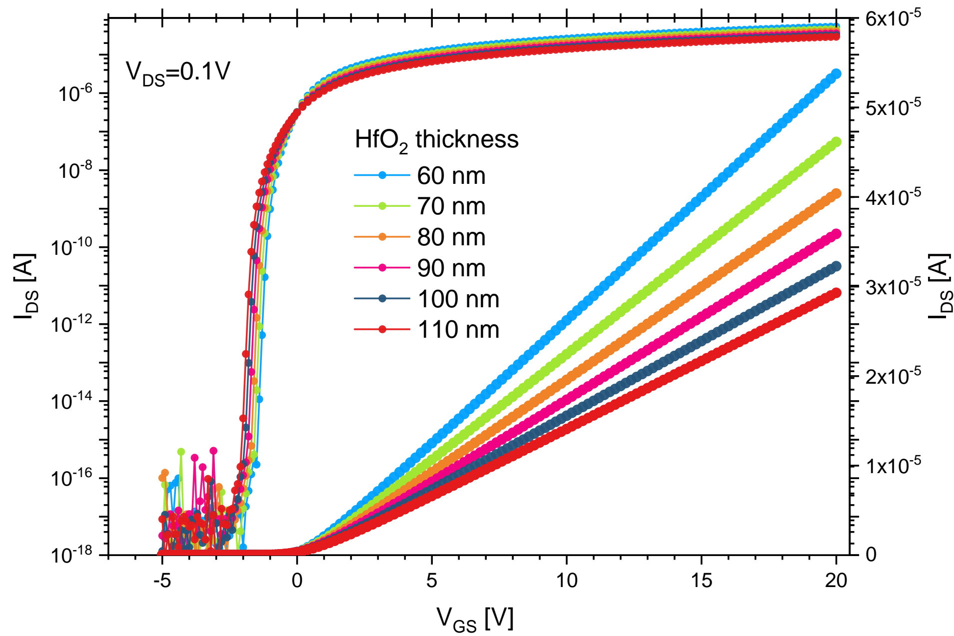


Figure IV-17:The transfer characteristics for different thickness of HfO2.

IV.5 Numerical simulation on thickness dependency and bias stress test of ultrathin IGZO thin-film transistors by a solution process

There have been several recent studies aiming to increase the stability of a-IGZO TFT or understanding the origin of its degradation. Some work showed that thickness of the a-IGZO channel is an important factor to consider for device optimization since it has a relation with the TFT performance [24], [52]–[54]. It has been observed that the a-IGZO TFT stability improved with increasing channel thickness [55]–[57]. By contrast other work showed that a decrease in the TFT channel thickness enhanced its stability [34], [58], [59]. Therefore, it seems that the experimental investigation the effect of thickness on the stability is not conclusive due to many factors. For example, contamination during the TFT fabrication, density of defects in the channel films, morphology of these films or absorption of ambient gases during or after fabrication. Using

numerical simulation can be more precise to clarify the channel thickness effect on a-IGZO TFTs and reveal how each factor is causing the a-IGZO TFT.

In this section, numerical simulation by ATLAS 2-D device simulator is used to investigate the channel thickness effect on the performance of ultra-thin film transistors. Its stability after negative illumination bias and positive bias stresses was also examined. The ATLAS 2-D device simulator has the ability to manipulate each factor in the semiconductor material and understand the impact of any factors on the output characteristics. The inverted-staggered a-IGZO TFT structure used for numerical simulation is shown Figure IV-18 and it is the same as in [59]. The structure consists of a 4/16 nm thick a-IGZO active layer and a 100 nm SiO_2 as a gate insulator layer. Channel length (L) and width (W) are 200 µm and 1000 µm, respectively. Note that front channel surfaces of the a-IGZO layer are assumed to be ideal, and no interface states are included, no leakage current through SiO_2, and no defect charges at the interface of a-SiO_2/a-IGZO or in the bulk of SiO_2. 100 nm thick aluminum (Al) is the ohmic contact for the source/drain (S/D) electrodes. P^{++} polycrystalline Si is used for the bottom gate.

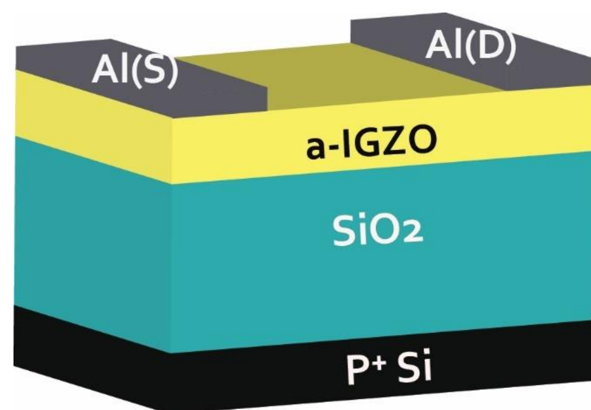


Figure IV-18. A schematic view of the a-IGZO TFT structure used in the simulation (similar to that of [59]*).*

The DOS model for a-IGZO is based on several published results [49], [60]–[62]. The increasing structural disorder within the amorphous material can induce electron scattering and, eventually, localized wave functions. Such phenomenon can be approximately represented as localized tail states within the band- gap, near the band edges. In a-IGZO, the conduction band-tail states are thought to originate from the disorder of metal ion s-bands, while the oxygen p-band disorder mainly contributes to the valence band-tail states and the donor Gaussian states result of oxygen vacancies [11], [14], [63]. Therefore, there are three distinguishable density of states (DOSs) in the band-gap region which are conduction band tail band ($g_{ct}^{A}(E)$), valence band tail band ($g_{vt}^{D}(E)$) and donor Gaussian states ($g_{G}^{D}(E)$),The conduction band-tail (CBT) states (acceptor-like states $g_{ct}^{A}(E)$)[5]:

The schematic DOS distribution in the a-IGZO layer is shown in Figure IV-19.

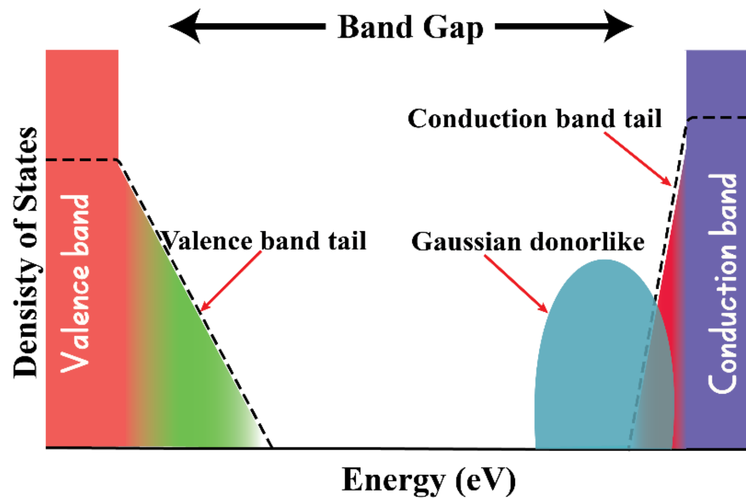


Figure IV-19. DOS distribution for a-IGZO.

The physical parameters of different layers used in this work are summarized in Table IV-6. Two structures were used in this work with different channel thickness: 4 and 16 nm. a-IGZO TFT is used in enhancement mode (V_{DS}=20V) and the gate voltage V_{GS} is varied from -20

to 40 V. The current-voltage characteristics are calculated, and internal parameters extracted. The stability was tested under negative illumination bias stress (NIBS) and positive bias stress (PBS).

Table IV-6: *The physical parameters of the different layers of the a-IGZO TFT used in this section.*

Layer	Parameters	Designation	Value
Channel (a-IGZO)	$N_C\ (cm^{-3})$	Effective DOS in the conduction band	5×10[18]
	$N_V\ (cm^{-3})$	Effective DOS in the valence band	5×10[18]
	$g_{ta}\ (cm^{-3}\ eV^{-1})$	Effective density at E_C	2.6×10[20]
	$E_a\ (meV)$	Energy slope of the conduction band-tail	13
	$g_{td}\ (cm^{-3}\ eV^{-1})$	Effective density at E_V	1.55×10[20]
	$E_d\ (meV)$	Energy slope of the valence band-tail	120
	$g_{gd}\ (cm^{-3}\ eV^{-1})$	Total density	1×10[17]
	$E_D\ (eV)$	Gaussian peak energy	3.1
	$\sigma_D(eV)$	Standard deviation	0.12
	$E_g(eV)$	Band gap	3.2
	$\chi\ (eV)$	Electronic affinity	4.16
	ε	Relative permittivity	10
	$L\ (\mu m)$	Length	200
	$W\ (\mu m)$	Width	1000
	$T\ (nm)$	Thickness	4/16
	$\mu_n(cm^2\ V^{-1}\ s^{-1})$	Free electron mobility	9
	$\mu_p(cm^2\ V^{-1}\ s^{-1})$	Free hole mobility	0.1
The insulator (SiO2)	$E_g\ (eV)$	Band gap	9.0
	ε_{ox}	Relative permittivity	3.9
S/D contacts (Al)	D (nm)	Thickness	100
	$\Phi_{Al}(eV)$	Work function	4.08
Gate (p++poly-Si)	D (nm)	Thickness	5
	$\Phi_{p-Si}\ (eV)$	Work function	4.58

To validate the simulation results we compared them to measurement of [59]. The experimental data were measured for a-IGZO TFT with inverted-staggered structure. The a-IGZO TFT fabricated on P^+ Si substrate and a 100 nm SiO_2 layer were used as a bottom gate and a gate dielectric respectively. A 4 nm channel thick of a-IGZO was obtained using a nitrate-based precursor from hexaaqua metal complexes, i.e. $[In(H_2O)_6]^{3+}$, $[Ga(H_2O)_6]^{3+}$, and $[Zn(H_2O)_6]^{2+}$. The composition ratio of indium:gallium:zinc was 9:0.5:0.5. The nitrate ligand-based oxide precursor solution was spin-coated onto the SiO_2/p+Si substrate at 3000 rpm for 30 s. After spin coating, the a-IGZO film were annealed at 100 °C for 5 min and for 250 °C for 5 min respectively. Next, the a-IGZO film was annealed at 250 °C for 2 h. The channel had a length of 200µm and a width of 1000µm. Finally, 100 nm of aluminum were deposited for the source and drain electrodes. Further details can be found in [64]. All the parameters extracted from experimental data used in this numerical simulation are listed in Table IV-6.

The simulated transfer characteristics are show in Figure IV-20. The electrical performance parameters are extracted from the transfer curves (Figure IV-21). The subthreshold voltage swing (SS) is given by the inverse of the maximum slope in the transfer characteristic. The threshold voltage (V_{th}) and saturation mobility μ_{sat} are extracted using equation *II-11*. This equation is the analytical approximation describing the enhancement mode TFT ($V_{DS} >> V_{GS} - V_{th}$):

Where W is the width of the channel, and L is the length of the channel, C_G is the insulator capacitance per area, V_{GS} is the gate bias. On-current (I_{on}) and on-to-off current ratio ($I_{on/off}$) are calculated from the transfer characteristics curve.

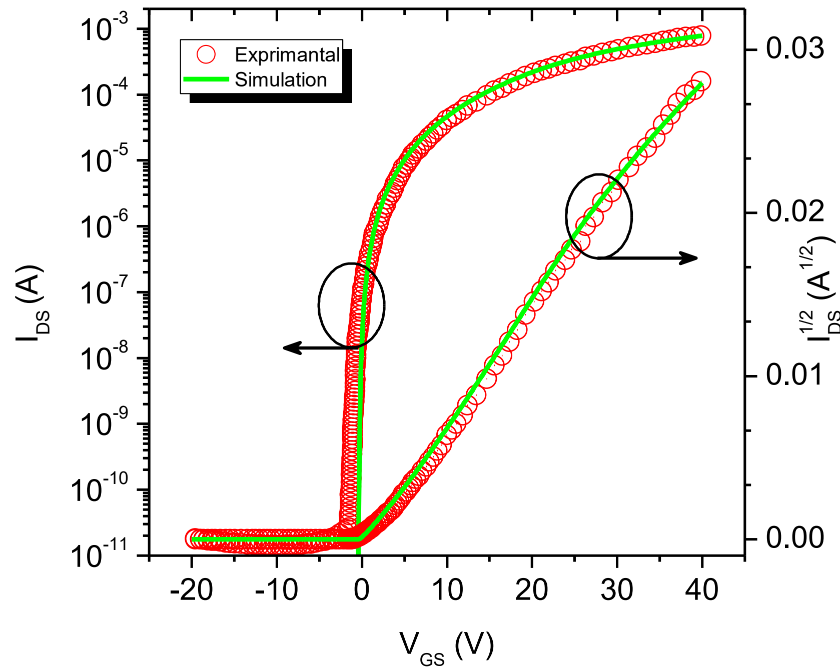


Figure IV-20. Experimental and simulated transfer characteristic curves for a-IGZO TFT.

As shown in Figure IV-21 there is a high similarity between experimental and simulation of the transfer characteristics. Table IV-7 summarizes the extracted output parameters from the simulated and experimental characteristics. The difference between the measured and simulated the threshold $\Delta V_{th} = V_{th_m} - V_{th_s} = 0.37\ V$ is acceptable. For the difference in the subthreshold extracted from measurement and simulation, it is very small ($\Delta SS = 0.27 - 0.22 = 0.05\ V\ dec^{-1}$). The saturation mobility is also comparable between experiment and simulation $\Delta\mu_{sat} = 7.73 - 7.56 = 0.17\ cm^2V^{-1}S^{-1}$ while the extracted values for I_{on} and $R_{\frac{on}{off}}$ from experiment and simulation are the same. Probably the small difference between some extracted experimental and simulated parameters are due to some factors which were not considered like interface states and fixed charge in the insulator.

Table IV-7: Comparison of extracted a-IGZO TFT parameters between experimental and simulation

	V_{th} (V)	SS (V dec^{-1})	μ_{sat} (cm^{2}V^{-1}s^{-1})	I_{on} (A)	$R_{on\text{-}off}$
Experimental a-IGZO TFT	3.10	0.27	7.73	7.08×10^{-4}	$\sim 10^{8}$
Simulated a-IGZO TFT	2.73	0.22	7.56	7.08×10^{-4}	1.77×10^{8}

IV.5.1.a Effect of thickness

Figure IV-21 shows the transfer characteristics of a-IGZO TFTs with different channel thickness. The extracted V_{th} are 2.73 V and 1.28 V for 4 and 16 nm respectively. V_{th} value of a-IGZO TFTs shifted toward negative direction as the thickness of a-IGZO channel layer increases from 4 to 16 nm. To show the origin of this behavior the free electron accumulated in the channel is extracted from the TFT simulation and is shown in Figure IV-22. It is evident that this is because of the increase in the number of free carriers, making it easier for them to accumulate. That is the thicker TFT have higher density of accumulated electrons concentration than the thinner one.

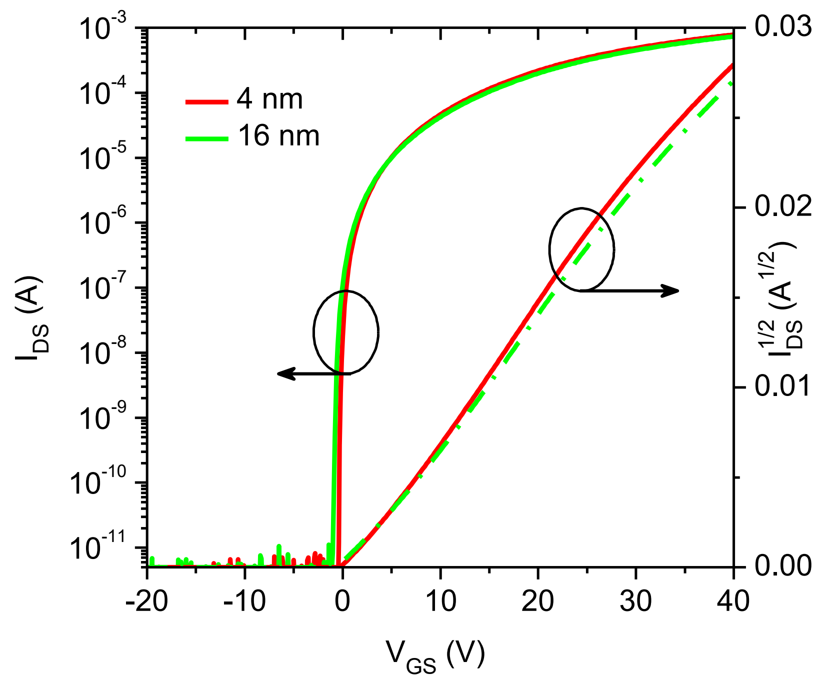


Figure IV-21. The simulated transfer characteristics for different thicknesses of the TFT channel.

With the increase in the film thickness, subthreshold swing increases from 0.22 to 0.27 V.dec^{-1} for 4 nm and 16 nm TFT respectively. We notice a degradation of SS as the channel layer thickness increases. Reducing the channel thickness increases the effective capacitance leading to the subthreshold swing decrease [53]. The thinner TFT shows a higher saturation mobility 7.56 compared to 6.41 cm^2 V^{-1} s^{-1} for the thicker one. I_{on} and I_{on}/I_{off} were also increased for the thinner TFT. They were 7.08×10^{-4} A and 1.77×10^{8} (for 4 nm) and 6.61×10^{-4} A and 1.65×10^{8} (for 16 nm) respectively. The higher I_{on} in the thinner channel is related to the saturation mobility as it is evident from equation *II-7*.

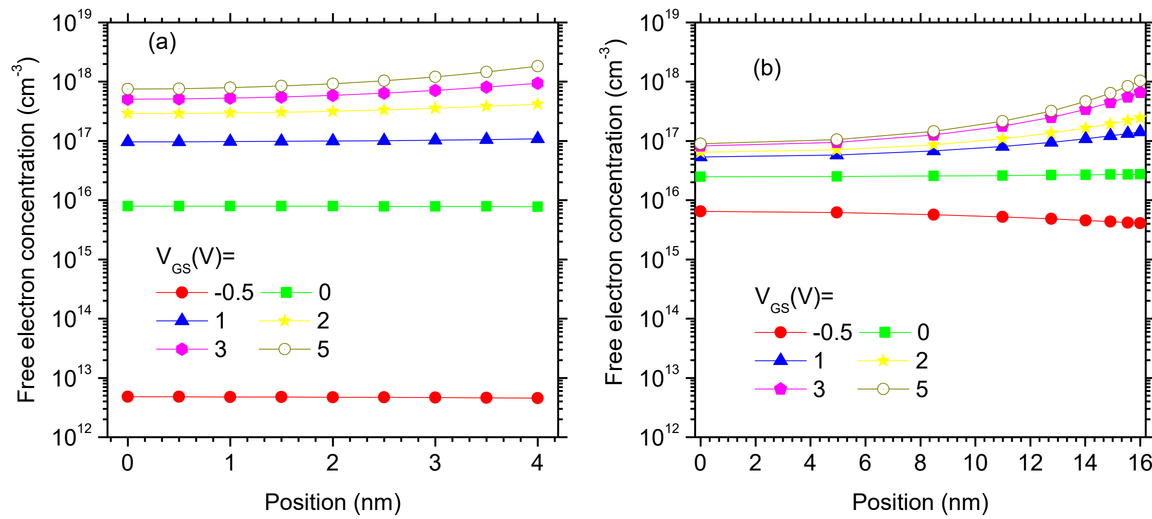


Figure IV-22. The extracted free electron density from simulation for 4 nm (a) and (b) for 16 nm channel thickness in TFTs for different gate voltages.

IV.5.1.b Stability of ultrathin a-IGZO thin films transistors

The degradation of V_{th} and SS are critical problems for a-IGZO TFT applications. The negative illumination bias stress (NIBS) test and the positive bias stress (PBS) test can be efficient ways to test stability of transistors. As known NBIS create more electron carriers in the a-IGZO channel which causes a V_{th} shift towards the negative side [31]. The NBIS can be simulate by increasing the Gaussian donor [5], [11], [14]. PBS, on the other hand, is the result of acceptor traps in the bulk of the channel [21], [55]. Therefore, PBS can be simulated as a Gaussian acceptor near the valance band. Figure IV-23 presents the transfer characteristics for the 4 nm to 16 nm a-IGZO TFT after NIBS. Figure IV-23(a)–(d) show variations in the I_{DS}-V_{GS} characteristics of the 4 ,8,12 and 16 nm devices with the evolution of Gaussian donor states. We found that an increasing Gaussian donor states can cause a negative shift in TFT transfer characteristic. The 16 nm TFT show stronger move to negative compared with 4 nm. For 16 nm TFT at high donor states show

increase in off current which 16 nm a-IGZO loses its semiconducting property and behaves more like a conductor. Figure IV-24 shows the extracted output parameters for different thickness.

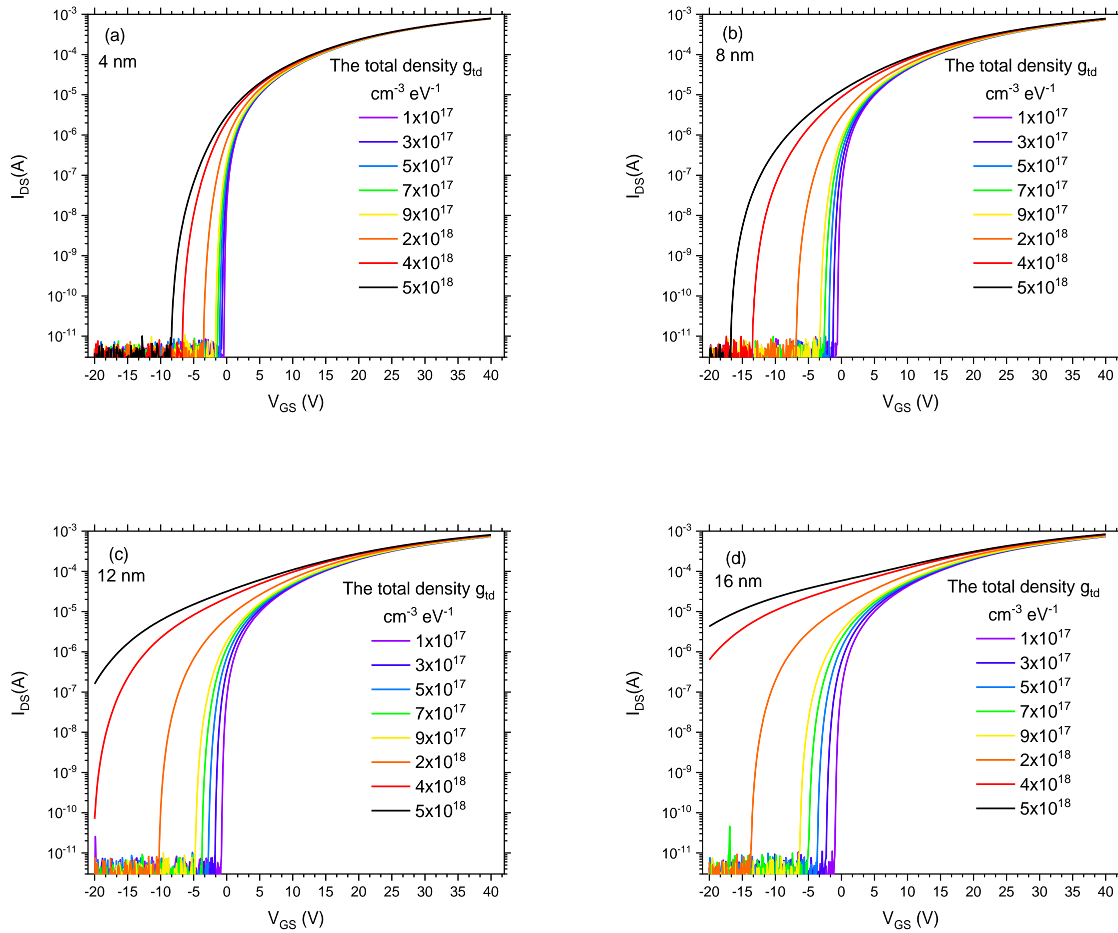


Figure IV-23. The effect of NBIS (creation of Gaussian donor states) on the transfer characteristics for: a) 4 nm a-IGZO TFT b) 8 nm a-IGZO TFT a) 12 nm a-IGZO TFT d) 16 nm a-IGZO TFT.

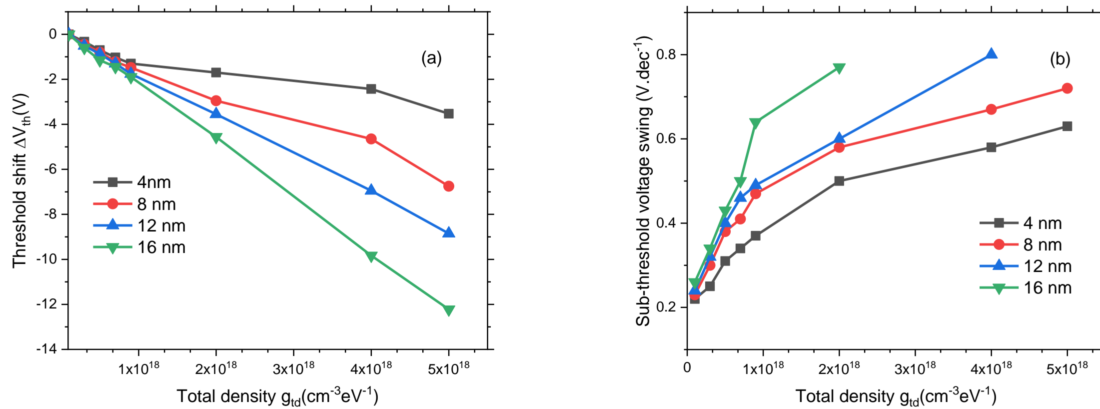


Figure IV-24. Effect of NBIS (creation of Gaussian donor states) for different thickness on extracted output parameters: a) Threshold shift b) Sub-threshold voltage swing

The Figure IV-24 (a) and (b) show degradation of output parameters with increasing the Gaussian donor causes a negative shift in V_{th} for different thickness. The 16 nm a-IGZO TFT shows a stronger degradation compared to other thickness. The increase in the Gaussian donor concentration is proportional to SS when SS value become larger which mean less performance of TFT. This behavior is predictable as mention previously that increase in the thickness causing more free electron carriers in the channel. The high density of electron in the channel make it easy to accumulate at interface between channel and insulators this led to negative shift of V_{th}. 16 nm TFT has higher free electron than the 4 nm TFT as the thicker shows a high shift in the threshold (ΔV_{th}). Simulation results indicate the dependency of thickness on NIBS.

Figure IV-25 (a)–(d) shows the simulated transfer characteristics for 4 ,8,12 and 16 nm a-IGZO TFT after PBS (creating more acceptor states).Figure IV-26 shows the extracted output parameters (from the transfer characteristics) after PBS.

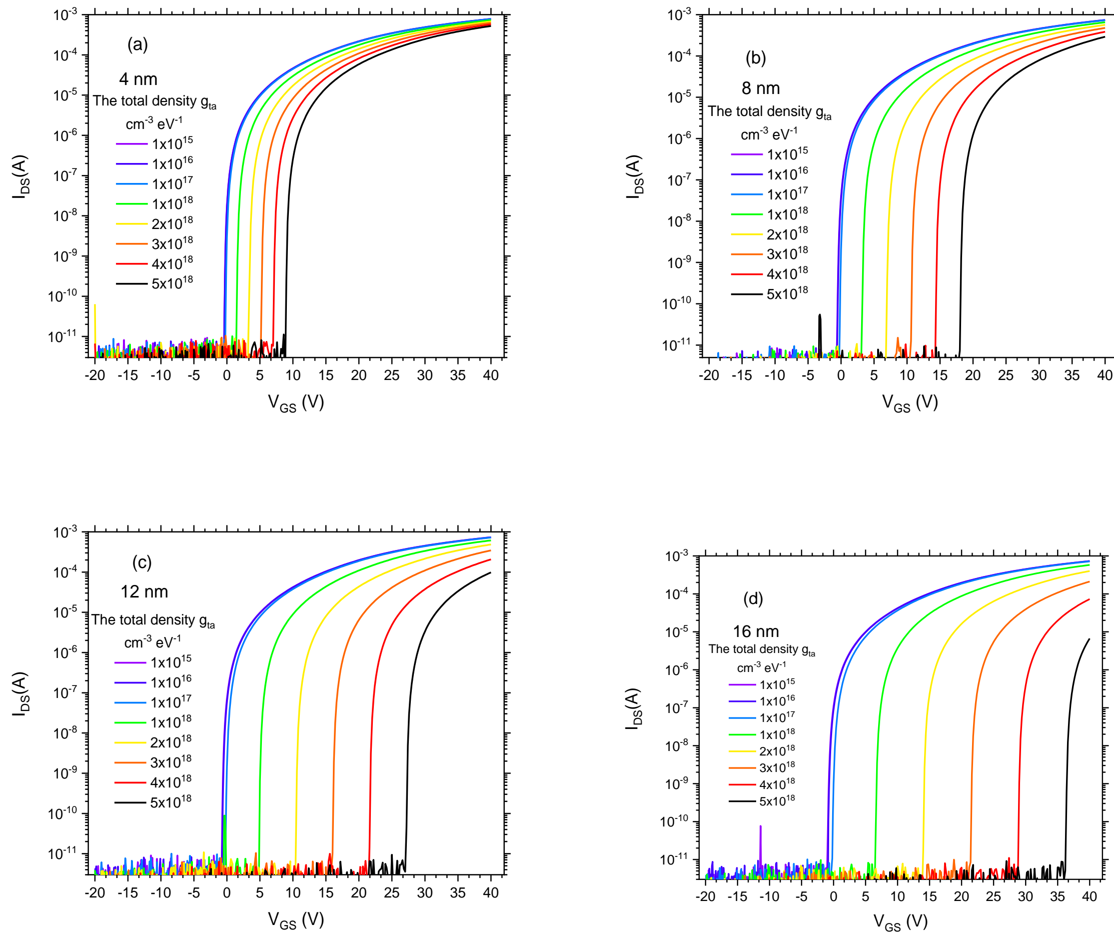


Figure IV-25. The simulated transfer characteristics after PBS for: for: a) 4 nm a-IGZO TFT b) 8 nm a-IGZO TFT a) 12 nm a-IGZO TFT d) 16 nm a-IGZO TFT.

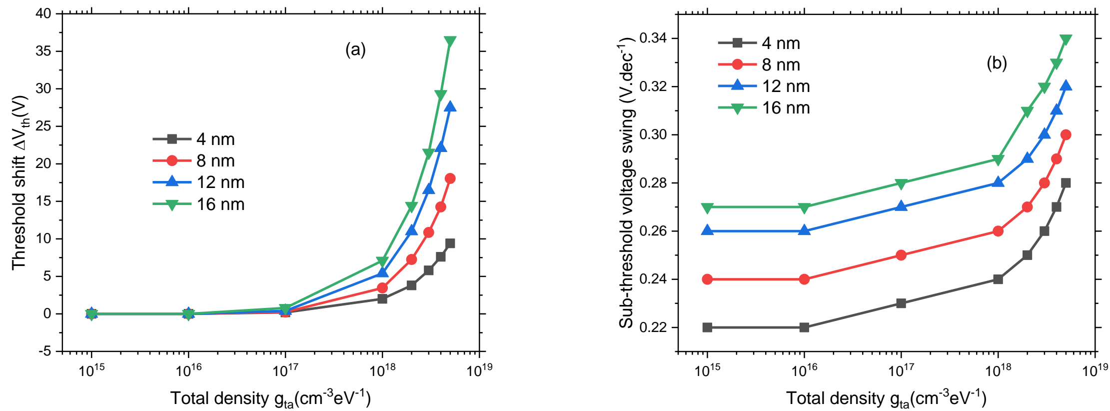


Figure IV-26. Effect of PBS (creation of Gaussian acceptor states) for different thickness on extracted output parameters: a) Threshold shift b) Sub-threshold voltage swing

Figure IV-25 (a)–(c) show variations in the I_{DS}-V_{GS} characteristics of the 4 ,8,12 and 16 nm devices with the evolution of Gaussian acceptor states. We found that an increasing Gaussian acceptor states can cause a positive shift in TFT transfer characteristic. The 4nm TFT show less move to positive compared with 16 nm. Acceptors states affected on I_{on} value that is clear at 16nm TFT. 4 nm TFT show more stability and more appropriate for TFT application.

The extracted parameters after PBS induces a positive shift in V_{th} and increases SS in all different thickness. The 4 nm a-IGZO TFT shows a higher stability compared to other thickness. The increase of the channel thickness leads to an increase in the free electron concentration. The high electron concentration increases the probability of the trapping rate and hence induces a higher positive shift in the thicker TFT. On other hand the acceptor states trap more free electron which make TFT requires a more positive gate voltage to switch ON. The PBS show decency with thickness.

Similar results were reported previously for an HfInZnO-TFTs [58], a-IGZO TFT [34]. The simulation of NBIS and PBS agreed very well with what have been reported for solution-processed ultrathin a-IGZO TFT in [59].wh Choi, C., Baek, ere Choi, C., Baek et all found that the thinner 4 nm show high stability compared with thicker 16 nm TFT.

IV.6 Deposition a-IGZO thin films by sol gel method

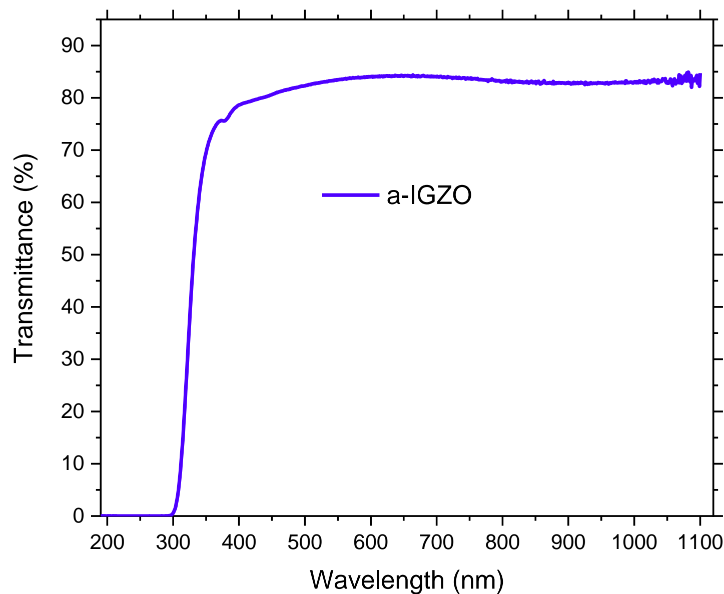


Figure IV-27 Transmittance spectra of a-IGZO film

The IGZO films were deposited on a glass substrate (commercial glass). A measurement of the original substrate transmittance was obtained using an ultraviolet–visible (UV–Vis) spectrophotometer (Thermofisher Evolution 220). The prepared films had high average transmittance values (over 90%) in the visible region, as shown in Figure IV-27.

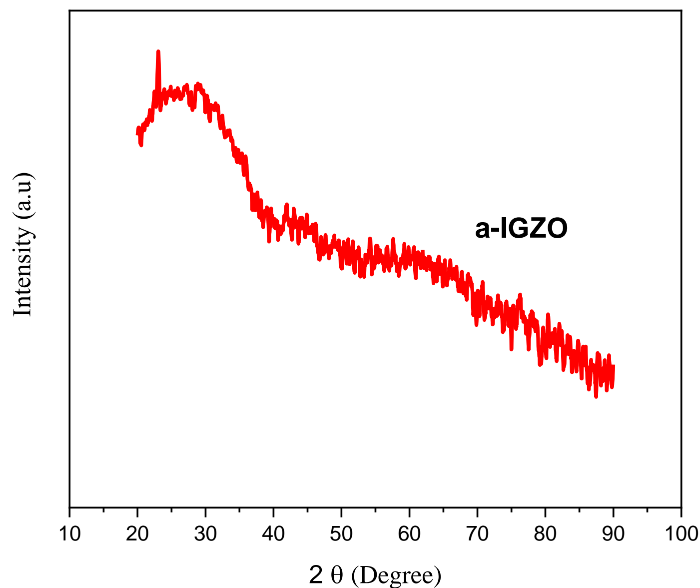


Figure IV-28 XRD patterns of a-IGZO thin films

Figure IV-28 shows XRD patterns of IGZO thin films annealed at 350°C. These diffraction patterns were examined using a thin film X-ray diffractometer using CuKα radiation (λ=1.5406 Å) with a glancing incident angle of 0.8. No observable diffraction peaks were detected from these thin films. However, showed a weak and broad diffraction signal in the 2θ range of 17–25. Such a feature indicated that the structure of annealed thin films was amorphous phase.

IV.7 References

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Conclusion

This thesis is a simulation work to elucidate some effects in a-IGZO TFTs. Three main parts are undertaken: the effect of defects due to Hydrogen is studied, the gate type and the channel thickness contributions to the TFT stability.

An extensive work was carried out to elucidate the effect of near valance band defects on the performance of an a-IGZO TFT. Several possibilities were explored. It was found that donor defects near the valance band did not show any effect on the TFT performance. However, the degradation of the mobility contributes to the degradation in the TFT performance. Acceptor defects states on the other hand degrade the threshold voltage by shifting its value to larger positive voltages. A Gaussian acceptor near the valance band has an effect and it is comparable to experimental measurements. It was concluded hydrogen and oxygen disorder are not responsible for donor defects creation near the valance band but deep acceptor defects having Gaussian distribution in a-IGZO. The near valance defect study might be helpful for a better understanding of the device stability and thus gives a hint for typical a-IGZO semiconductor device improvement.

The performance and stability of a-IGZO TFTs with SiO_2, Si_3N_4, Al_2O_3 and HfO_2 as the gate dielectrics have been investigated and compared. The simulation results have shown a superior performance achieved for a-IGZO TFTs with the HfO_2 dielectric, such as small threshold voltage, improved subthreshold swing, increased mobility and I_{on} current. The HfO_2 insulator achieved a high term of stability compared with SiO_2, Si_3N_4 and Al_2O_3 while the instability of a-IGZO independent on the gate insulator material. SiO_2, Si_3N_4, Al_2O_3 and HfO_2 as the gate insulators show degradation with increasing of the donor Gaussian density of states. The proper choice of the gate dielectric can provide better device reliability in oxide TFTs. Therefore, the optimization of gate dielectrics materials will be helpful in reducing the instability.

Finally, the channel thickness effect on the performance of a-IGZO TFTs was investigated by comparing simulation to measurements provided by a collaboration with a South Korean

University. The 4 nm-channel-IGZO TFT revealed a superior performance compared to the its 16 nm counterpart. The 4 nm-thick, or ultrathin a-IGZO TFT; exhibited a higher saturation mobility, low threshold voltage, a small value of SS, a high on/off current ratio. The 4 nm-thick a-IGZO TFT also showed superior operating stability during NBS and PBS tests. Our results based on simulation were successfully used for explaining the measured (experimentally observed) performance of the TFT. Also; based on our simulation results we concluded that reducing in thickness increase the performance of a-IGZO TFT. The thickness optimization is a key factor for optoelectronics and display devices application.

Appendix: Publications and Conferences

Publication

M. Labed, N. Sengouga, K. H. Kim, Y. S. Rim, *Phys. status solidi*, **2019**, DOI:10.1002/pssa.201800987.

M. Labed, N. Sengouga, A. Meftah, *Mater. Res. Express*, **2019**, DOI:10.1088/2053-1591/ab11a5.

M. Labed, N. Sengouga, *J. Comput. Electron.*, **2019**, DOI:10.1007/s10825-019-01316-4.

Conferences

NANO FOR NEXT GENERATION, Firat university-2015-Elazig

SCIENCE AND APPLICATION THIN FILMS-Izmir institute of Technology -2016-Izmir

SUSTAINABLE ENERGY AND ENVIRONMENTAL PROTECTION -University of manbor 2017-SLOVENIA

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Numerical Simulation on Thickness Dependency and Bias Stress Test of Ultrathin IGZO Thin-Film Transistors Via a Solution Process

Mohamed Labed, Nouredine Sengouga,* Kyung Hwan Kim,* and You Seung Rim**

The authors report the effect of ultra-thin channel layer thickness on the performance of an amorphous InGaZnO (a-IGZO) thin-film transistor (TFT). Numerical simulation is used to investigate the thickness effect on the a-IGZO TFT output parameters. The simulation results are compared to measurements of the stability of nitrate ligand-based hexaaqua complexes solution-processed ultrathin a-IGZO transistors a-IGZO. This TFT is also tested under negative illumination bias stress (NIBS) and positive bias stress (PBS). The thinner channel layer is found to have a better performance than the thicker channel layer. The 4 nm-thick, ultra-thin a-IGZO TFT exhibits high saturation mobility (7.56 $cm^2 V^{-1} s^{-1}$), low threshold voltage (2.73 V), a small value of sub threshold swing (0.22 V dec^{-1}), and a high on/off ratio (1.77×10^8). It is also noticed that the threshold voltage (V_{th}) shifts negatively as the thickness increases. The 4 nm long channel TFT shows more stability under NIBS and PBS while 16 nm have a strong degradation under NIBS and PBS.

1. Introduction

Thin films based on amorphous oxide semiconductor (AOS) like amorphous InGaZnO has received much attention in recent years due to high optical transmittance,[1] high mobility,[2] low cost,[3] chemical stability,[4] easy deposition for large area, and compatible with flexible electronics.[5,6] AOS replaced the conventional semiconductors such as a-Si, organic semiconductors, and binary oxides like ZnO and In_2O_3, SnO_2.[7] a-IGZO has many possible uses in optoelectronics such as light emitting diode,[8] solar cells,[9] and thin films transistors (TFT).[10,11] TFTs based on a-IGZO show high mobility with the low threshold voltage (V_{th}), low subthreshold (SS), high mobility, and stable amorphous structure. Because heavy metal indium cations share electrons in 5 s orbital and acts as electron pathways which contributes to an increased carrier mobility of a-IGZO.[12,13] Gallium ions form strong chemical bound with oxygen ions which is important to obtain stable AOSs and TFT.[14] However, the biggest hurdle in commercialization a-IGZO TFT-based electronics is their stability against negative illumination bias,[15] positive bias,[16] temperature,[17] and the presence of ambient gas.[18]

There have been several recent studies aiming to increase the stability of a-IGZO TFT or understanding the origin of its degradation. Some work showed that thickness of the a-IGZO channel is an important factor to consider for device optimization since it has a relation with the TFT performance.[19–22] It has been observed that the a-IGZO TFT stability improved with increasing channel thickness.[23–25] By contrast other work showed that a decrease in the TFT channel thickness enhanced its stability.[26–28] Therefore, it seems that the experimental investigation of the effect of thickness on the stability is not conclusive due to many factors: in case of contamination issues during the TFT fabrication, density of defects in the channel films, morphology of these films, or absorption of ambient gas during or after fabrication. Using numerical simulation can be more precise to clarify the channel thickness effect on a-IGZO TFTs and reveal how each factor is causing the a-IGZO TFT.

In this work, numerical simulation by ATLAS 2-D device simulator is used to investigate the channel thickness effect on the performance of ultra-thin film transistors. Its stability after negative illumination bias and positive bias stresses was also examined.

2. 2D Numerical Simulation

The ATLAS 2-D device simulator could manipulate each factor in the semiconductor material and understand the impact of any factors on the output characteristics. The inverted-staggered a-IGZO TFT structure used for numerical simulation is shown in **Figure 1** and it is the same as in ref. [28]. The structure consists of a

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Simulation of the influence of the gate dielectric on amorphous indium-gallium-zinc oxide thin-film transistor reliability

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Abstract

Indium-gallium-zinc oxide (IGZO) thin films have attracted significant attention for application in thin-film transistors (TFTs) due to their specific characteristics, such as high mobility and transparency. The performance of a-IGZO TFTs with four different insulators (SiO_2 Si_3N_4, Al_2O_3 and HfO_2) is examined using a numerical simulator (Silvaco Atlas). It is found that the output performance is significantly enhanced with high relative permittivity of the insulator. HfO_2 gives the best performance: lower threshold voltage 0.23 V and subthreshold 0.09 V dec^{-1}, higher field-effect mobility 13.73 $cm^2\ s^{-1}\ V^{-1}$ and on current (I_{on}) and I_{on}/I_{off} ratio 2.81×10^{-6} A, 5.06×10^{12}, respectively. Therefore, HfO_2 gate showed high stability compared with other gate insulator materials.

Keywords a-IGZO · TFT · Simulation · Insulators · Stability

1 Introduction

Transparent amorphous oxide semiconductors (TAOS) have attracted more attention compared to conventional transparent oxide semiconductor (TOS) such as zinc oxide (ZnO), indium oxide (In_2O_3) and indium-doped zinc oxide (IZO). Amorphous indium-gallium-zinc oxide (a-IGZO) is the most promising TAOS due to several good properties such as higher mobility, larger band gap, better transparency and room temperature deposition. a-IGZO has a wide application, especially in thin-film transistors (TFT). TFT based on a-IGZO replaced the conventional TFTs based on amorphous silicon (a-Si), zinc oxide (ZnO) or organic semiconductors (OSC) [1, 2]. Enhancing the performance of a-IGZO was the objective of several groups [3–5]. The instability of a-IGZO TFTs following a stress by bias, light, temperature or mechanical is a serious drawback and a sensitive issue in application and industry. Also, a considerable work is ongoing to understand the reasons for this instability following a negative bias illumination stress [6, 7] or a positive bias stress [8, 9]. Several ways are implemented in order to reduce the impact of this instability such as finding an optimal structure [10], using a passivation layer [11], physical and chemical treatments after deposition [3] and finding an optimal insulator of the gate from the channel of the a-IGZO TFT [12]. Various gate insulators, such as silicon dioxide (SiO_2) [13], silicon nitride (Si_3N_4) [14, 15], aluminum oxide (Al_2O_3) [16, 17] and hafnium oxide (HfO_2) [12, 18], have been investigated for use in TFTs.

In this paper, numerical simulation is used to understand the effect of the insulator type on the operation of a-IGZO TFT and the threshold (V_{th}) instability. The insulators compared are SiO_2, Si_3N_4, Al_2O_3 and HfO_2. The other parameters evaluated are: on-current (I_{on}), field-effect mobility (μ_{FE}), threshold voltage (V_{th}), subthreshold swing (SS), on-to-off current ratio (I_{on}/I_{off}) and threshold shift (ΔV_{th}). The numerical simulation is carried out using TCAD of SILVACO-ATLAS software which is a very powerful tool to simulate and study electronic devices. TCAD permits to vary many parameters which model the experimentally observed phenomenon. The numerical study explains the effect of insulators separately from the contribution of other parameters such as interface states between the semiconductor and the insulator or the fixed charge in insulator material. This separation is not achievable in experimental work. Furthermore, numerical simulation decreases the cost and time required by measurement and it is obvious that a rigorous study of insulators and instability effects is very difficult to be achieved experimentally .

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PAPER

Simulation of the effect of deep defects created by hydrogen on the performance of amorphous indium gallium zinc oxide thin film transistor (a-IGZO TFT)

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Keywords: a-IGZO, TFT, simulation, defects, degradation, hydrogen

Abstract

Amorphous indium gallium zinc oxide (a-IGZO) are promising for developing thin film transistors (TFTs) because of their large electron mobility, small threshold voltage (V_{th}), and low temperature fabrication process. In this study, we have investigated the effect of near valance band defects on the output parameters of a-IGZO TFTs by using two-dimensional TCAD numerical simulation. It was found that donor defects near the valance band have no effect. The degradation of the mobility also causes degradation in the TFT performance. Acceptor defects states near valance band is the reason of positive V_{th} shift. It is therefore concluded that near valance band defects are not donor defects but acceptor defects with a Gaussian distribution which can also degrade the mobility.

1. Introduction

Amorphous oxide semiconductors (AOSs) such as amorphous In–Ga–Zn–O (a-IGZO) are promising for developing thin film transistors (TFTs) because of their large electron mobilities, small threshold voltage, and low temperature fabrication process. a-IGZO TFTs are expected to be used in high-resolution active-matrix organic light-emitting diode displays (AMOLEDs) and liquid crystal displays (AMLCD) [1, 2]. The stability of a-IGZO TFTs, defined by the threshold voltage shift (ΔV_{th}), is a crucial issue for its practical applications. There is an intense ongoing research work investigating possible causes of the threshold voltage shift (ΔV_{th}). One of such possible causes is oxygen vacancies near the conduction band minimum (CBM) states [3–5]. The oxygen vacancies are the reason for negative V_{th} shift. The presence of hydrogen creates defect states near the valance band maximum (VBM) [6, 7]. The oxygen disorder is origin of deep defects states [8]. The high density subgap defects in a very deep energy region just above the valance band maximum (near-VBM states) may be another cause of the instability. However, it is not yet known what kind of influence defect near VBM states have on the device performance such as threshold voltage shift. In this work a detailed numerical simulation is carried out to understand the effect of defects near VBM on the a-IGZO TFT performance. In particular each possible defect type, supposed to be created by the presence of hydrogen, is introduced in the a-IGZO channel (channel material of the TFT) and its effect on the electrical TFT characteristics is studied. This is carried out by numerical simulation using ATLAS software which is a very powerful tool to simulate and study many electronic devices. The software allows the variation of many parameters in order to model or to reproduce the experimentally observed phenomenon. Furthermore, numerical simulation decreases the cost and time required by measurement and it is obvious that a careful study of defect effects is very difficult to be achieved experimentally.

2. 2D Numerical simulation

A 2D inverted-staggered a-IGZO TFT structure was defined in this work which is shown in figure 1. It consists of an a-IGZO active layer (20 nm thick), an SiO_2 insulator layer (100 nm thick) and a silicon wafer substrate (n^{++})

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*Presented by M. LABED, F. AZRI, AF. MEFTAH, *N. SENGOUGA, AM. MEFTAH in NANONG2015*

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Effect of Hydrogen on the Performance of amorphous Indium gallium Zinc Oxide (a-IGZO) Thin Film Transistors

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[keywords] a-IGZO, TFT, Hydrogen.

Amorphous In-Ga-Zn-O (a-IGZO) are promising for developing thin films transistors (TFTs) because of their large electron mobilities, small subthreshold voltage swing, and low temperature fabrication process. a-IGZO TFTs are largely used in high-resolution active-matrix organic light-emitting diode displays (AMOLEDs) and liquid crystal displays (AMLCD) [1,2]. The impurity hydrogen in gallium-indium-zinc oxide a-IGZO create deep defect near valance band minimum (VBM) which may cause instability. In this study we have investigated the effect of hydrogen on output parameter a-IGZO TFTs by two-dimensional numerical simulation (Silvaco). Our results indicates that the standard model does not reproduce measurements [3]. We therefore adopted the well known defect pool model for amorphous silicon to a-IGZO which gave much better results. The threshold Voltage (Vth) increase with increasing of Hydrogen and states near VBM concentration.

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Effect of Insulators on the a-IGZO TFT Performance

MOHAMED LABED, NOUREDINE SENGOUGA & SLIMANE CHALA

Abstract Indium Gallium Zinc Oxide (IGZO) thin films have attracted significant attention for application in thin-film transistors (TFTs) due to their specific characteristics, such as high mobility and transparency. The performance a-IGZO thin film transistors (TFTs) with four different insulators (SiO2 Si3N4, Al2O3 and HfO2) are examined by using numerical simulation. It is found that the output performance is significantly enhanced with high relative permittivity of the insulator. The HfO2 gate insulator gives the best performance: lower threshold voltage and subthreshold, and higher field effect mobility, on current and Ion/Ioff ratio.

Keywords: • a-IGZO • TFT • Simulation • Insulators • Stability.•

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