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Radiation hardness studies in a CCD with high-speed column parallel readout

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ABSTRACT: Charge Coupled Devices (CCDs) have been successfully used in several high energy physics experiments over the past two decades. Their high spatial resolution and thin sensitive layers make them an excellent tool for studying short-lived particles. The Linear Collider Flavour Identification (LCFI) collaboration is developing Column-Parallel CCDs (CPCCDs) for the vertex detector of the International Linear Collider (ILC). The CPCCDs can be read out many times faster than standard CCDs, significantly increasing their operating speed. The results of detailed simulations of the charge transfer inefficiency (CTI) of a prototype CPCCD including the variation of model parameters are reported. The effects of bulk radiation damage on the CTI of a CPCCD are studied by simulating the effects of two electron trap levels, 0.17 and 0.44 eV, at different concentrations and operating temperatures. The dependence of the CTI on different occupancy levels (percentage of hit pixels) and readout frequencies is also studied. The optimal operating temperature for the CPCCD, where the effects of the charge trapping are at a minimum, is found to be about 230 K for the range of readout speeds proposed for the ILC. The results of the full simulation have been compared with an analytic model.

KEYWORDS: Models and simulations; Radiation damage to detector materials (solid state).

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Contents

1. Introduction

Particle physicists worldwide are working on the design of a high energy collider of electrons and positrons (the International Linear Collider or ILC) which could be operational sometime around 2019. Any experiment exploiting the ILC will require a high performance vertex detector to detect and measure short-lived particles, yet be tolerant to radiation damage for its anticipated lifetime. One candidate is a set of concentric cylinders of Charge-Coupled Devices (CCDs), read out at a frequency of around 50 MHz.

It is known that CCDs suffer from both surface and bulk radiation damage. However, when considering charge transfer losses in buried channel devices only bulk traps are important. These defects create energy levels (traps) between the conduction and valence band, and electrons are captured by them. These electrons are also emitted back to the conduction band after a certain time.

It is usual to define the Charge Transfer Inefficiency (CTI) as the fractional loss of charge after transfer across one pixel. An initial charge Q_0 after being transported across m pixels is reduced to $Q_m = Q_0(1-\mathrm{CTI})^m$. For CCD devices containing many pixels, CTI values around 10^{-5} are important. Previous results for a CCD with sequential readout have recently been reported [1 – 6] The expected background rate at the future ILC near the interaction point leads to radiation damage in the CCD detector. We simulated the charge transfer in a CPCCD (Column-Parallel CCD) using the trap concentrations listed in table 1. They correspond to about 3 years of operation of the CCD at about 1 cm from the collision point of the beam at the ILC for the 0.17 eV traps and several more years for the 0.44 eV traps.

In contrast to silicon microstrip detectors, such as those used in the Large Hadron Collider (LHC), where all kind of traps in the bulk are important, in CCDs only electron traps are important. Traditionally, for these CCD studies, only the two traps with the largest trap densities are considered [2, 6 – 8].

Table 1. Energy levels E, trap concentrations C, and electron-capture cross-section σ_n used in simulation.

E (eV)	C (cm^{-3})	σ_n (cm^2)
0.17	1×10^{12}	1×10^{-14}
0.44	1×10^{12}	1×10^{-15}

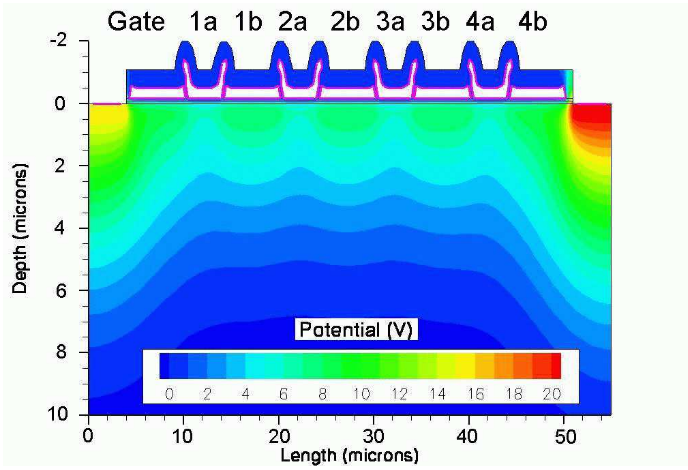

Figure 1. Detector structure and potential at gates (nodes) after initialization. In this 2-phase CCD one pixel is made of two gates. Each gate consists of two parts (a,b). The parts a and b have different doping profiles within one micron depth. The pixel under consideration is located between 20 and 40 μm length.

2. Simulations

The UK Linear Collider Flavour Identification (LCFI) collaboration [9] has been studying a CCD with high-speed (50 MHz) column-parallel readout produced by e2V Technologies. It is a two-phase buried-channel CCD with 20 μm square pixels.

Simulations of a simplified model of this device have been performed with the ISE-TCAD package (version 7.5), particularly the DESSIS program (Device Simulation for Smart Integrated Systems). The simulation is essentially two dimensional. The overall length and depth are 55 μm and 20 μm respectively (figure 1).

Parameters of interest are the readout frequency, up to 50 MHz, and the operating temperature between 130 K and 300 K although simulations have been performed up to 440 K. The charge in transfer and the trapped charge are shown in figures 2 and 3.

Charge Transfer Inefficiency is a measure of the fractional loss of charge from a signal packet as it is transferred over a pixel, or two gates. After DESSIS has simulated the transfer process, a 2D integration of the trapped charge density distribution is performed independently to give the total charge under each gate.

This CTI study, at nominal clock voltage, focuses only on the bulk traps with energies 0.17 eV and 0.44 eV below the bottom of the conduction band. These traps will be referred to simply as the 0.17 eV and 0.44 eV traps. The 0.17 eV trap is an oxygen-vacancy defect, referred to as an A-centre defect. The 0.44 eV trap is a phosphorus-vacancy defect, an E-centre defect, as a result

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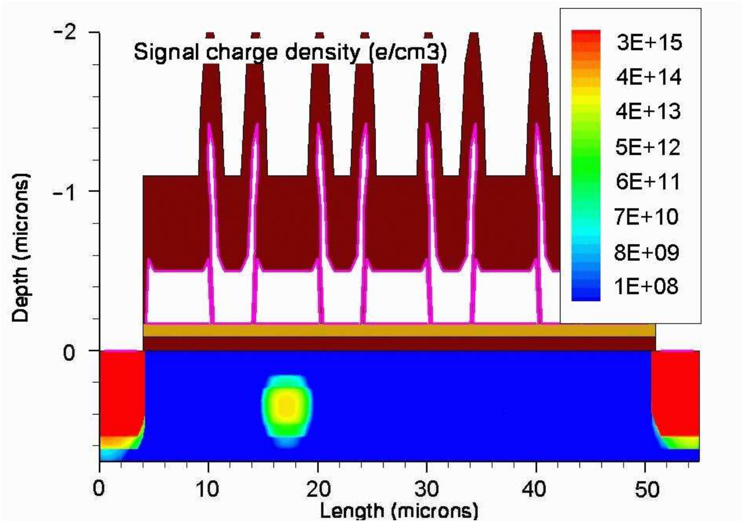

Figure 2. Signal charge density in transit. The plots shows the charged packet located under gate 1 at a depth of about 0.5 μm. The density is given in electrons per cm^3.

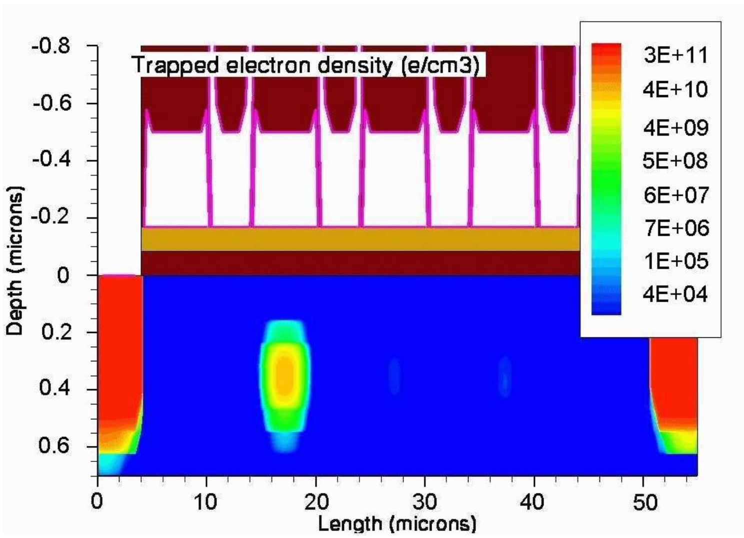

Figure 3. Trapped charge density. The plot shows the trapped charge density under gate 1. Note the difference in density scales between this figure and the previous one.

of the silicon being doped with phosphorus and a vacancy manifesting from the displacement of a silicon atom bonded with a phosphorus atom [2].

3. Results

The CTI dependence on temperature and readout frequency was explored. Figure 4 shows the CTI for simulations with partially filled 0.17 eV and 0.44 eV traps at different frequencies for temperatures between 130 K and 440 K, with a nominal clock voltage of 3 V. Continuous operation of the CCD means that the charge packet under investigation is affected by the previous charge packet, and the initially fully filled traps are emptying until the next charge packet arrives. At low tem-

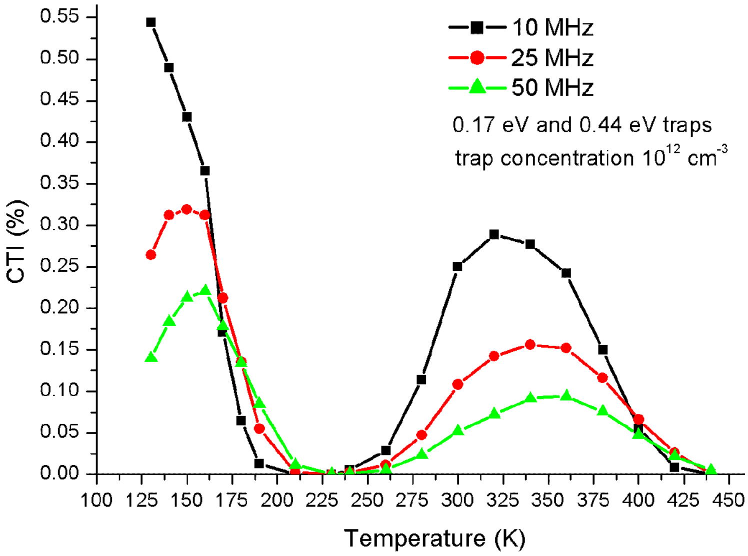

Figure 4. CTI values for 0.17 and 0.44 eV traps at readout frequencies 10, 25 and 50 MHz. A strong dependence of the CTI as a function of temperature is obtained. The 0.44 eV traps result in a peak structure between about 230 K and 450 K and for the 0.17 eV traps in the region below about 230 K. The optimal operating temperature is therefore around 230 K. Also noted is the shifts of the maximum CTI value, clearly visible for the 0.44 eV traps, to a lower temperature for decreasing frequency, as explained in the text.

peratures, the emission time constant τ_e, which characterizes the emptying of electrons from traps, can be very large and of the order of seconds. The charge shift time from one pixel to the next is of the order of nanoseconds. A larger τ_e means that a trap remains filled for much longer than the charge shift time. Further trapping of signal electrons is not possible and, consequently, CTI is small at low temperatures. A peak occurs between low and high temperatures because the CTI is also small at high temperatures. This manifests itself because, at high temperatures, the emission time constant decreases to become comparable to the charge shift time. Now, trapped electrons rejoin their signal packet.

Regarding the dependence of the readout frequency, the peak positions shift to lower temperatures as the frequency reduces. This is due to the fact that the charge shift time increases with decreasing frequency. Thus, there is a tendency that the trapped charge can rejoin the charge packet even at a lower temperature. The CTI value depends linearly on the trap concentration for a large concentration variation as also shown in figure 5.

The CTI values for a variation of the 0.17 eV trap level by 0.005 eV are shown in figure 6 for a readout frequency of 50 MHz. The trap energy level affects the emission time such that a deeper trap (larger trap energy level) results in a longer emission time which in turn leads to a larger CTI because fewer electrons can join the passing charge packet.

In the operation of the CPCCD only a small fraction of the pixels are hit. The occupancy depends on the design and operation of the detector and can vary to a large extent. It is therefore interesting to study how the occupancy affects the CTI. Figure 7 shows the CTI values for 0.1% and 1% hit (pixel) occupancy as a function of the operating temperature. At low temperatures a larger hit (pixel) occupancy leads to a larger filling of the traps before a charge packet arrives, and

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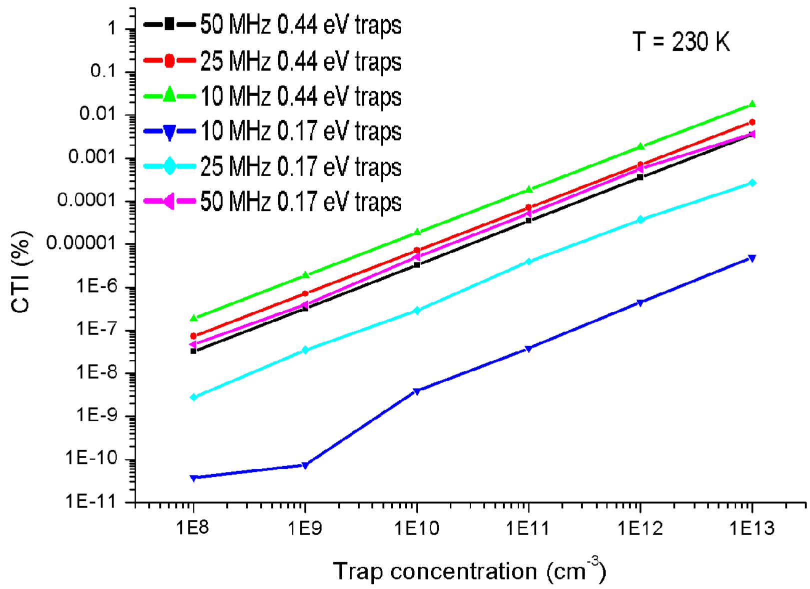

Figure 5. CTI values for a large range of trap concentrations. A largely linear increase of the CTI with trap concentration is observed.

thus fewer electrons can be trapped, which leads to smaller CTI values.

Another design aspect of the CCD development is the operating voltage. A low operating voltage is an advantage as the CCD then has a smaller power consumption. An optimization is needed in order to keep the CTI at an acceptable level. Figure 8 shows the CTI as a function of the operating temperature. The CTI sharply increases below a certain clock voltage depending on the temperature and the readout frequency. Very small CTI values are found for clock voltages above 1.6 and 1.7 V for readout frequencies of 1 and 20 MHz, respectively. A higher temperature results in lower CTI, and a higher frequency results in a larger CTI. The clock voltage where the sharp increase occurs depends strongly on the precise doping profiles of the CCD in the manufacturing process and therefore the given values are only an indication.

4. Comparisons with an analytic model

The motivation for introducing an analytic model is to understand the underlying physics through making comparisons with the TCAD simulations. This might then allow predictions of CTI for other CCD geometries without requiring a full simulation. An analytic model [6] has been adapted to the CPCCD characteristics. The analytic model was previously applied to a 3-phase CCD [6], hence, the CTI calculation included a factor three for the three gates. For this study the factor three is replaced by a factor two as the CPCCD is a 2-phase CCD with a two gate structure. Following the treatment by Kim [10], based on earlier work by Shockley, Read and Hall [11], a defect at an energy below the bottom of the conduction band has emission, τ_e, and capture, τ_c, time constants for electrons in the passing signal charge packet. This model considers the effect of a single trap level and includes the emission and capture time constants in the following differential equation

$$\frac{dn_t}{dt} = -\frac{n_t}{\tau_e} + \frac{N_t - n_t}{\tau_c} \tag{4.1}$$

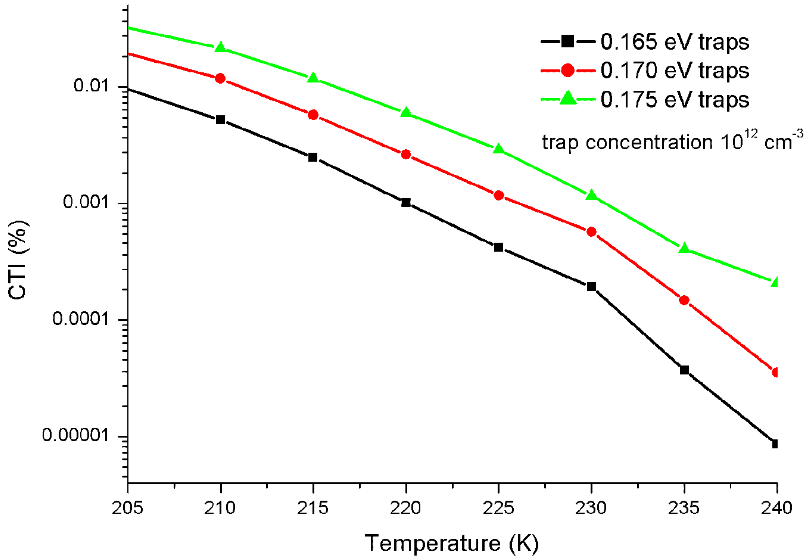

Figure 6. CTI values for 0.165, 0.170 and 0.175 eV traps for a fixed trap concentration of 10^{12} electrons per cm^3 and 50 MHz readout frequency. The effect of a small variation of the trap energy level on the CTI is shown. Higher trap energy levels ("deeper traps") lead to larger CTI values.

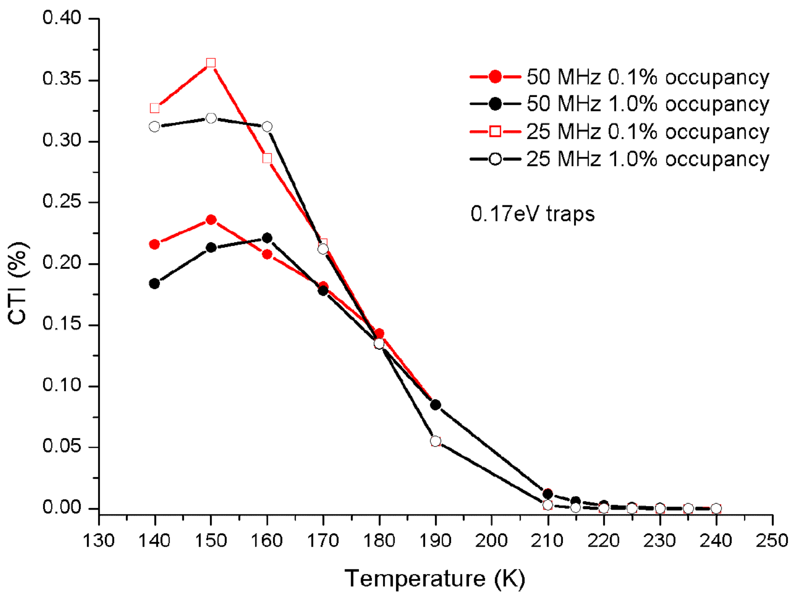

Figure 7. CTI values for 0.1% and 1% hit (pixel) occupancy for 0.17 eV traps. For low temperatures a tendency of a smaller CTI value is observed with increasing occupancy. This is because more traps are filled before a charged packet arrives and thus fewer electrons can be trapped.

where n_t is the density of filled traps, and N_t is the density of traps. For a realistic description of the CPCCD in operation, the traps are initially filled for this model, and the filling reduces exponentially until the next charge packet arrives. In order to be consistent with the DESSIS simulation (that uses partially filled traps), the analytic model uses a time constant such that the traps remain

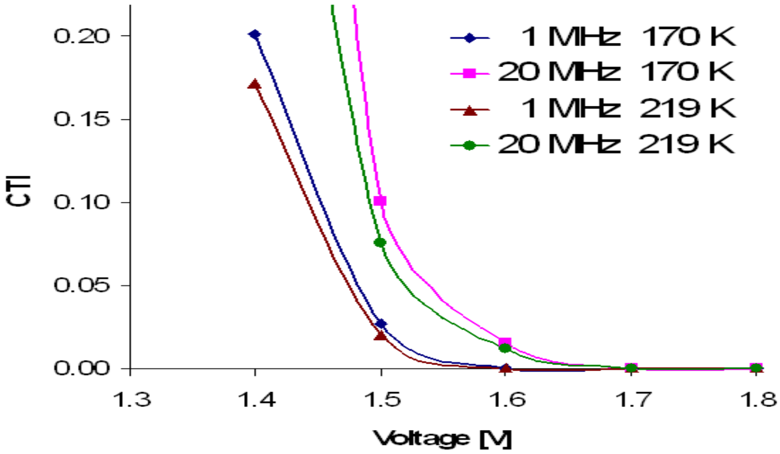

Figure 8. Clock voltage induced CTI. Two tendencies are observed, a higher operating temperature results in lower CTI, and a higher operating frequency results in a larger CTI. The CTI sharply increases below a certain clock voltage depending on the operating temperature and the readout frequency. The clock voltage where the sharp increase occurs depends strongly on the precise doping profiles of the CCD in the manufacturing process and therefore the given values are only an indication.

partially filled. The solution of this differential equation leads to an estimator of the CTI

$$CTI = \left(1 - e^{-t_{\rm sh}/\tau_{\rm c}}\right) \frac{2N_{\rm t}}{n_{\rm s}} \left(e^{-t_{\rm join}/\tau_{\rm e}} - e^{-t_{\rm emit}/\tau_{\rm e}}\right) \tag{4.2}$$

where $n_{\rm s}$ is the density of the signal charge packet, $t_{\rm join}$ is the time period during which the charges can join the parent charge packet, and $t_{\rm emit}$ is the total emission time from the previous packet, the mean waiting time between charge packets related to the mean occupancy of pixels in the device. This definition is for the CTI with a single trap level. The factor two in the formula appears as there is a sum over the two gates that make up a pixel. The Hardy model solution [12] does not have the terms inside the leftmost bracket, as in the Hardy model $\tau_{\rm c} \ll t_{\rm sh}$ was assumed.

Figure 9 compares the full TCAD simulation for 0.17 eV traps and readout frequency of 50 MHz to the results of the analytic model. It shows reasonably good agreement between the analytic model and the full simulations.[1] The variation of hit occupancy has been studied and as expected at lower temperatures larger hit occupancy leads to lower CTI values as more traps are filled before the charge packet passes. At higher temperatures where the CTI is reducing, no significant effect of the occupancy on the CTI is observed.

The agreement between the analytic model and the full simulation gives confidence that the physics of the CTI origin is understood and described with a precision useful for predictions. While the full TCAD simulation requires several CPU days of computing per data point, very similar results are obtained almost instantaneously with the analytical description. However, there are limitations with the analytic model. It does not consider the wave form of the readout voltage which was used in the full simulation. Furthermore, the analytic model assumes that the charge moves instantaneously from one pixel to the next and does not consider edge effects in the charge transfer. These effects are currently being studied with the goal of improving the analytic model.

[1]For temperatures below 140 K the full simulation does not converge.

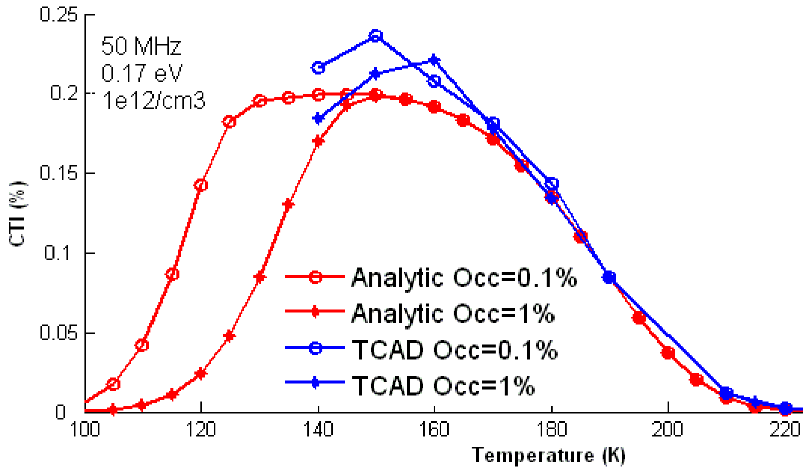

Figure 9. CTI values for 0.17 eV traps at readout frequency 50 MHz. Comparison of the analytic model with the full TCAD simulation for hit (pixel) occupancies of 0.1% and 1%.

Although the analytic model does not take into account the variation of the effective trap volume with temperature, studies showed this effect to be small. The effect of the shape of the signal packet in the context of the analytic model is also being studied.

5. Conclusions

The Charge Transfer Inefficiency (CTI) of a CCD with high-speed column parallel readout has been studied with a full simulation (ISE-TCAD DESSIS) and compared with an analytic model. The 0.17 eV and 0.44 eV trap levels have been implemented in the full simulation and variations of the CTI with respect to temperature and frequency have been analysed. At low temperatures ($<$ 230 K) the 0.17 eV traps dominate the CTI, whereas the 0.44 eV traps dominate at higher temperatures. Good agreement between simulations and an analytic model adapted to the CPCCD has been found. This gives an indication that the underlying physics of the radiation damage is well understood. The optimum operating temperature for the CPCCD in a high radiation environment is found to be about 230 K for readout frequencies in the range 10 to 50 MHz. Our prototype CPCCD has recently operated at 45 MHz and a test-stand for CTI measurements is in preparation. The development of a high-speed CCD vertex detector is on track as a vital part of a future ILC detector.

Acknowledgments

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