

## Design of a wideband low noise amplifier for radio-astronomy applications

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## Design of a wideband low noise amplifier for radio-astronomy applications

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**ABSTRACT:** In this work, we discuss the design of two low noise amplifiers (LNA) based on  $1\mu\text{m}$  gate-length pHEMT InP transistors using two topologies. Designed for radio-astronomy applications, the first is a cascode circuit with a maximum gain of 15dB and noise figure of 0.6dB, while the second is a 2-stage cascaded amplifier with 27 dB gain and 0.63dB noise figure. The two amplifiers exhibit an input 1-dB compression point of -22dBm and -26dBm respectively, and a third order input intercept point of -10dBm and -5dBm, respectively.

**KEYWORDS:** HEMT amplifiers; Modeling of microwave systems; Analogue electronic circuits

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## 1 Introduction

In the last few years, a good progress has been made in designing and implementing Microwave Monolithic Integrated Circuits (MMICs) employing compound semiconductors. One of the most exciting applications of this technology is the Square Kilometer Array (SKA) radio telescope. The SKA Design Studies (SKADS) is an international effort to investigate and develop technologies which will enable to build an enormous radio astronomy telescope with a million square metres of collecting area.

A large research effort has been conducted in improving electronic equipment performance used in astronomy. While a classic radio telescope uses only few receivers with cryogenically cooled transistors, the SKA telescope requires better devices to efficiently cover a large area. Since high electron mobility transistors (HEMT) achieve excellent noise figure, they have been dominating the field of radio astronomy [1, 2].

The low noise amplifier (LNA) is the closest device to the antenna and thus plays a key role in SKA receivers. It must provide low noise behaviour not only at one frequency but over the whole bandwidth of interest. The main purpose of the LNA is to increase the signal to noise ratio, i.e., amplifying the signal without adding significant noise to the output signal relatively to the input

signal (minimizing the noise contribution). Therefore, the noise figure (NF) is a crucial factor for LNA design. However, linearity is also a key factor in LNA performance [3–6].

The main objective of this work is small and large signal modelling of a novel pHEMT and its use in the design of an MMIC InP-pHEMT broadband LNA in the L-band (1-2 GHz) with the lowest possible noise figure and the gain response as flat as possible, as a part of the European SKADS.

In this paper, we focus on a 1-2 GHz LNAs for SKA receivers. To achieve the desired sensitivity, the LNA should exhibit a NF less than 0.6dB with a gain of at least 10 dB.

## 2 HEMT technology and characteristics

The fabricated high breakdown  $1\ \mu\text{m}$  InGaAs-InAlAs-InP pHEMT used in this work is shown in figure 1. Such transistor is suitable for radio-astronomy applications. It uses an advanced MBE (Molecular Beam epitaxy) growth technique and is a four finger device with  $200\ \mu\text{m}$  unit gate width and  $1\ \mu\text{m}$  gate length. More details about this HEMT can be found in [7, 8].

Looking at the structure from bottom to top, a lattice- matched undoped  $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$  buffer layer of  $4350\ \text{\AA}$  thickness, is grown on top of an InP semi insulating substrate. A highly strained, undoped  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ , channel is grown well below the critical thickness of this composition ( $140\ \text{\AA}$ ). The spacer is a lattice matched, undoped  $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$  layer of  $100\ \text{\AA}$  thickness used to spatially separate the heavily doped delta-region from the active channel. A supply layer  $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$  is formed with  $300\ \text{\AA}$  thickness to supply electrons into the 2DEG and the  $500\ \text{\AA}$   $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  cap layer.

The  $200\times 4$  pHEMT device is characterized by measuring its DC and RF performances in the frequency range of 0.1-50GHz. As shown in figure 2, typical drain source saturation current  $I_{\text{DSS}}$  of the fabricated device is 180 mA, while a maximum transconductance ( $g_{m,\text{max}}$ ) of 214mS/mm was measured at a drain voltage  $V_{\text{ds}}$  of 1 V and gate voltage  $V_{\text{gs}}$  of -0.84 V (figure 3).

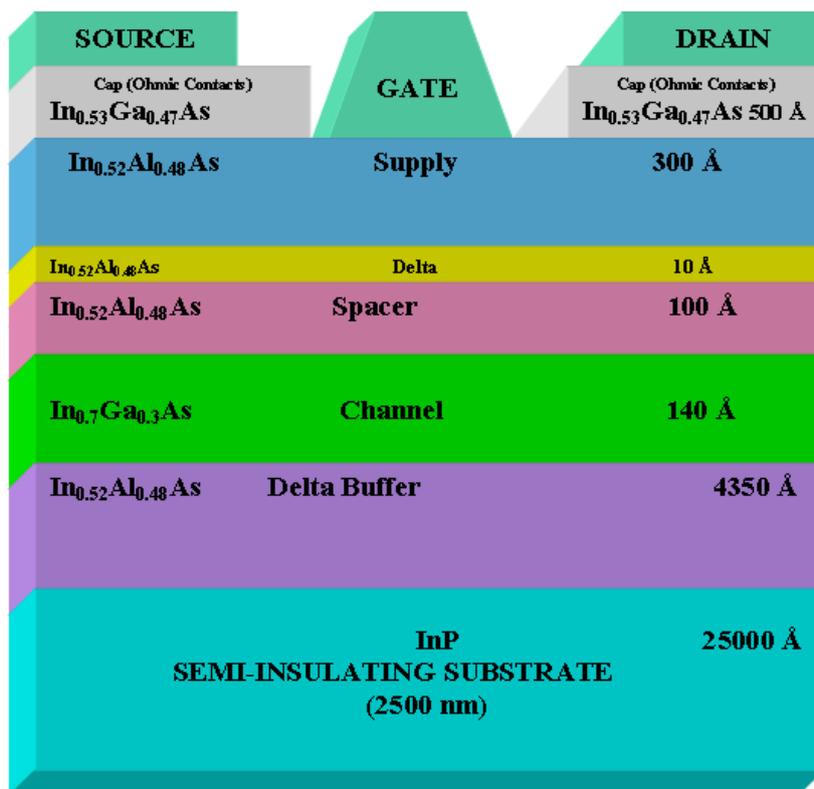
The curves of the gain ( $H_{21}$ ) and the maximum available gain (MAG) shown in figure 4 allow to graphically obtain the cut-off frequency ( $F_c$ ) and the maximum frequency of oscillation ( $F_{\text{max}}$ ) [8].

## 3 PHEMT device modelling

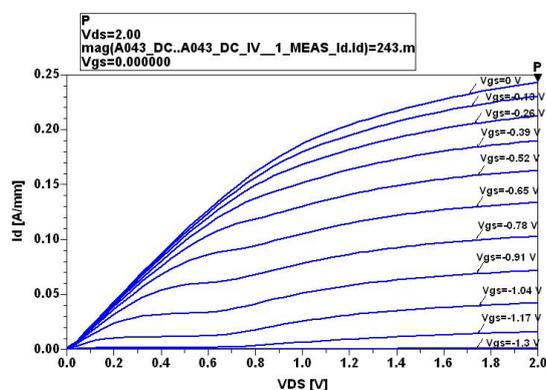
The design of LNAs requires small-signal modelling of the transistor [9–11]. In this work S-parameters measurements were carried out to obtain the parameters of the small-signal model of the transistor.

A simple approach to extract the extrinsic and intrinsic elements linear small signal model of HEMT devices is used in this work [12]. This approach uses two sets of S-parameter measurements at two different bias conditions. It consists of two main steps. In the first step, the bias-independent extrinsic parameters are extracted. In the second step, all other parameters are extracted at the bias point of interest. The extracted parameters are then optimized so that the modelled (reconstructed) S-parameters fits the measured data as accurately as possible using a commercial microwave CAD software package from Agilent technologies, (ADS2006).

The EE-HEMT nonlinear large signal model (model available in ADS shown in figure 5) is extracted using the device modelling and measurement automation software package, IC-CAP. Then the extracted model can be easily exported to ADS where optimization algorithms are applied until

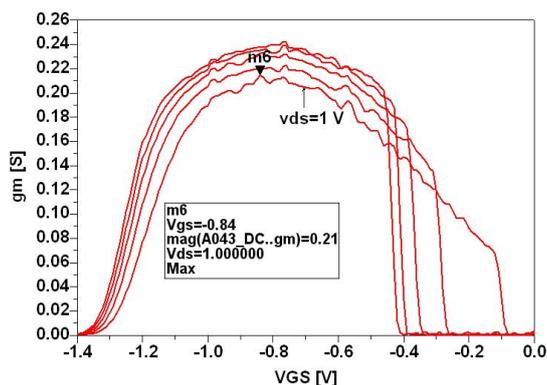


**Figure 1.** The epitaxial layer structure of the pHEMT used in this work to design radio frequency LNAs.

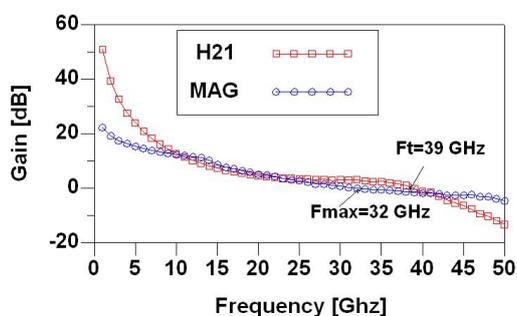


**Figure 2.** The HEMT drain current –voltage characteristics  $I_{ds}$  ( $V_{ds}$ ) for different gate voltages ( $V_{gs}$ ).

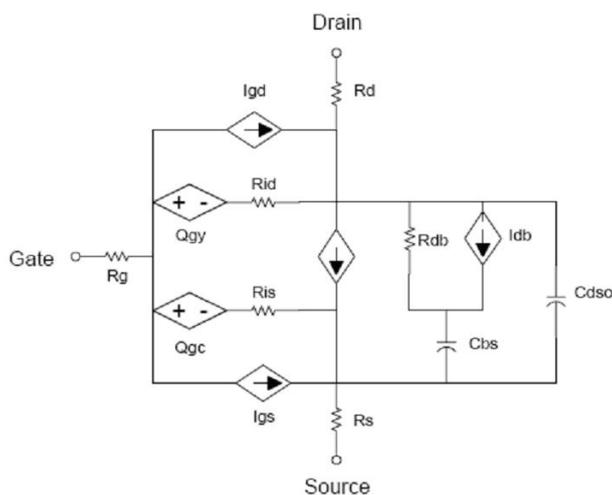
the modelled DC and RF characteristics of the device accurately fit the measured data. Comparisons, given in figure 6 and figure 7, between the measured and modelled DC and RF characteristics show excellent fits for the extracted nonlinear model.



**Figure 3.** The HEMT extrinsic transconductance ( $g_m$ ) versus the gate voltage.



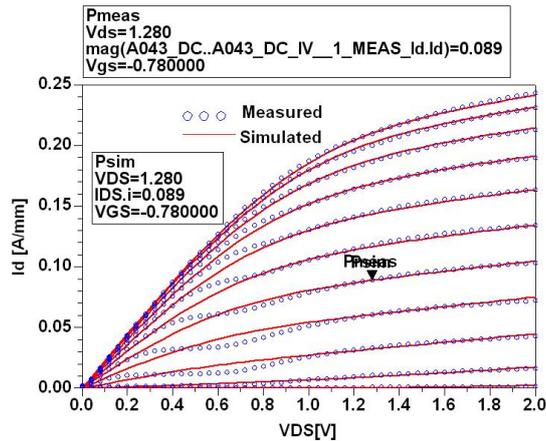
**Figure 4.** The Maximum Available Gain (MAG) and the gain ( $H_{21}$ ) versus frequency.



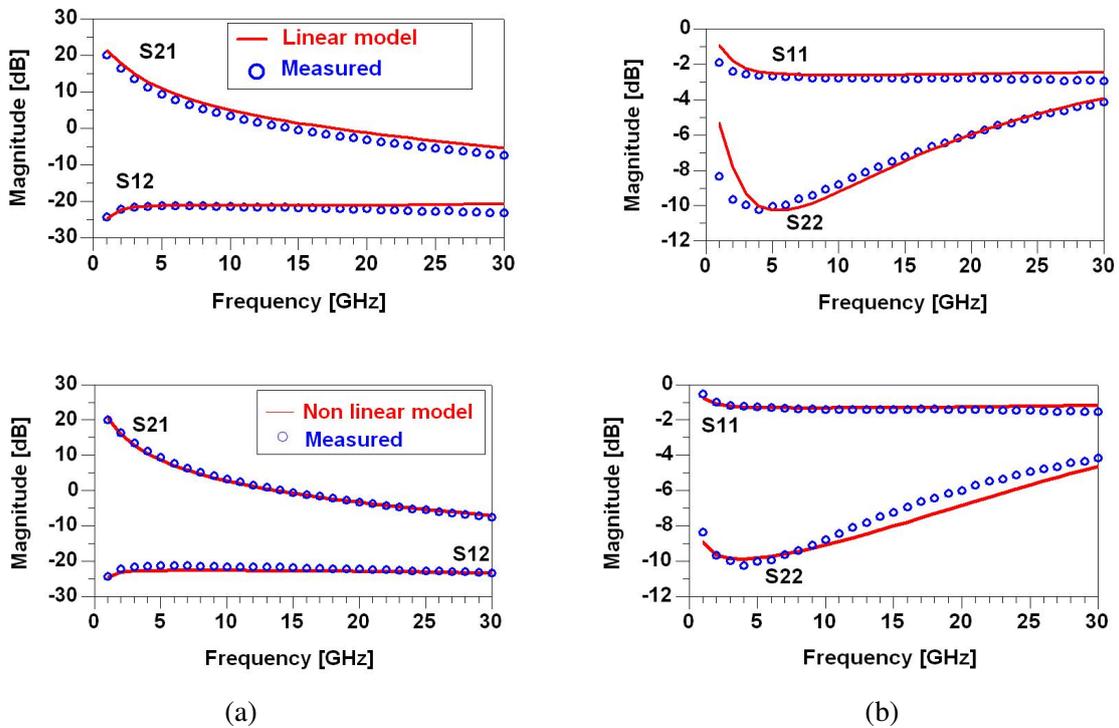
**Figure 5.** The equivalent circuit of the non linear Model of the Agilent EE-HEMT.

#### 4 Circuit design and theoretical analysis

We designed two LNAs with the same objectives, i.e., minimizing the noise figure and providing an acceptable gain with sufficient linearity [11–13].



**Figure 6.** Comparison between measured and modelled DC characteristics.



**Figure 7.** Comparison between measured and modelled RF characteristics (a): linear model, (b): non linear model.

Commonly used for broadband applications, the first circuit (figure 8-a) is a cascode source inductive degenerated structure which has already demonstrated its robustness [8, 10]. In fact, the cascode configuration allows good trade off between input matching and noise figure, as well as good stability by achieving good isolation between output and input, while the source inductive degeneration input architecture is widely used in LNA design [3, 11, 14–17] to minimise noise and maximize gain.

In the second circuit (figure 8-b), and in order to improve the performance by minimizing the noise figure and achieving a gain greater than 20 dB, a double stage cascaded amplifier is used. As for the bias network, passive components were preferred for their simplicity.

#### 4.1 Noise figure

The complete noise characterization of an active device requires the knowledge of four real parameters, i.e. minimum noise figure  $NF_{\min}$ , noise resistance  $R_n$ , the optimum source admittance ( $Y_{\text{opt}} = G_{\text{opt}} + jB_{\text{opt}}$ ) and the source admittance ( $Y_s = G_s + jB_s$ )

The noise figure for any source admittance  $Y_s$  can be expressed in terms of the above parameters

$$NF = NF_{\min} + \frac{R_n}{G_s} |Y_s - Y_{\text{opt}}|^2 \quad (4.1)$$

Three of the four parameters in equation (4.1) are fixed constants that are determined by the device characteristics at a given frequency, so the amplifier noise figure is completely determined by the source impedance  $Z_s$ . An LNA reaches its minimum noise figure, i.e., when its source impedance is equal to  $Z_{\text{opt}}$  [18–22], while the source impedance should be equal to the conjugate of the LNA's input impedance in order to achieve power matching as well to preserve the antenna filter's frequency response. Preferably, noise matching and power matching should be achieved simultaneously, i.e.,

$$Z_{\text{opt}} = Z_s^* \quad (4.2)$$

The noise performance of the proposed topology is due to two main factors: the losses of the input network and the noise of the active device  $T_1$ . Optimizing noise in a wideband (0.5-2 GHz) is not the same as for a single frequency. It is performed on the in-band average NF, as opposed to the spot NF (i.e., NF at the center frequency for the narrow-band case).

#### 4.2 Choice of bias conditions

As seen in figure 10, and in order to obtain a minimum noise factor, the behaviour of the LNA at different bias points is simulated (modelled as in figure 10, with dc drain current  $I_d$  equals to 10%, 20%, 30%, and 40% of the drain saturation current  $I_{\text{DSS}}$ ). It is noted that since the noise figure is inversely proportional to  $I_d$ , a large current would help minimising noise. However, such target cannot be realised without scarifying other important parameters such as gain, input/output return loss, power consumption and stability. An optimal value of  $0.2 \cdot I_{\text{DSS}}$  was selected for  $I_d$  with a noise figure only 0.2dB higher than the extrapolated one (figure 12).

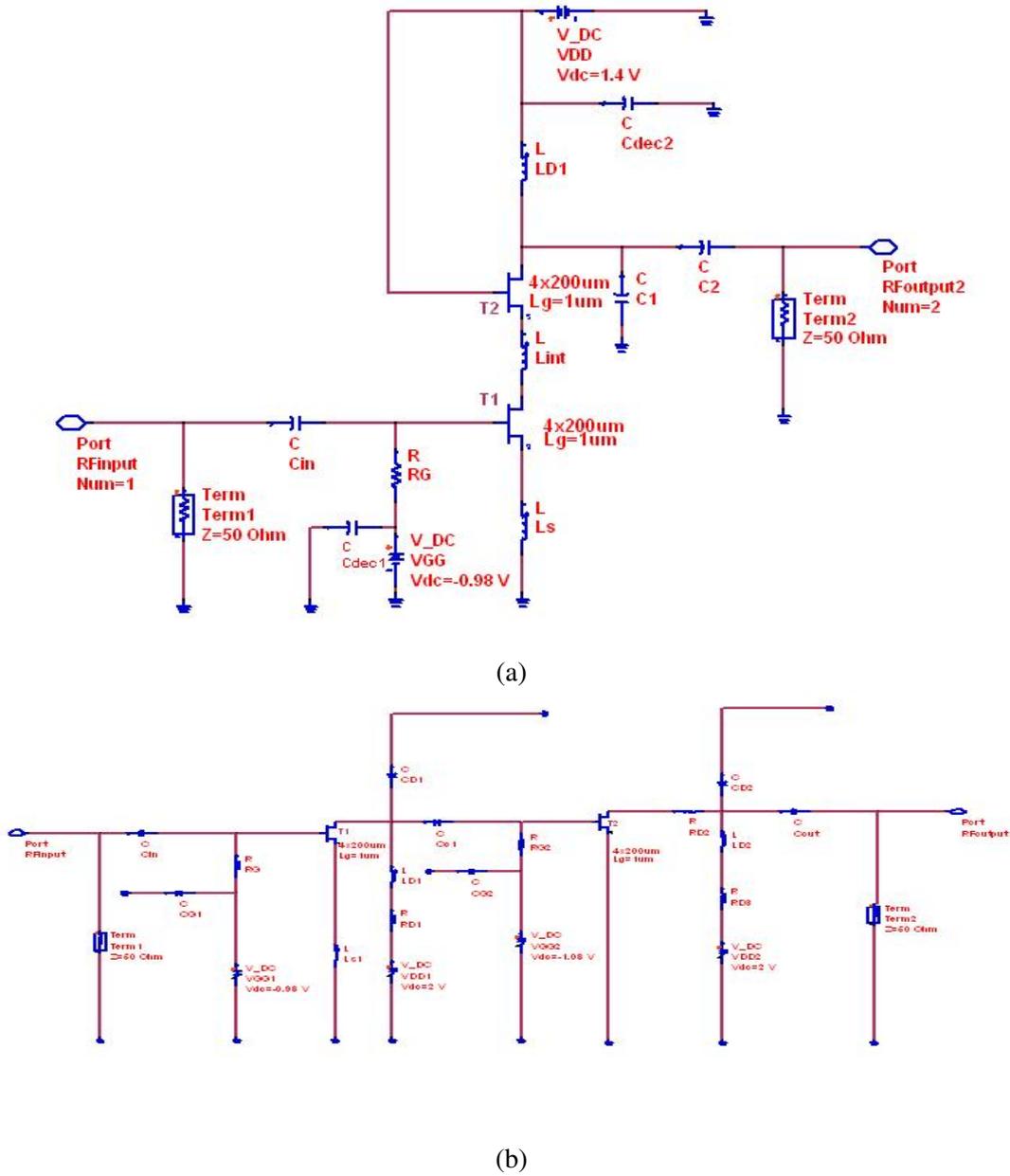
#### 4.3 Input impedance matching

From the circuit model shown in figure 11, the input impedance can be written as [19]

$$Z_{\text{in}} = \sum R + L_s \omega_T + j\omega L_s + \frac{1}{j\omega C_{gs1}} \quad (4.3)$$

$$\sum R = R_{i1} + R_{L_s} \quad (4.4)$$

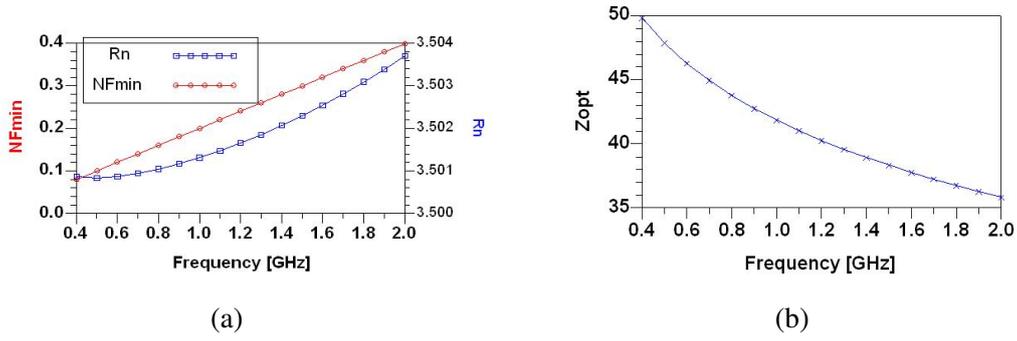
$$\omega_T = \frac{g_{m1}}{C_{gs1}} \quad (4.5)$$



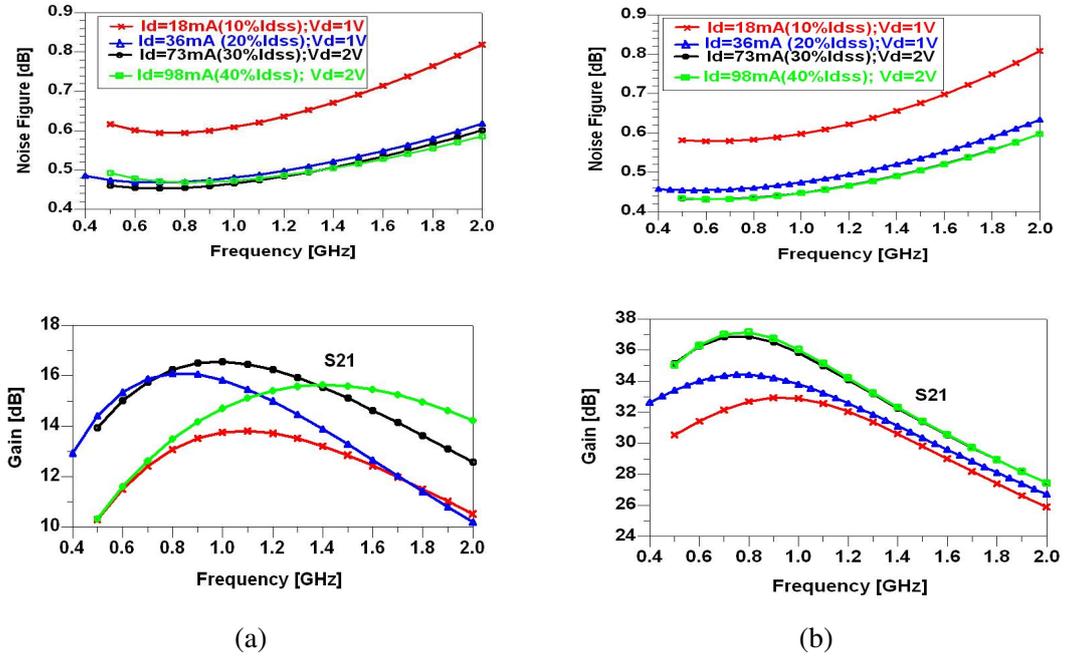
**Figure 8.** LNA proposed designs: (a) single-stage cascode and (b) two-stage cascode configurations.

Where the parameters  $g_{m1}$ ,  $C_{gs1}$ ,  $R_{i1}$  are respectively the transconductance, gate-source capacitance and distributed intrinsic resistor of transistor T<sub>1</sub>, and  $R_{L_s}$  the parasitic inductor series resistor of  $L_s$ . In the source degeneration topology, the input impedance  $Z_{in}$  at the resonance frequency  $f_o$  is purely real and proportional to  $L_s$ . Therefore, by choosing the appropriate value of the inductance  $L_s$ , the real term of the input impedance can be set equal to the source impedance ( $R_s = 50\Omega$ ). Thus, the resonance condition for real input impedance is given by the relation

$$f_o = \frac{1}{2\pi\sqrt{C_{gs1}L_s}} \quad (4.6)$$



**Figure 9.** Noise characterization of an InP pHEMT device: (a): Noise resistance ( $R_n$ ): minimum noise figure ( $NF_{min}$ ); (b): Optimum impedance for noise match  $Z_{opt}$ .



**Figure 10.** Influence of bias conditions ( $I_d$ ,  $V_d$ ) on the noise factor and the gain: (a) single stage cascode , (b) two-stage cascaded LNA.

with no reactive part for  $Z_{in}$  and with a real part approximately equals to

$$R_{in} \approx \omega_T L_S \quad (4.7)$$

The gain of the amplifier is then maximized.

#### 4.4 Interstage impedance

The cascode configuration reduces the Miller effect and provides good output isolation. Adding  $L_{int}$  can further reduce the Miller capacitance of  $T_1$ , increasing isolation. Figure 11 shows the small



Where  $\Gamma_s$ ,  $\Gamma_l$ ,  $\Gamma_i$ , and  $\Gamma_o$  represent the source, load, input, and output reflection coefficients respectively. With proper rearrangement, (4.10)–(4.13) result in the following two conditions:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \quad (4.15)$$

$$|\Delta| < 1 \quad (4.16)$$

where  $K$  is the Rollet or stability factor. Note that (4.15) and (4.16) are derived for a single-stage amplifier. Note that for multistage configurations, the conditions of stability should be applied to each stage (each input/output impedance should belong to its related stable region).

In this work, the circuits in figure 8 were used to evaluate the circuit stability. Due to the source degeneration, considered as a negative feedback at the frequencies of interest, the proposed amplifier satisfies the unconditionally stable conditions.

## 4.6 Gain analysis

### 4.6.1 Gain of the cascode amplifier

Figure 11 shows the circuit of the cascode amplifier used to calculate the voltage gain based on

$$V_{in} = \left( \frac{1}{sC_{gs1}} + R_{i1} + Z_{Ls} + g_{m1} \frac{Z_{Ls}}{sC_{gs1}} \right) i_{in} \quad (4.17)$$

$$V_{D1} = \left( (sL_{int} + Z_{i2})g_{m1} \frac{1}{sC_{gs1}} + Z_{i2} \frac{g_{m1}g_{m2}}{sC_{gs1}(sC_{gs2} + g_{m2})} \right) \cdot i_{in} \quad (4.18)$$

$$V_{out} = L_{d2} \cdot \frac{g_{m1}g_{m2}}{C_{gs1}(pC_{gs2} + g_{m2})} i_{in} \quad (4.19)$$

where

$$Z_{Ls} = R_{Ls} + sL_s, \quad Z_{i2} = R_{i2} + \frac{1}{sC_{gs2}}$$

The gain of the first stage is given by

$$A_{v1} = \frac{V_{D1}}{V_{in}} \approx \frac{L_{int}}{L_s} \quad (4.20)$$

While the gain of the second stage is approximated by

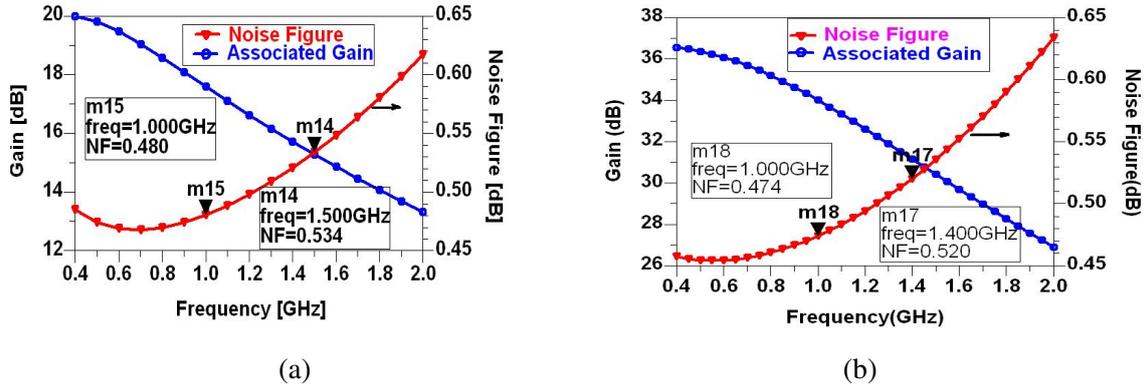
$$A_{v2} = \frac{V_{out}}{V_{D1}} \approx \frac{g_{m2} \cdot pL_{D2}}{pL_{in} + Z_{i2}} \approx \frac{L_{D2}}{L_{in}} \quad (4.21)$$

Therefore, the total gain is the ratio of the inductor at the drain to the inductor at the source. Thus, a high gain can be easily achieved by setting the load inductor to be much higher than the degeneration inductor.

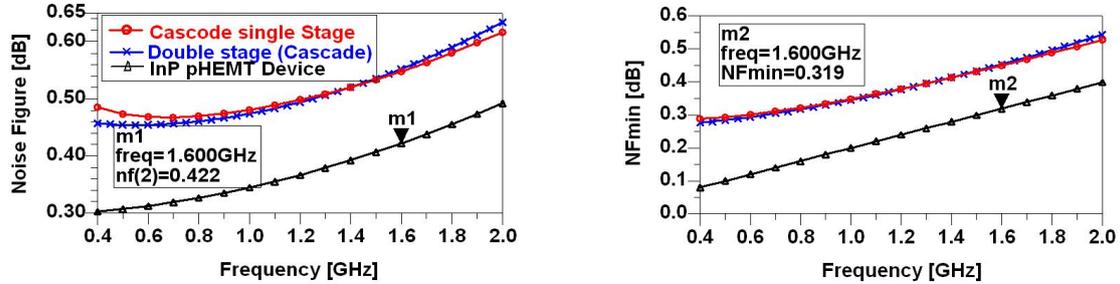
### 4.6.2 Gain of the cascade amplifier

Two cascaded common-source stages were needed to reach the LNA specifications. The first stage was designed for minimum noise while the second was for high gain. We can write

$$V_{out1} = -\frac{g_{m1}sL_{D1}}{C_{gs1}} i_{in} \quad (4.22)$$



**Figure 12.** Variations of associated gain and noise figure vs. frequency for (a) the cascode single stage, (b) the two-stage cascaded LNA.



**Figure 13.** Noise figure of the two configurations and the InP device.

Therefore, the gain of the first cascaded stage is given by:

$$\frac{V_{out1}}{V_{in}} = \frac{-g_m s L_{D1}}{1 - \omega^2 L_s C_{gs1} + s(R_{i1} C_{gs1} + g_m L_s)} \quad (4.23)$$

At the resonance, it becomes

$$\frac{V_{out1}}{V_{in}} = \frac{-g_m L_{D1}}{R_{i1} C_{gs1} + g_m L_s} \quad (4.24)$$

In order to improve the noise figure, the first stage should be designed with a low noise figure and high gain to suppress the noise contribution of the next stage. The degeneration inductance should be carefully selected for noise and gain matching considerations.

#### 4.7 Linearity

In RF circuit design, the linearity is another important parameter that needs to be considered. Since the LNA is the first block in a typical receiver system, the linearity of the LNA is commonly estimated by the third-order intermodulation (IM3) product. Two signals of adjacent channels  $A \cdot \sin \omega_1$  and  $A \cdot \sin \omega_2$  will generate IM3 products such as  $A \cdot \sin(2\omega_1 - \omega_2)$  and  $A \cdot \sin(2\omega_2 - \omega_1)$  at

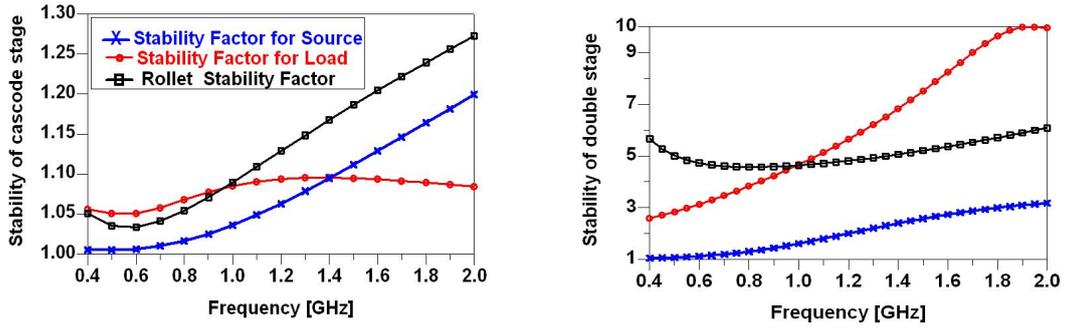


Figure 14. Stability of LNAs.

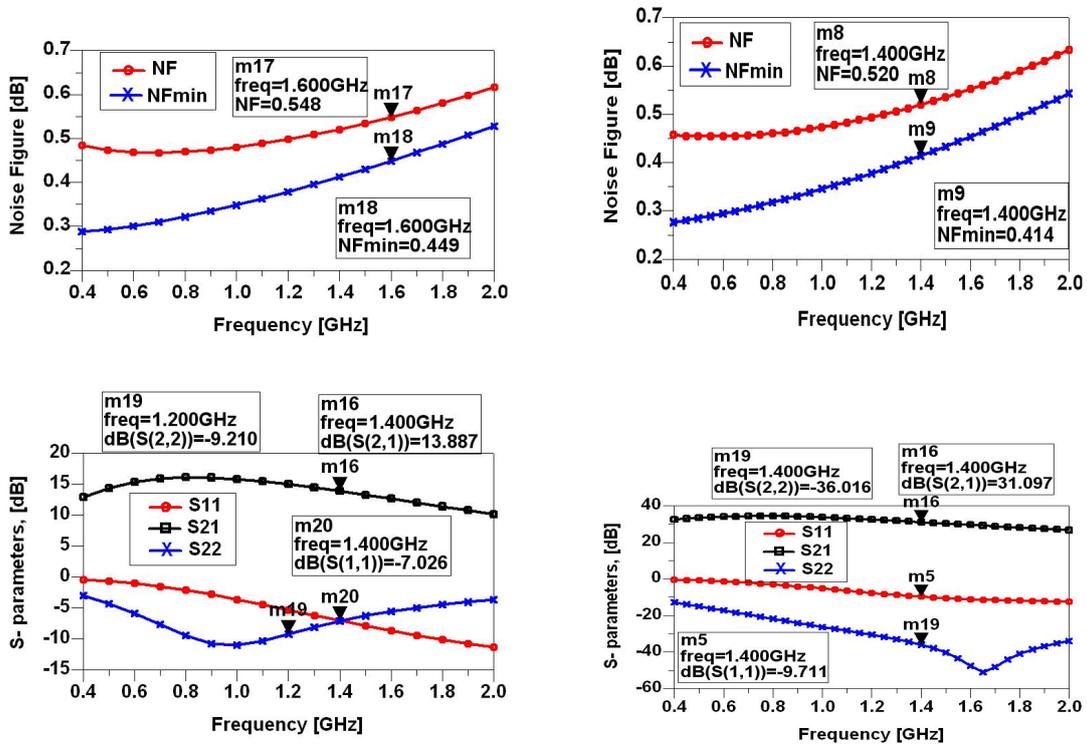
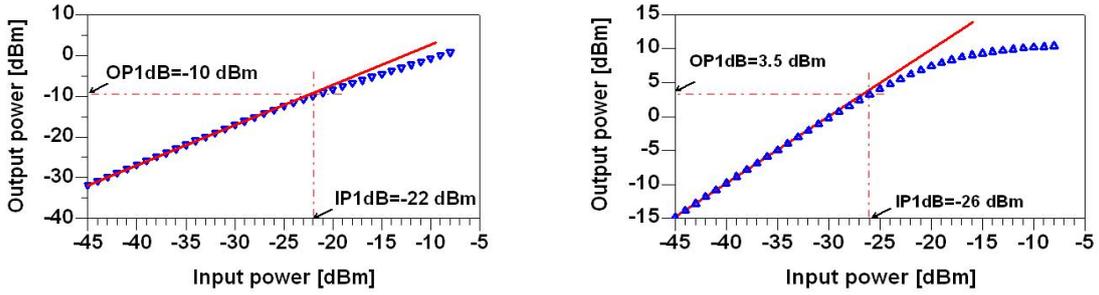


Figure 15. Simulated LNA performances: S-parameters and Noise Figure (a) Cascode stage, (b) double stage cascaded amplifier.

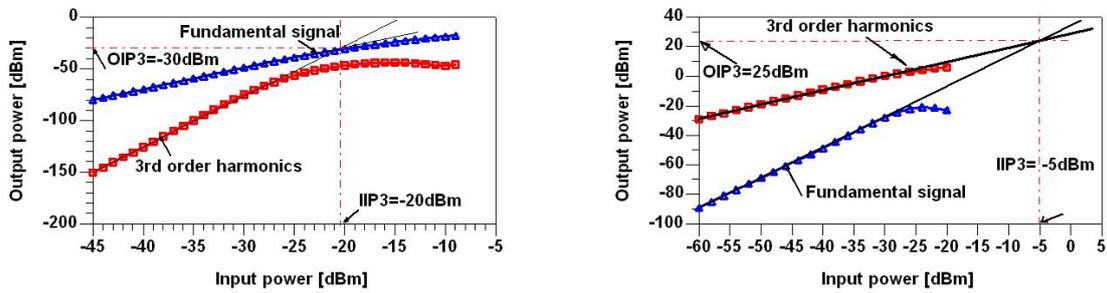
the output of the nonlinear circuit. It is usually evaluated as [22, 23]

$$IM3 = \frac{3}{4} A^2 \left| \frac{A_3(2\omega_1 - \omega_2)}{A_1(\omega)} \right| \quad (4.25)$$

where  $A_1$  and  $A_3$  are the first- and third-order Volterra series coefficients, respectively. Therefore, the linearity considers only the input 1-dB compression point (P1dB) and the input third-order intercept point (IIP3). In a common source amplifier biased in saturation region, its small-signal



**Figure 16.** 1-dB compression point for the (a) cascode single stage, (b) the two-stage cascaded LNA.



**Figure 17.** Simulated results for IIP3 under the two tones input of 1.4 and 1.6 GHz. for (a) cascode single stage, (b) for the two-stage cascaded amplifier.

output current can be expressed as the following power series:

$$i_D(V_{gs}) = g_{m1}V_{gs} + g_{m2}V_{gs}^2 + g_{m3}V_{gs}^3 + \dots \quad (4.26)$$

where the first order coefficient  $g_{m1}$  is the small-signal transconductance and  $g_{m,i}$  ( $i \geq 2$ ) is the  $i^{\text{th}}$  order coefficient of the transfer characteristics, and  $V_{gs}$  the input voltage. Among these coefficients,  $g_{m3}$  is the dominant factor for determining the IIP3 at a low signal level.

## 5 Simulation results and discussion

The proposed wideband LNAs were simulated using the ADS circuit simulation tool [24] (figures 12, 13, 14 and 15). With a bias point of  $V_{ds} = 1V$  and  $I_D = 36mA$  ( $I_D = 0.2 * I_{DSS}$ ),  $V_{ds} = 1V$  and  $I_D = 20mA$  for the second LNA architecture, input/output return losses below  $-5dB$  and a power gain higher than  $10dB$  for the first circuit were obtained. As for the two-stage cascaded amplifier, a gain of  $27dB$  was achieved with an output return loss below  $-26dB$  and an input return loss lower than  $-5dB$ . The circuits also showed unconditional stability up to  $30 GHz$  with a total power dissipation of  $72 mW$  and  $55 mW$ . The cascode stage and double stage common-source operating from a  $1.4 V$  and  $2 V$  power supply respectively were designed to include the on-chip output matching network. The simulated results obtained including the effects of series resistances of on-chip inductors

**Table 1.** Performance comparisons with other LNAs designs for SKA receivers.

	Unit	This work		[1]	[2]	[5]	[19]	[20]
		LNA1	LNA2					
<i>Freq</i>	GHz	1-2	1-2	.8-1.8	.6-1.6	.6-1.6	.7-1.5	.8-1.4
<i>NF</i>	dB	< .6	< .6	< 1	< .5	< 1.2	< .6	.2
<i>NF<sub>min</sub></i>	dB	< .5	< .5	.8	.45		.45	*
<i>Gain<sub>max</sub></i>	dB	> 11	> 27	> 23	> 21	> 23	> 18	> 17
$ S_{11} $	dB	< -4	< -5	*	< -11	< -15	< -15	< -11
$ S_{22} $	dB	< -4	< -26	*	*	*	*	< -7
<i>IP<sub>1dB</sub></i>	dBm	-22	-26	*	*	*	*	*
<i>OP<sub>1dB</sub></i>	dBm	-10	3.5	*	*	*	*	2
<i>IIP<sub>3</sub></i>	dBm	-20	-5	*	*	*	*	*
<i>OIP<sub>3</sub></i>	dBm	-30	25	15	15	5.7	*	12
<i>V<sub>DD</sub></i>	V	1.4	2	*	*	*	*	1
<i>P<sub>DC</sub></i>	mW	72	55	90	850	110	50	43
<i>Topology</i>	-----	<i>Cascode</i>	<i>Cascaded</i>	<i>Cascode</i>	<i>DLNF<sup>1</sup></i>	<i>DLRF<sup>2</sup></i>	<i>Cascode</i>	<i>cascode</i>
<i>Technology</i>	-----	<i>1 μm pHEMT (InP)</i>	<i>1 μm pHEMT (InP)</i>	<i>.18 μm CMOS</i>	<i>.2 μm pHEMT GaAs</i>	<i>.35 SiGe</i>	<i>.18 μm CMOS</i>	<i>.09 μm CMOS</i>
<i>Meas/sim</i>	-----	<i>sim</i>	<i>sim</i>	<i>meas</i>	<i>sim</i>	<i>sim</i>	<i>sim</i>	<i>meas</i>

[20] input is matched to 85 ohms.

<sup>1</sup> DLNF: Dual Loop Negative Feedback, Power to power.

<sup>2</sup> DLRF: Dual Loop Resistive Feedback Power to current.

Meas/sim: measured/simulated.

A minimum noise figure slightly below 0.6dB with associated gain above 15 dB at mid-bands was obtained. Table 1 summarizes the performances of the two designed circuits. The 1-dB compression point of the LNA was also simulated (figure 16). It was found to be -22dBm and -26dBm at 1.5 GHz for the single-stage cascode and the two-stage cascaded amplifiers, respectively. The simulated input third order intercept point (IP3) shown in figure 17 was -20dBm and -5dBm for the single-stage cascode amplifier and the two-stage cascaded amplifier, respectively. Table 1 also compares both simulations and measurements to other designs reported in the literature, showing the competitiveness of this design in low noise bandwidth for SKA receivers.

Since our amplifiers were designed for radio-astronomy applications, all passive components are on chip, exhibiting a low noise figure (<0.6dB) over an acceptable wideband frequency range (1-2GHz).

It is noted that since submicron devices are prone to oscillations at low frequencies, the designed circuit based on these devices could be highly unstable at the frequency operation range. Large periphery transistors (device used in this work) are needed for low noise resistance and wideband operation especially at frequencies lower than 2GHz. For these reasons, a high breakdown InGaAs-InAlAs pHEMT device was used [7].

The excellent low noise characteristics of the InP-based HEMT make it a natural choice for usual low noise applications. However, manufacturing at large scale production is difficult due to limited size, high cost and brittle nature the InP substrate. Furthermore, achieving a noise figure value close to the minimum noise figure across a wide frequency band is significantly more

complicated. Thus, by using an inductive degeneration in our wideband application, a noise figure very close to the minimum noise figure ( $NF \approx NF_{\min} + 0.1\text{dB}$ ) is obtained and with a reduced input VSWR.

Compared to published results, the proposed designs exhibit excellent performances (table 1). Indeed our simulations demonstrated the high performance of our circuits while compared to other simulated or measured results. The circuits will be later integrated in radio astronomy and wireless communication systems.

## 6 Conclusion

In this paper, two different LNA topologies using  $4 \times 200\mu\text{m}$  InP pHEMTs have been designed for SKA telescope requirements. The first configuration is a cascoded single-stage amplifier while the second is a two-stage cascoded amplifier. The designed circuits satisfy most of the desired specifications, providing a noise figure very close to the transistor minimum noise figure with adequate gain and return loss. However, by using inductive degeneration, achieving low noise figure led to relatively high input voltage standing wave ratio. The designed circuits will be later integrated in radio astronomy and wireless communication systems using the fabricated transistor as well as the on-chip matching networks.

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