SMALL-SIGNAL MODELING OF PHEMTS AND ANALYSIS OF THEIR MICROWAVE PERFORMANCE

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ABSTRACT

Accurate extraction of the small-signal equivalent circuit elements of pseudomorphic high electron mobility transistors (pHEMT) is crucial for the design of microwave analog circuits such as low noise amplifiers (LNAs). This paper presents a direct analytical extraction procedure. Its efficiency is demonstrated on two different 1µm gate-length novel high breakdown InGaAs/InAlAs pHEMTs: one is grown on a GaAs while the other is on an InP substrate.

KEYWORDS: small signal modelling, pHEMT, extraction.

1 INTRODUCTION

Microwave amplifiers constitute an area of prime interest for the high-frequency industry. Most of them use III-V semiconductors such as Gallium Arsenide (GaAs) and Indium Phosphide (InP) because of their higher performance in terms of gain and noise. At the component level, pseudomorphic heterojonction transistors (pHEMTs) are widely used in monolithic microwave integrated circuits (MMICs) because of its superior electron mobility compared to classic F. The InAlAs/InGaAs material system provides one of the highest transconductance pHEMT devices because of its large conduction band discontinuity, high electron mobility and very good carrier confinement in the channel. The aim of this paper is the modelling of such transistors subsequently used to design a low-noise amplifier.

2 SMALL SIGNAL EQUIVALENT CIRCUIT

One of the most widely used small-signal HEMT equivalent circuit is presented in figure 1 [1-3]. This equivalent circuit is usually made of two parts: the intrinsic and the extrinsic circuits. The intrinsic part corresponds to the active area of the transistor, i.e., the channel. The extrinsic part corresponds to the connecting zones (access lines and electrode components).

3 EXTRACTION OF SMALL SIGNAL PARAMETERS

Determination of the elements of a linear model is based on an experimental characterization of the transistor. The small-signal extraction method proposed in this paper is based on S-parameters measurements. It involves the use of two sets of measurements at different bias conditions: pinched or cold and hot device measurements. The measured S matrix is converted to an impedance matrix (Z) whose elements Z_{ij} have real and imaginary parts: Real(Z_{ij}) and Imag(Z_{ij}) [4]. The extrinsic elements can be obtained from S-parameters measurements under cold and pinched off biasing conditions: a zero drain source voltage V_{ds} and a gate source voltage much lower than the pinch-off voltage V_p (i.e., V_{ds} = 0V and $V_{gs} << V_p$). In fact, cold pinched off bias conditions can simplify the topology of the small signal equivalent circuit as shown in figure 2.

In order to simplify the circuit analysis, the π circuit model in figure 2 can be transformed to a T circuit [5-6] as shown in the insert of figure 2. Thus, the z–parameters zpij can be expressed as

$$Z_{p11} = R_g + R_s + j*[\omega(L_g + L_s) - \frac{1}{\omega}(\frac{1}{C_g} + \frac{1}{C_s})] \quad (1)$$

$$Z_{p12} = Z_{p21} = R_s + j*[\omega L_s - \frac{1}{\omega C_s}] \quad (2)$$

$$Z_{p22} = R_d + R_s + j*[\omega(L_d + L_s) - \frac{1}{\omega}(\frac{1}{C_s} + \frac{1}{C_d})] \quad (3)$$

where the subscript p is the pinched off condition.

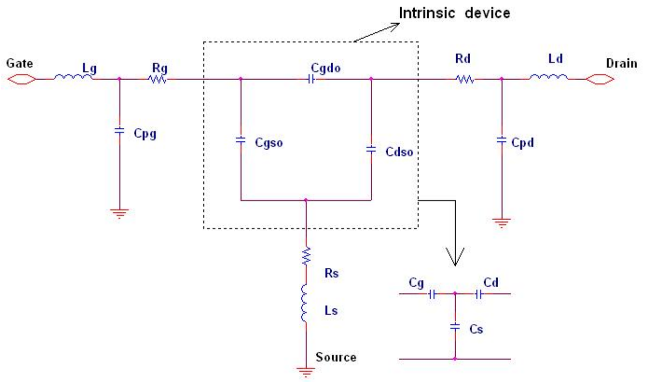


Figure 1: The small signal equivalent circuit of a HEMT

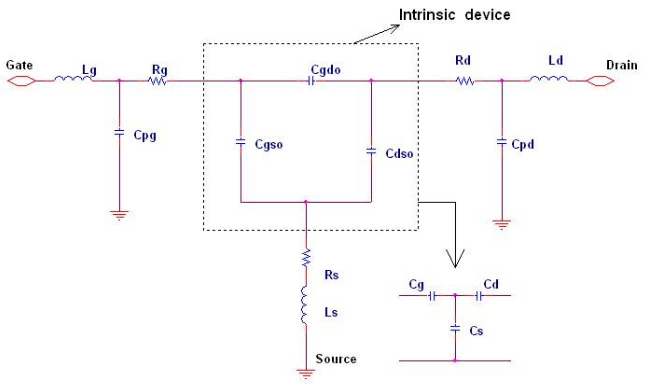


Figure 2: The mall signal equivalent circuit of a HEMT at zero drain bias and gate voltage below pinch-off

The three capacitances Cg, Cs and Cd are then given by Kennely theory de (triangle-star transformation) [see for example 5-7]:

$$C_g = C_{gso} + C_{gdo} + \frac{C_{gso}C_{gdo}}{C_{dso}} \quad (4)$$

$$C_s = C_{gso} + C_{dso} + \frac{C_{gso}C_{dso}}{C_{gdo}} \quad (5)$$

$$C_g = C_{gso} + C_{gdo} + \frac{C_{gso}C_{gdo}}{C_{dso}} \quad (6)$$

The parasitic resistances R_g, R_s, and R_d can be deduced from the real part of (1), (2), and (3) [7]. The parasitic inductances L_g, L_s, and L_d can be extracted from the slope of the curve of "ω*Imag(Z_{pij})" versus ω^2 [5], [7-9]. When the conduction in the channel is removed (i.e. deeply in pinch off $V_{ds} = 0$, $V_{gs} << V_p$), it is possible to extract the parasitic (extrinsic) capacitances: C_{pg} and C_{pd}. Note that for frequencies of some GHz, the effects due to parasitic inductances and resistances can be neglected and thus, have little influence on the imaginary parts of the admittance matrix, assuming C_{gso}=C_{gdo} and neglecting C_{ds} [1, 4, 6, 9-10]. We can write these equations as:

$$C_{pg} = \frac{\mathrm{Imag}(Y_{11}) + 2*(\mathrm{Imag}(Y_{12}))}{\omega} \quad (7)$$

$$C_{pd} = \frac{\mathrm{Imag}(Y_{22}) + \mathrm{Imag}(Y_{12})}{\omega} \quad (8)$$

Once all the extrinsic elements are determined, we can directly extract the intrinsic elements (Ri, Cgs, Cgd, Rds, Cds, Gm and τ) from the intrinsic Y-parameters according to the expressions proposed in [1-2, 7, 10-12].

$$C_{gs} = \frac{(1+d_1^2)}{\omega} * (\mathrm{Imag}(Y_{int11}) + \mathrm{Imag}(Y_{int12}) \quad (9)$$

$$R_i = \frac{d_1}{(1+d_1^2) * (\mathrm{Imag}(Y_{int11}) + \mathrm{Imag}(Y_{int12})} \quad (10)$$

$$C_{gd} = -\frac{(1+d_2^2)}{\omega} \mathrm{Imag}(Y_{int12}) \quad (11)$$

$$R_{gd} = -\frac{d_2}{(1+d_2^2) * \mathrm{Imag}(Y_{int12})} \quad (12)$$

$$C_{ds} = \frac{\mathrm{Imag}(Y_{int22}) + \mathrm{Imag}(Y_{int12})}{\omega} \quad (13)$$

$$g_{ds} = \mathrm{Real}(Y_{int22}) + \mathrm{Real}(Y_{int12}) \quad (14)$$

$$g_m = |G_m| \quad (15)$$

$$\tau = -\frac{1}{\omega} \angle(G) \quad (16)$$

where

$$d_1 = \frac{\mathrm{Real}(Y_{int11}) + \mathrm{Real}(Y_{int12})}{\mathrm{Imag}(Y_{int11}) + \mathrm{Imag}(Y_{int12})}$$

$$d_2 = \frac{\mathrm{Real}(Y_{int12})}{\mathrm{Imag}(Y_{int12})}$$

$$G = g_m * \exp(-j\omega\tau) = (Y_{int21} + Y_{int12})(1 + j * d_1)$$

4 DESCRIPTION OF DEVICE

The fabricated high breakdown InGaAs-InAlAs-InP pHEMT (sample-1841) and InGaAs-AlGaAs-GaAs pHEMT (sample-1891) were used in this work. These devices have a 1 µm gate length and a 200 µm (2x100 µm) gate width a [13].

The epitaxial layer structure of the device is shown in figure 3. Looking at the structure from bottom to top, a lattice-matched undoped InAlAs buffer layer of thickness

4500 Å, is grown on top of an InP semi insulating substrate. A highly strained, undoped InGaAs, channel is grown well below the critical thickness of this composition (140Å). The spacer is a lattice matched, undoped InAlAs layer of thickness 100Å used to spatially separate the heavily doped delta-region from the active channel. A supply layer is formed with thickness 150Å to supply electrons into the 2DEG, with Delta-doping sheet density of 3.6x1012cm-2.

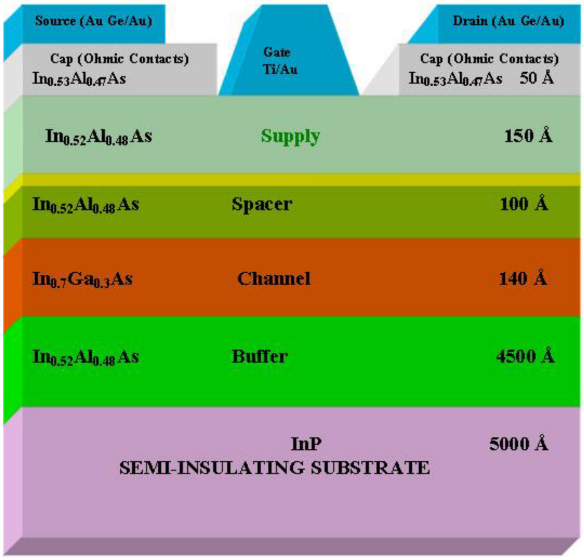


Figure 3 : The structure of the epitaxial layers of the pHEMT on an InP substrate. In the second device the semi insulating devices is made of GaAs.

5 NOISE FIGURE CHARACTERIZATION

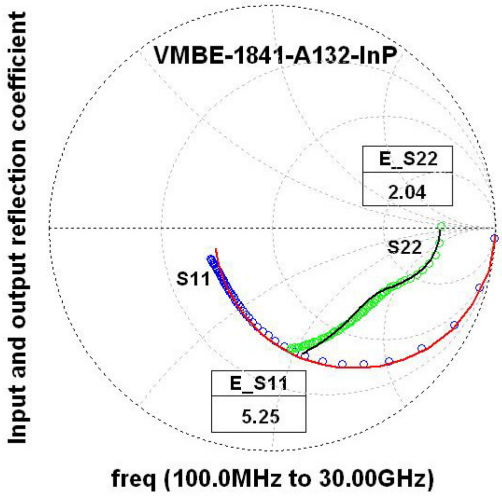
The main aim of the fabricated pHEMTs is the design and implementation of broadband low noise amplifiers for the square kilometre array (SKA) project. Thus it is important to get an accurate analytic expression for calculating the minimum noise figure of these devices. Since the noise figure of a FET is affected by both the bias point and the generator impedance, the minimum noise figure, NFmin defined here is an absolute minimum noise figure obtained by adjusting both the bias and the generator impedance. Using the four equivalent element values of Gm, Cgs/Fc , Rs, and Rg, determined by S-parameter measurements and small-signal parameter extraction. Fukui empirically derived a simple expression for NFmin [14], thus:

$$F_{\min}(dB) = 10Log(1 + 2\pi k_f fC_{gs}\sqrt{\frac{(R_s + R_g)}{G_m}}) \quad (17)$$

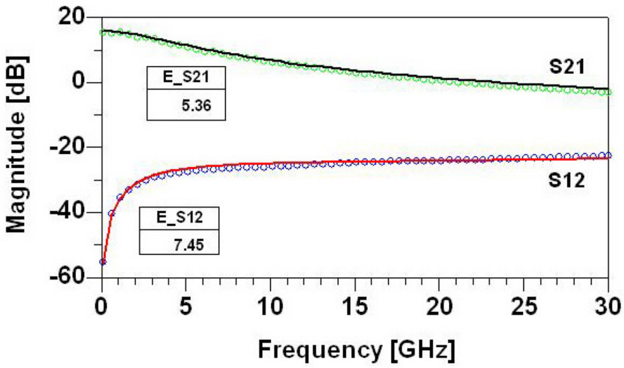
k_f is a fitting factor which depends on the material properties and f is the frequency. Applying this empirical form to our devices, and comparing with experimentally measured NFmin, the best-extracted values for the fitting factor k_f is 2.8 for the sample on a GaAs substrate and 3.4-3.6 for the sample on an InP substrate.

6 RESULTS AND DISCUSSION

The direct method presented in this work was demonstrated through the extraction of the small-signal equivalent circuit of two pHEMTs. Practically, the values of the extrinsic components were optimized to best fit with measurements (Figure 4). Table 1 shows the extrinsic and intrinsic element values of the small-signal equivalent circuit of the two following pHEMTs: the VMBE-1841-A132-InP (biased at V_{ds} = 1.5V and V_{gs} = -0.2V) and the VMBE-1891-A322-GAs (biased at V_{ds} = 0.5V and V_{gs} = - 0.4V). The curves displayed in figure 4 showed a good agreement between obtained and measured S-parameters. It should be noted that the stability factor k as well as the maximum available gain G_{max} (with k≥1) or the most stable gain MSG (if k<1) are critical parameters for microwave circuits designers. By comparing the GaAs-pHEMT and the InP-pHEMT, it is noted that the InP-pHEMT exhibits a lower minimum noise factor (NF_{min}) (figure 5, 6) , a higher gain G_{max} and a higher cut-off frequency F_c (Table 3): For InP-pHEMT: S_{21} = 14 dB, G_{max} = 22 dB, NF_{min} = 0.14 dB and F_c = 28 GHz; while for GaAs-pHEMT: S_{21} = 2 dB, G_{max} = 13 dB, NF_{min} = 0.198 dB and F_c = 8.6 GHz.



(a)



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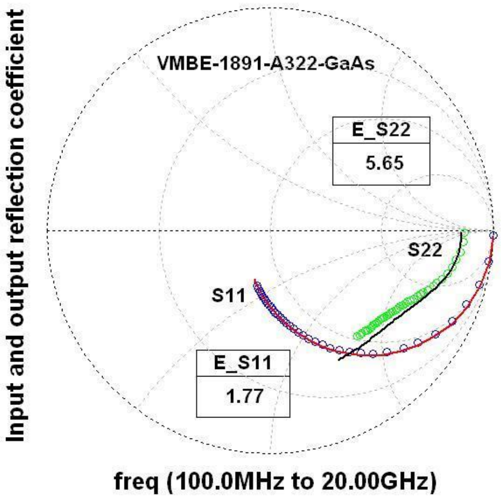

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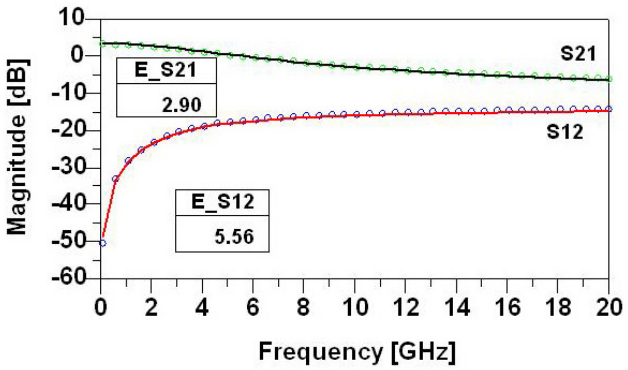


(d)

Figure 4 : Comparison between measured (circles) and calculated (lines) S parameters of pHEMT devices: (a), (b) VMBE-1841-A132-InP under the bias conditions: V_{ds} = 1.5V, V_{gs} =-0.2V, (c), (d) VMBE-1891-A322-GaAs under the bias conditions: V_{ds} = 0.5V, V_{gs}=-0.4V

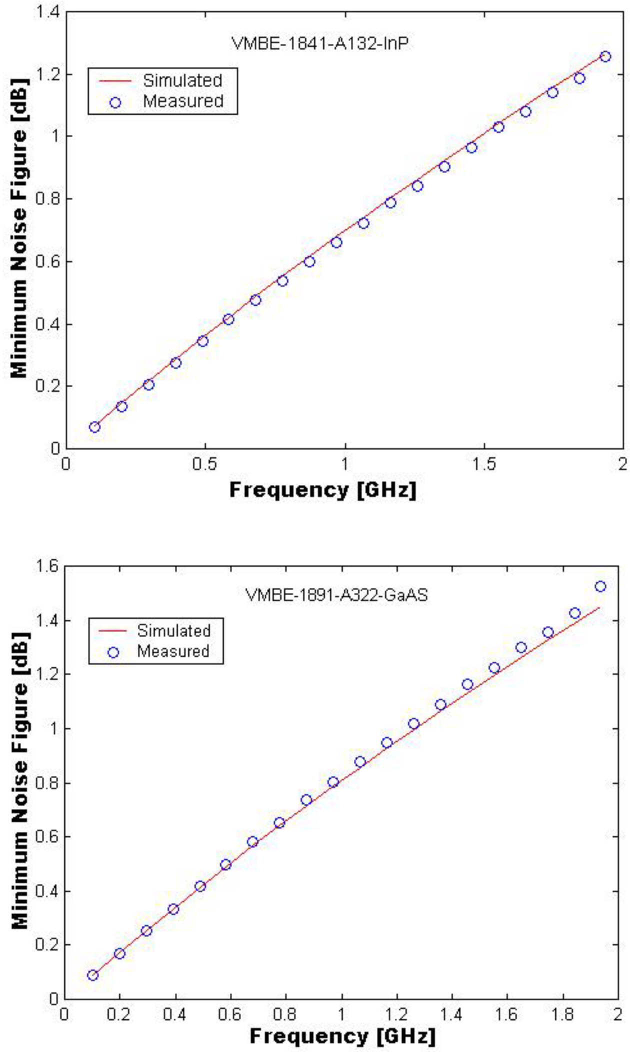
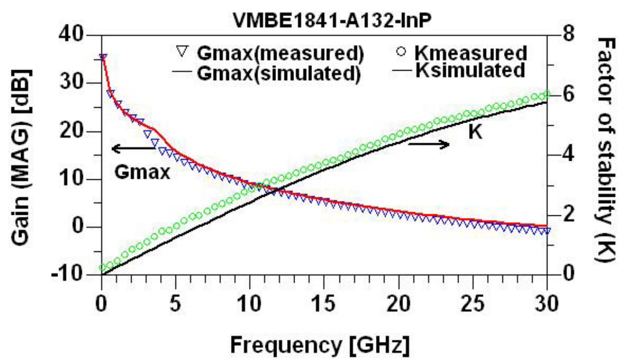


Figure 5 : Comparison of the measured minimum noise figure (room-temperature minimum noise figure of a 1x200 µm device from each sample up to 2 GHz) (circles) with minimum noise Figure calculations based on Fukui's analysis (lines).

Table 1 : Extracted parameter values for the two transistors

Device elements	VMBE-1841-A132-InP	VMBE-1891-A322-GaAs	Device elements	VMBE-1841-A132-InP	VMBE-1891-A322-GaAs
R_g (Ω)	20.65	23	R_i(Ω)	6.36	15.9
R_s(Ω)	2.6	5.77	C_{gs}(fF)	506	291
R_d(Ω)	3	8.16	C_{gd}(fF	25.2	60
L_g (pH)	15.3	21.8	R_{ds}(Ω)	285	585
L_s(pH)	12.1	8.34	C_{ds}(fF)	24.8	11.5
L_d(pH)	24	21	G_m(ms)	89	18
C_{pg} (fF)	2.2	1.47	τ (ps)	1.86	2.84
C_{pd}(fF)	30	34	C_{gs}(fF)	506	291



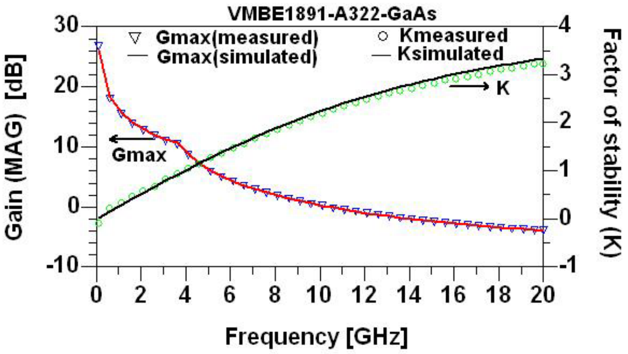


Figure 6 : Maximum Gain G_{max}, stability factor K for the: (a) VMBE-1841-A132-InP under the bias conditions: V_{ds} = 1.5V, V_{gs}= -0.2V, (b) VMBE-1891-A322-GaAs under the bias conditions: V_{ds} = 0.5V, V_{gs} =-0.4V.

Table 2 : Errors between measured and modelled values of S-parameters.

Device	S_{11} (% error)	S_{12} (% error)	S_{21} (%error)	S_{22} (%error)
VMBE-1841-InP	5.27	7.37	5.41	2.06
VMBE-1891-GaAs	1.78	5.55	2.88	5.61

Table 3 : Transistor performance parameters

Parameters	VMBE-1841		VMBE-1891	
	1 GHz	2 GHz	1 GHz	2 GHz
$NF_{min\ measured}$ (dB)	0.661	1.255	0.805	1.526
$NF_{min\ simulated}$ (dB)	0.680	1.265	0.786	1.449
$k_{measured}$	0.432	0.804	0.292	0.546
$k_{simulated}$	0.252	0.504	0.259	0.516
$G_{max\ measured}$ (dB)	25.785	22.926	15.859	12.938
$G_{max\ simulated}$ (dB)	25.963	22.952	16.413	13.147
$S_{21\ measured}$ (dB)	15.371	14.224	2.900	2.410
$S_{21\ simulated}$ (dB)	15.602	14.829	3.248	2.458

7 CONCLUSION

This work presents a direct extraction method of the elements of small signal equivalent circuit of two transistors PHEMT one on the GaAs substrate and the other on the InP substrate of which the length and the width of the gate respectively 1µm and 200 µm. This modelling is essential for any active or passive component and which precedes any design of a radio frequency circuit.

The technique suggested is of experimental type, rests to measures of the parameters of dispersion S, followed by a method of optimization; with an aim of studying the linear behavior and the performances ultra high frequencies of the transistor.

The results obtained show a good agreement between simulated and measured S-parameters. The analysis of the performances ultra high frequencies such as the gain, the factor of noise NFmin and the frequency band justifies the choice of transistor PHEMT on the InP substrate for the application low noise.

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