



ELSEVIER

Contents lists available at ScienceDirect

Superlattices and Microstructures

journal homepage: www.elsevier.com/locate/superlattices

Deep traps and temperature effects on the capacitance of p-type Si-doped GaAs Schottky diodes on (2 1 1) and (3 1 1) oriented GaAs substrates

R. Boumaraf^a, N. Sengouga^{a,*}, R.H. Mari^b, Af. Meftah^a, M. Aziz^c, Dler Jameel^c, Noor Al Saqri^c, D. Taylor^c, M. Henini^c

^a Laboratory of Metallic and Semiconducting Materials, Université de Biskra, B.P. 145 RP, 07000 Biskra, Algeria

^b Institute of Physics, University of Sindh, Jamshoro, Pakistan

^c School of Physics and Astronomy, Nottingham Nanotechnology and Nanoscience Center, University of Nottingham, Nottingham NG7 2RD, UK

ARTICLE INFO

Article history:

Received 15 November 2013

Accepted 16 November 2013

Available online 23 November 2013

Keywords:

High index GaAs

Capacitance–temperature

Deep levels

SILVACO simulation

ABSTRACT

The SILVACO-TCAD numerical simulator is used to explain the effect of different types of deep levels on the temperature dependence of the capacitance of p-type Si-doped GaAs Schottky diodes grown on high index GaAs substrates, namely (3 1 1)A and (2 1 1)A oriented GaAs substrates. For the (3 1 1)A diodes, the measured capacitance–temperature characteristics at different reverse biases show a large peak while the (2 1 1)A devices display a much smaller one. This peak is related to the presence of different types of deep levels in the two structures. These deep levels are characterized by the Deep Level Transient Spectroscopy (DLTS) technique. In the (3 1 1)A structure only majority deep levels (hole deep levels) were observed while both majority and minority deep levels were present in the (2 1 1)A diodes. The simulation software, which calculates the capacitance–voltage and the capacitance–temperature characteristics in the absence and presence of different types of deep levels, agrees well with the experimentally observed behavior of the capacitance–temperature properties. A further evidence to confirm that deep levels are responsible for the observed phenomenon is provided by a simulation of the capacitance–temperature characteristics as a function of the ac-signal frequency.

© 2013 Elsevier Ltd. All rights reserved.

* Corresponding author.

E-mail address: n.sengouga@univ-biskra.dz (N. Sengouga).

1. Introduction

Silicon (Si) and Beryllium (Be) are the main doping elements in Gallium Arsenide (GaAs) and other III–V based semiconductor devices. While Be is a p-type dopant, Si can be either an n-type or p-type depending on the growth conditions. Despite many efforts hole mobilities in Be-doped structures grown on conventional (100) GaAs substrate remained considerably lower than those obtained by growing on (311)A oriented surface, so called high index substrate, using silicon as p-type dopant [1]. It is important to add that the silicon (a group IVA element) impurity in GaAs grown by Molecular Beam Epitaxy (MBE) can act as either a donor (occupies a Ga site: group V) or acceptor (occupies a As site: group III) [2,3]. This amphoteric dopant is dependent on the substrate orientation [4–6]. Silicon is mainly a donor when the growth is on the (100) surface. However, silicon incorporates preferentially as a donor in (N11)B and as an acceptor on (N11)A surfaces ($N = 1, 2, 3$). A and B denote a Ga- and As-terminated plane, respectively. In addition, in (111)A, (211)A, and (311)A planes, silicon may act as a donor or as an acceptor depending on the substrate temperature and the arsenic overpressure used during the MBE growth. This amphoteric nature of silicon could lead to the development of novel devices. In fact the amphoteric nature of Si facilitates the MBE growth of p-type GaAs/AlGaAs heterostructures on (311)A that have higher hole mobilities than those based on the conventional Be-doped p-type on (100) GaAs plane [7–11]. Thus, the interest in the growth of III–V compound semiconductors such as GaAs, InAs, InGaAs, GaAsSb and AlGaAs on high index planes, other than the conventional (100) orientation, has increased tremendously and attracted a great deal of attention over the last several years. The structural, optical and electrical properties of III–V based structures are found to improve by growing on (N11) planes. The growth of semiconductor layers and structures strongly depends on the substrate orientation and hence to surface atomic arrangement [12,13]. This may lead to some defects which could have deleterious effects on the electrical and optical properties of III–V based devices [14].

A wide variety of structures can be grown on high index planes. For example quantum wire structures [15], quantum dots [16,17], quantum strings [18], InAs three-dimensional islands [19]. InGaAs strained growth on GaAs surfaces results in zero-dimensional quantum dots and the formation of one-dimensional quantum wires is demonstrated during InGaAs MBE growth on GaAs (311)A at high temperature [20]. InGaAs/GaAs quantum wells grown by MBE on GaAs (100), (210), (311), and (731) substrates were investigated for possible application in superluminescent diodes [21,22].

Although the Deep level Transient Spectroscopy (DLTS) [23] and capacitance–voltage (C–V) profiling [24] are quite old techniques, they are still extensively used in the characterization of semiconductor devices [25]. The combination of these two techniques is to relate the departure of the shape C–V curves from ideality to the presence of defects in the different regions of the semiconductor device (bulk, surface or interface) [26]. An example of this is the so called negative differential capacitance (NDC) effect [27–29]. NDC behavior is sometimes related to nonuniform distribution of defects [30]. In other structures it is related to quantum states [31]. The temperature and frequency dependence of the C–V characteristics are some of the effects usually related to deep levels [32–35].

In this work two Si-doped p-type GaAs samples were grown by MBE on (211)A and (311)A oriented GaAs semi-insulating substrates, named hereafter NU928 and NU926, respectively. They are investigated using C–V measurements at different temperatures and DLTS technique. In order to relate the capacitance–temperature relationship to the observed deep levels, the ATLAS module of the commercial software (SILVACO-TCAD) is used to calculate these characteristics of the two samples [36]. The experimental and simulation data are then compared.

2. Experimental details

p-Type Si-doped GaAs samples are grown on (N11)A ($N = 2, 3$) planes to investigate the electrical properties and the defects present in epitaxial layers grown on different Miller indices. They were characterized by C–V and DLTS techniques.

2.1. Samples

To ensure similar growth conditions, the samples investigated in this work were grown simultaneously in a Varian Gen-II MBE machine. The growth temperature was 580 °C and the As:Ga beam equivalent flux ratio determined by an ionization gauge was 12:1 (As overpressure was 1×10^{-5} Torr). The growth rate was one monolayer per second ($\sim 1 \mu\text{m/h}$) as measured by the Reflection High Energy Electron Diffraction (RHEED) technique. The samples were rotated during the growth to enhance uniformity.

Sample NU926 is grown on semi-insulating (311)A GaAs substrate. It consists of a 0.1 μm un-doped GaAs buffer layer followed by a 0.5 μm Si-doped p-type GaAs layer. The silicon cell was set to a temperature which normally gives a doping level of $(N_D - N_A) = 1 \times 10^{17} \text{ cm}^{-3}$ for the (100) samples. The carrier concentration of the (211)A and (311)A samples of $N_A - N_D = 0.8 \times 10^{17} \text{ cm}^{-3}$ was obtained at room temperature using the Hall Effect and electrochemical capacitance–voltage measurements. N_A refers to the acceptor concentration and N_D to the donor concentration. Although these measurements indicate that the auto-compensation is similar in both substrate orientations, our previous detailed assessment of the low-temperature photoluminescence spectra of p-type Si-doped (311)A and (111)A samples with a carrier concentration of $\sim 2 \times 10^{16} \text{ cm}^{-3}$ suggested that the (311)A samples are more compensated than the (111)A samples [37]. The structure was processed into mesa where the Schottky contacts were made by evaporating Ti/Au on the top of the doped GaAs layer. The top layer was etched up for the deposition of Ohmic contacts [Au/Ni/Au]. Sample NU928 has the same structure except that it is grown on (211)A GaAs substrate.

Fig. 1 shows the average effective density evaluated from the C–V characteristics of the (211)A and (311)A samples at different temperatures. At 300 K, the average effective density is $\sim 6.0 \times 10^{16} \text{ cm}^{-3}$ and $\sim 2.2 \times 10^{16} \text{ cm}^{-3}$ for the (211)A and (311)A samples, respectively. The effective density is a bit different from that of Hall measurements especially for the (311)A sample. This may be due to the non-uniformity of the effective density and defects profile in these samples.

2.2. Capacitance–voltage measurements

The analysis of the C–V characteristics provides important parameters such as the built-in voltage, the background doping concentration and concentration depth profile. The DLTS data analysis relies on these parameters. Therefore, C–V characteristics of each device are measured using a BOONTON 7200 Capacitance Meter, which is controlled by a computer. It operates at a frequency of 1 MHz.

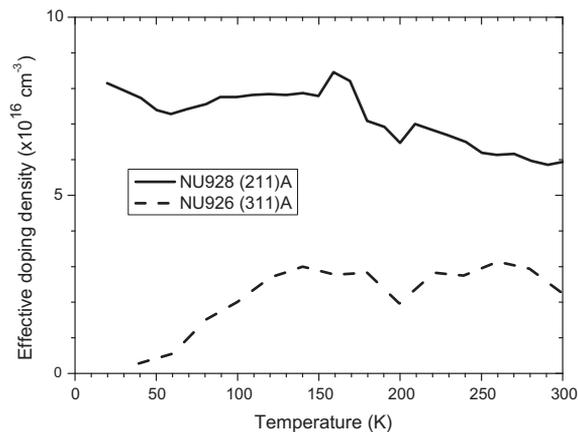


Fig. 1. The average effective density evaluated from the C–V characteristics of the (211)A and (311)A samples at different temperatures.

2.3. DLTS and Laplace DLTS measurements

DLTS and Laplace DLTS are used as the main tool for the characterization of deep levels present in the material systems. The samples packaged in a TO5 header were mounted on a sample holder. The samples were first cooled down to a temperature of 10 K in a Closed Cycle Cryodyne Refrigerator, Model number CCS-450. DLTS measurements were then started by ramping the temperature at a rate of 2 K/min. A train of electrical pulses, generated by a pulse generator (model Agilent 33,220 A) was applied to the sample. The filling pulse repetition rate is fixed to 50 Hz. The reverse bias (VR) and filling pulse (VP) is applied in such a way that $VP < VR$.

For the resolution of the broad featureless DLTS peaks, High Resolution Laplace DLTS measurements were carried out. Laplace DLTS is an isothermal DLTS process; therefore, the measurements are performed at constant temperature within a temperature range where the conventional DLTS peak appears. Further details of the measurements can be found in [38].

3. The simulation software SILVACO-TCAD

In order to characterize semiconductor devices and relate the observed effects to each other, extensive experimental work has to be carried out. In some cases, analytical or qualitative modelling has to be used to relate these experimentally observed effects. The experimental characterization turns out to be time consuming and can be very expensive. The analytical modelling has to accept several simplifications. Numerical simulation is an alternative and a powerful tool. Many parameters can be varied to model the observed phenomenon. In this present study the variables are the defects and the phenomenon is the capacitance dependence on voltage and temperature. Numerical simulation can also offer a physical explanation of the observed phenomenon since internal parameters can be calculated such as the electrical field and the free carrier densities.

The electrical characteristic of the device are calculated using ATLAS of SILVACO. It is a physically-based two and three dimensional device simulator. It predicts the electrical behavior of specified semiconductor structures and provides insight into the internal physical mechanisms associated with device operation. The simulator is based on a mathematical model valid for any semiconductor device. This model consists of a set of fundamental equations, which link together the electrostatic potential and the carrier densities, within some simulation domain. These equations, which are solved inside any general purpose device simulator, have been derived from Maxwell's laws and consist of Poisson's equation, the carrier continuity equations and the transport equations.

The current density equations, or charge transport models, are usually obtained by applying approximations and simplifications to the Boltzmann Transport Equation. These assumptions can result in a number of different transport models. The simplest model of charge transport that is useful is the drift–diffusion model. This model is adequate for nearly all devices that were technologically feasible. This model is based on the two first equations cited above. The Poisson's equation which relates the electrostatic potential to the space charge density:

$$\text{div}(\varepsilon \nabla \psi) = -\rho \quad (1)$$

where ψ is the electrostatic potential, ε is the local permittivity, and ρ is the local space charge density.

And the continuity equations for electrons and holes, given respectively by:

$$\frac{\partial n}{\partial t} = \frac{1}{q} \text{div} \vec{J}_n + G_n - R_n \quad (2.a)$$

$$\frac{\partial p}{\partial t} = \frac{1}{q} \text{div} \vec{J}_p + G_p - R_p \quad (2.b)$$

where n and p are the electron and hole concentration, \vec{J}_n and \vec{J}_p are the electron and hole current densities, G_n and G_p are the generation rates for electrons and holes, R_n and R_p are the recombination rates for electrons and holes, and q is the electron charge.

In steady state these equations becomes:

$$0 = \frac{1}{q} \text{div} \vec{J}_n + G_n - R_n \tag{3.a}$$

$$0 = -\frac{1}{q} \text{div} \vec{J}_p + G_p - R_p \tag{3.b}$$

By default ATLAS includes both Eqs. (2.a) and (2.b). In some circumstances, however, it is sufficient to solve only one carrier continuity equation.

In the drift–diffusion model, the current densities are expressed in terms of the quasi-Fermi levels ϕ_n and ϕ_p as:

$$\vec{J}_n = -q\mu_n n \nabla \phi_n \tag{4.a}$$

$$\vec{J}_p = -q\mu_p p \nabla \phi_p \tag{4.b}$$

where μ_n and μ_p are the electron and hole mobilities. The quasi-Fermi levels are then linked to the carrier concentrations and the potential through the two Boltzmann approximations:

$$n = n_i \exp\left(\frac{\psi - \phi_n}{k_B T}\right) \tag{5.a}$$

$$p = n_i \exp\left(-\frac{\psi - \phi_p}{k_B T}\right) \tag{5.b}$$

where n_i is the effective intrinsic concentration and T is the lattice temperature. These two equations may then be re-written to define the quasi-Fermi potentials:

$$\phi_n = \psi - \frac{k_B T}{q} \ln \frac{n}{n_i} \tag{6.a}$$

$$\phi_p = \psi + \frac{k_B T}{q} \ln \frac{p}{n_i} \tag{6.b}$$

By substituting these equations into the current density expressions, the following current relationships are obtained:

$$\vec{J}_n = qD_n \nabla n - q\mu_n n \nabla \psi - \mu_n n k_b T \nabla \ln(n_i) \tag{7.a}$$

$$\vec{J}_p = -qD_p \nabla p - q\mu_p p \nabla \psi + \mu_p p k_b T \nabla \ln(n_i) \tag{7.b}$$

assumed that the Einstein relationship holds:

$$D_n = \frac{k_B T}{q} \mu_n$$

$$D_p = \frac{k_B T}{q} \mu_p$$

The final term accounts for the gradient in the effective intrinsic carrier concentration, which takes account of bandgap narrowing effects.

The conventional formulation of drift–diffusion equations is:

$$\vec{J}_n = qD_n \nabla n + q\mu_n n \vec{E}_n \tag{8.a}$$

$$\vec{J}_p = -qD_p \nabla p + q\mu_p p \vec{E}_n \tag{8.b}$$

where:

$$\vec{E}_n = -\nabla\psi - \frac{k_B T}{q} \nabla \ln(n_i) \quad (9.a)$$

$$\vec{E}_p = -\nabla\psi + \frac{k_B T}{q} \nabla \ln(n_i) \quad (9.b)$$

The electrical characteristics are calculated following the specified physical structure and bias conditions. This is achieved by approximating the operation of the device onto a two dimensional grid, consisting of a number of grid points called nodes. By applying the set of differential equations (Poisson's and continuity equations) onto this grid (or equation's discretisation), the transport of carriers through the structure can be simulated. The finite element grid is used to represent the simulation domain.

Of interest to the present work, the capacitance–voltage characteristics are calculated under different conditions (presence or absence of deep levels) at various temperatures or the capacitance–temperature characteristics at different voltages. Once the DC solution is obtained, it can be developed into an AC solution (sinusoidal steady state analysis). The frequency–domain perturbation analysis of a DC solution can be used to calculate small-signal characteristics at any specified frequency [39]. The calculation proceeds in the following manner:

- Variables are represented as the sum of the known DC component and a small unknown sinusoidal AC component. Therefore we write:

$$F(X_s + dX_s \cdot \exp[j\omega t]) = DC \cdot \exp[j\omega t] \quad (10)$$

$F = \psi, n$ or p

- All equations are expanded.
- Differentiation in time becomes multiplication by the value of ω ($\omega = 2\pi f$).
- Products of AC quantities are neglected since they are small with respect to other quantities.
- The DC solution is subtracted.
- Small unknown sinusoidal AC component means that the DC solution is not perturbed and everything is linear.
- What remains is a complex system whose unknowns are the AC components of the solution, now we can solve the AC part directly from the DC solution. The results are complex, the real parts are converted into G values and the complex parts are converted into capacitances.

4. Results and discussions

4.1. Measurements

First the capacitance–voltage characteristics are measured at different temperatures ranging from 10 to 300 K for the two samples. A typical example is shown in Fig. 2. The characteristics are presented using similar scales for the sake of comparison.

The first observation is that the NU926 sample characteristics have a more complicated shape and are more affected by the temperature. It is evident that for this sample the C–V curve departs from the conventional shape characterized by the proportionality $C \propto 1/\sqrt{(V_B + |V_R|)}$ where V_B and V_R are the Schottky barrier and the reverse voltages, respectively. In fact it shows a NDC behavior especially at higher temperatures. This departure can be explained by the presence of different types of deep levels in the two structures when DLTS measurements are presented. It is also worth to note the scale difference in the capacitance of the two samples as shown by the insert in (b).

The second observation is that the capacitance initially increases with increasing temperature then starts to drop at temperatures of 120 and 170 °K for NU926 and NU928, respectively. This behavior is more pronounced for the first sample and is better illustrated by plotting the capacitance–temperature characteristics at a fixed voltage. This will be presented later since it will be compared to simulation.

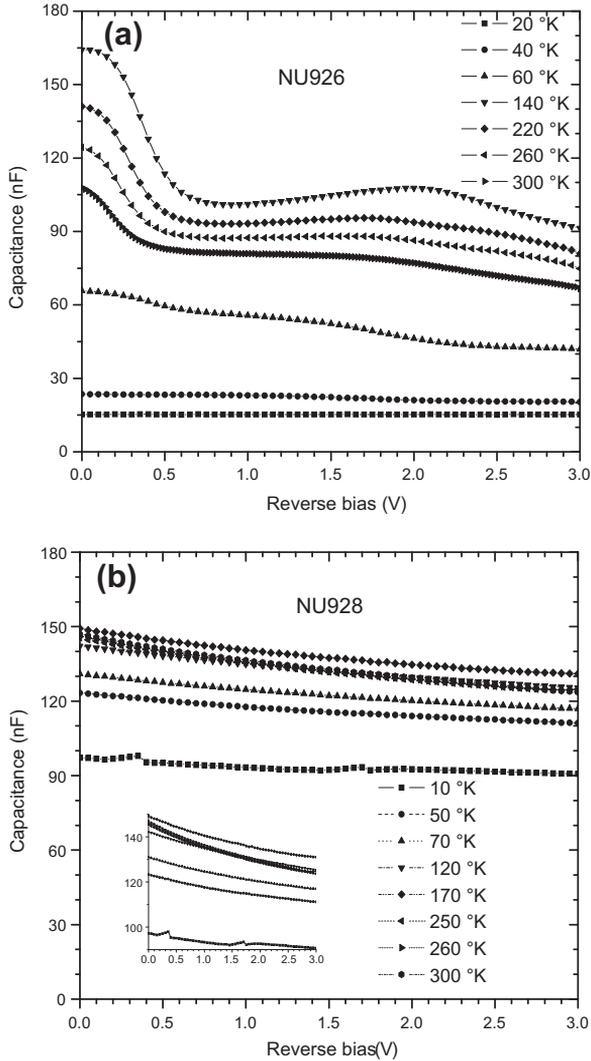


Fig. 2. The capacitance–voltage characteristics at different temperatures for the samples (311)A (NU926) (a) and (211)A (NU928) (b).

To explain this behavior, DLTS measurements are performed to reveal the deep levels present in the two samples. Typical DLTS spectrums are presented in Fig. 3. The filling pulse has a height of 0.8 V, a reverse bias of -0.5 V and a filling time of 1 ms. The rate window varies from 2.5 to 200 Hz by a factor of 2. It is worth mentioning that negative peaks are due to majority deep levels (hole deep levels in this case) while positive peaks represent minority deep levels (electron deep levels). The samples are p-type. For sample NU926, only majority (hole) deep levels are found while both hole and electron deep levels are detected in NU928. It has also to be mentioned that there is a difference in the scales of DLTS signals for the two samples. The electron deep levels in NU928 give a DLTS signal about 40 times larger than hole deep levels. This is clarified by the insert in Fig. 3(b) where the positive DLTS signal (signature of electron deep levels) is divided by a factor of 20 so that the negative signal (hole deep levels) can be clearly seen. This means that the electron deep levels have a much higher density than

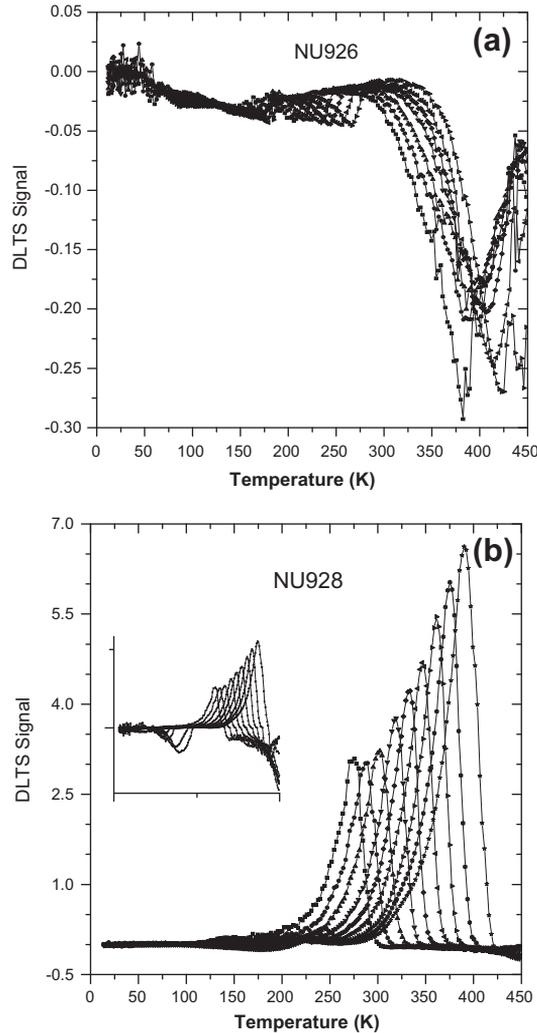


Fig. 3. DLTS spectra for (311)A (NU926) (a) and (211)A (NU928) (b) samples. In the insert in (b), the positive signal (electron deep levels) is divided by 20.

hole deep levels. These are the main reasons (different types of deep levels and different densities) of the observed difference in the capacitance–temperature dependence for the two samples.

For the first sample, the parameters of deep acceptors are given in Table 1. For the second sample, the parameters of deep acceptors and donors are given in Table 2. In both tables the activation energy is above the valence band and below the conduction band for the deep acceptors (H) and deep donors (E) respectively. The deep acceptor parameters are measured by Laplace DLTS whereas the electron trap parameters are extracted from the conventional DLTS spectrum.

In this preliminary investigation it is difficult to ascertain the origin of the observed defects, which could be due to complexes involving silicon atoms, background impurities, and defects related to the growth conditions. It is also worth pointing out that the samples studied in this work are p-type Si-doped (211)A and (311)A GaAs substrates. Silicon always behaves as n-type dopant in (100) GaAs. It would be difficult to compare our p-type Si-doped samples grown on high index GaAs with p-type

Table 1

The defect parameters determined by Laplace DLTS for (311)A sample (NU926).

Deep level	Activation energy (eV)	Density (cm ⁻³)	Capture cross section (cm ²)
H1	0.025 ± 0.003	1.43 × 10 ¹⁵	1.63 × 10 ⁻¹⁸
H2	0.014 ± 0.002	1.47 × 10 ¹⁵	4.79 × 10 ⁻¹⁷
H3	0.247 ± 0.005	1.19 × 10 ¹⁵	7.35 × 10 ⁻¹⁸
H4	0.837 ± 0.007	1.54 × 10 ¹⁵	6.75 × 10 ⁻¹⁸

Table 2

The defect parameters determined by Laplace DLTS for the sample (211)A (NU928).

Deep level	Activation energy (eV)	Density (cm ⁻³)	Capture cross section (cm ²)
H1	0.061 ± 0.014	5.65 × 10 ¹⁵	5.35 × 10 ⁻¹⁶
H2	0.075 ± 0.011	6.64 × 10 ¹⁵	4.36 × 10 ⁻¹⁶
H3	0.153 ± 0.03	2.81 × 10 ¹⁵	4.36 × 10 ⁻¹⁶
H4	0.170 ± 0.02	3.39 × 10 ¹⁵	4.77 × 10 ⁻¹⁶
H5	0.283 ± 0.001	7.83 × 10 ¹⁴	3.99 × 10 ⁻¹⁶
E	0.431 ± 0.019	1.68 × 10 ¹⁶	3.33 × 10 ⁻¹⁷

Be-doped samples grown on the conventional (100) GaAs. In addition, it has to be mentioned that not much work is carried out on deep levels in p-type GaAs grown on conventional (100) GaAs.

We plan to study different samples grown under different conditions in order to shed some light on the nature of the defects. In our previous studies on p-type Si-doped (311)A and (111)A samples with a carrier concentration of ~2 × 10¹⁶ cm⁻³, detailed assessment of the low-temperature photoluminescence spectra suggested that the (311)A samples are more compensated than the (111)A samples [37]. It is expected that also (311)A will be more compensated than the (211)A samples. Further detailed studies are required to confirm this. In addition, it has to be mentioned that this work concerns only the effect of the deep levels on the C–V–T characteristics and not the deep levels themselves. This requires separate and thorough work since not much work on deep levels in p-type Si-doped GaAs is known so that comparison can be made.

The relation between the capacitance–temperature characteristics and the presence of defects is first explained qualitatively by considering the evolution of p-type doping and deep levels with temperature. These effects are then quantified using numerical simulation by SILVACO TCAD.

Let us first consider the capacitance of a p-type Schottky diode. In the absence of defects, it is given by the well-known formula [40]:

$$C = \sqrt{\frac{q \cdot \epsilon_s \cdot N_A^-}{2(V_B - V - \frac{K.T}{q})}} \tag{11}$$

N_A^- is the ionized acceptor doping density. The other symbols have the usual meaning [40]. It is expected thus that the capacitance increases with increasing temperature since the most affected parameter in Eq. (11), is the doping density of which the ionization increases exponentially with increasing temperature. However, the experimental results show a different behavior as can be seen in Fig. 4 (below). The capacitance increases and then start to decrease as the temperature increases.

In presence of defects, the capacitance formula should be modified to take into account these changes. Thus,

$$C = \sqrt{\frac{q \cdot \epsilon_s \cdot (N_A^- \mp \sum N_{Ti}^\mp)}{2(V_B - V - \frac{K.T}{q})}} \tag{12}$$

Here N_{Ti}^\mp is the ionized *i*th deep level (the sign indicates whether it is a donor or acceptor).

If the deep level is an acceptor, like in the case of NU926, the Fermi level is initially (at low temperatures) located somewhere between the shallow acceptor and the deep acceptor so that even

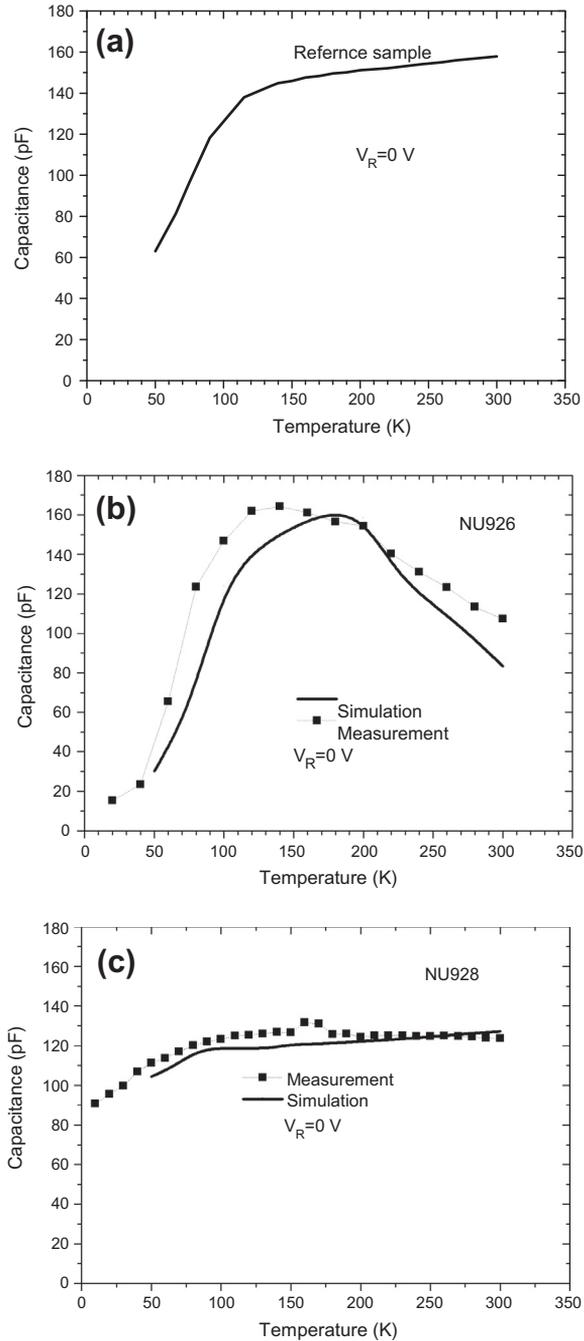


Fig. 4. The simulated capacitance–temperature characteristics for three samples: in the absence of deep levels [(a), reference sample], in the presence of deep acceptors [(b) (3 1 1)A sample (NU926)] and in the presence of deep acceptors and donors [(c), (2 1 1)A sample (NU928)].

the shallow levels are not ionized. Therefore the capacitance is almost independent of voltage (Fig. 2(a)) because there is no depletion region. As the temperature increases the Fermi level moves down and the shallow level ionizes faster than the deep one giving an increase in the capacitance until the ionization of the first is complete. This is the point where the capacitance reaches its maximum. From this point the deep acceptor continues to ionize and the Fermi level moves upwards leading to a decrease in the ionization of the shallow level and an increase in deep level ionization. But the first is faster than the second. Hence a decrease in the capacitance is observed. This explanation will be strengthened when the simulation results are presented.

On the other hand if the deep level is a donor, which is the case of NU928, the situation is that the shallow and deep levels compensate each other. Therefore, the capacitance does not change with voltage or temperature as much as for the previous case. This will also be demonstrated by the simulation results.

4.2. Simulation

In order to relate the observed dependence of the capacitance on temperature to the defects present in the samples, a simulation of three structures using SILVACO-TCAD is carried out. The three structures are similar; they differ only in the defects introduced. The parameters, other than the defects, are those described in Section 2.1. The first structure is ideal, i.e. no defects are present, which will be the reference sample. The second is when only deep acceptors are present (the case of NU926). The third is when both deep donors and acceptors are present in the structure (the case of NU928).

In carrying out numerical simulation, it has to be mentioned that there are so many different parameters to adjust to fit the measurements (several defects, each of them is characterized by three parameters: energy, capture cross section and density, in addition to other parameters of the material such as mobility, lifetime, and doping density). Therefore numerical simulation is usually more difficult than analytical modelling because of the reason mentioned above. In the latter, much fewer parameters have to be adjusted and in most cases they do not have a physical meaning. In this work the parameters of deep levels are fixed (Tables 1 and 2) and the doping density is adjusted so that simulation is as close as possible to measurements. A value of $\sim 1 \times 10^{16} \text{ cm}^{-3}$ gives an acceptable comparison. This value is lower than the real doping density. This may be due to the presence of other shallow levels in both structures and hence may contribute to the effective doping density in the simulation. This is perhaps a first indication that the shallow levels, detected by Laplace DLTS, may be related to the doping element (Si). The simulated dependence of the capacitance on temperature, compared to measurements, at a reverse bias of 0 V is shown in Fig. 4 (a), (b) and (c) for the reference, (311)A and (211)A samples, respectively.

When no defects are present (reference sample) the capacitance increases monotonically as expected and predicted by Eq. (11). The increasing rate is faster at low temperatures where the shallow doping level is still ionizing. At high temperatures, the increase slows down since most of the shallow level is fully ionized.

When only deep acceptors are present the capacitance initially increases with increasing temperature. This is because the shallow level ionizes faster than the deep acceptors and hence the Fermi level moves down. At a certain temperature the deep acceptors ionization becomes so important that the Fermi level moves up and the ionized shallow level is reduced. The overall effective density of charges is reduced and the capacitance decreases. This is the point where the capacitance reaches its maximum. From this point the deep acceptor continues to ionize and the Fermi level moves upwards leading to a decrease in the ionization of the shallow level and an increase in deep level ionization. This is the case of NU926 [(311)A sample] where only hole deep levels (deep acceptors) are present.

For the third sample both deep donor and acceptors are present. It is worth mentioning that the deep donor has a much higher density than deep acceptors. The shallow and deep acceptors are therefore compensated by the deep donors. Hence the effective doping density is reduced. The increase in temperature ionizes almost equally the deep donor and acceptors. Hence the effective doping density does not change much with temperature. Therefore the capacitance also does not change much with

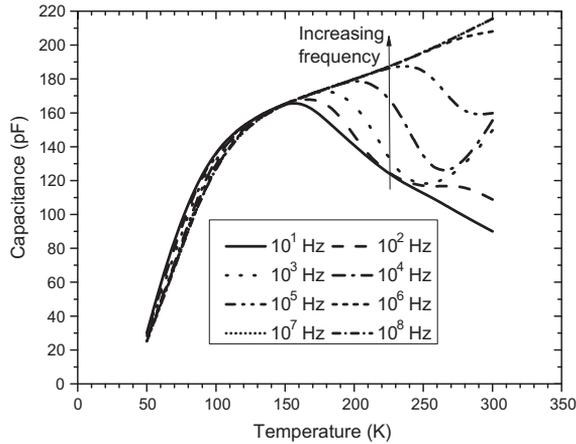


Fig. 5. The simulated capacitance–temperature characteristics for different frequencies in the presence of deep acceptors only (3 1 1)A sample (NU926).

temperature. This is similar to the effect observed in the case of (2 1 1)A sample (NU928). Therefore, the simulation results confirm the results observed experimentally.

The effect of frequency on the capacitance–temperature characteristics is also simulated. This is to enhance our explanation of the relation between the C – T characteristics and the presence of different type of deep levels. It is well known that the deep levels response depends on the frequency of the alternating signal used to measure the change in capacitance. This is because a deep level is characterized by an emission rate, i.e. a frequency. If the signal frequency is much higher than the deep level emission rate, the deep level cannot follow the signal variations. That is the deep level does not respond to the signal. An example of the frequency effect on the capacitance–temperature relation is shown in Fig. 5 for the case of sample NU926 (presence of deep acceptors only).

As demonstrated in Fig. 5 the capacitance–temperature relationship is sensitive to the frequency. When the frequency is low the capacitance–temperature dependence has a similar behavior as the solid line (without symbols) in Fig. 4(b). That is deep levels are able to follow the slow changing ac signal. As the frequency increases the capacitance–temperature dependence on frequency decreases. This is because the deep acceptor cannot follow the fast changing signal (high frequency). The high frequency curves tend to be similar to Fig. 4(a) (that is when no deep levels are present in the sample). This also confirms that the experimentally observed capacitance dependence on temperature is due to the presence of deep traps.

5. Conclusion

Two p-type GaAs Schottky diodes grown on (3 1 1)A and (2 1 1)A Si GaAs substrates were characterized by capacitance–voltage, capacitance–temperature and DLTS measurements. The capacitance–voltage characteristics of the (3 1 1)A sample were found to depart from the usual C – V dependence. DLTS revealed that in the (3 1 1)A sample only majority type defects are present, while in the (2 1 1)A sample both majority and minority related defects were detected. The departure of the C – V characteristics was related to the presence of deep acceptor defects. The capacitance–temperature was also found to depart from the expected defect free samples. A peak was found in these characteristics and this effect was more pronounced for the (3 1 1)A sample for which the C – V characteristics depart from the usual shape. The effect of temperature was also related to deep acceptors. Numerical simulation by the SILVACO-TCAD software was successfully used to reproduce the experimentally observed effects.

Acknowledgements

R. Boumaraf, N. Sengouga and Af. Meftah would like to thank the Faculty of Fundamental Sciences (University of Biskra) for its financial support for the scientific visit to the University of Nottingham.

References

- [1] R.H. Mari, M. Shafi, M. Aziz, A. Khatib, D. Taylor, M. Henini, *Nanoscale Res. Lett.* 6 (2011) 180.
- [2] R.H. Mari, M. Shafi, M. Henini, D. Taylor, *Phys. Status Solidi C* 6 (2009) 2873.
- [3] B. Pavesi, Ky Nguyen Hong, J.D. Ganière, F.K. Reinhart, N. Baba-Ali, I. Harrison, B. Tuck, M. Henini, *J. Appl. Phys.* 71 (2225) (1992).
- [4] W.I. Wang, E.E. Mendez, T.S. Kuan, L. Esaki, *Appl. Phys. Lett.* 47 (1985) 826.
- [5] B. Lee, S.S. Bose, M.H. Kim, A.D. Reed, G.E. Stillman, W.I. Wang, L. Vina, P.C. Colter, *J. Cryst. Growth* 96 (1989) 27.
- [6] I. Harrison, L. Pavesi, M. Henini, D. Johnston, *J. Appl. Phys.* 75 (1994) 3151.
- [7] A.G. Davies, R. Newbury, M. Pepper, J.E.F. Frost, D.A. Ritchie, G.A.C. Jones, *Phys. Rev. B* 44 (1991) 13128.
- [8] A.G. Davies, R. Newbury, M. Pepper, J.E.F. Frost, D.A. Ritchie, G.A.C. Jones, *Surf. Sci.* 263 (1992) 81.
- [9] M.B. Santos, J. Yo, Y.W. Suen, L.W. Engel, M. Shayegan, *Phys. Rev. B* 46 (1992) 13639.
- [10] J.J. Heremans, M.B. Santos, M. Shayegan, *Appl. Phys. Lett.* 61 (14) (1992) 1652.
- [11] M. Henini, P.J. Rodgers, P.A. Crump, B.L. Gallagher, G. Hill, *Appl. Phys. Lett.* 65 (16) (1994) 2054.
- [12] J. Ibáñez, R. Kudrawiec, J. Misiewicz, M. Schmidbauer, M. Henini, M. Hopkinson, *J. Appl. Phys.* 100 (093522) (2006).
- [13] Proceedings of the 5th International Workshop on Epitaxial Semiconductors on Patterned Substrates and Novel Index Surfaces (ESPS-NIS), *Physica E: Low-dimensional Systems and Nanostructures*, vol. 23, 2004, p. 3.
- [14] M. Shafi, R.H. Mari, A. Khatib, Taylor, M. Henini, *Nanoscale Res. Lett.* 5 (2010) 1948.
- [15] V.R. Yazdanpanah, Z.M. Wang, G.J. Salamo, *Appl. Phys. Lett.* 82 (2003) 1766.
- [16] G.E. Dialynas, S. Kalliakos, C. Xenogianni, M. Androulidaki, T. Kehagias, P. Komninou, P.G. Savvidis, Z. Hatzopoulos, N.T. Pelekanos, *J. Appl. Phys.* 108 (2010) 103525.
- [17] S. Sanguinetti, M. Gurioli, M. Henini, *Microelectron. J.* 33 (2002) 583.
- [18] M. Bennour, F. Saidi, L. Bouzaïene, L. Sfaxi, H. Maaref, *J. Appl. Phys.* 111 (2012) 024310.
- [19] Z.M. Wang, H. Wen, V.R. Yazdanpanah, J.L. Shultz, G.J. Salamo, *Appl. Phys. Lett.* 82 (2003) 1688.
- [20] H. Wen, Z.M. Wang, G.J. Salamo, *Appl. Phys. Lett.* 84 (2004) 1756.
- [21] Z. Li, J. Wu, Z.M.W.D. Fan, A. Guo, S. Li, S.Q. Yu, O. Manasreh, G.J. Salamo, *Nanoscale Res. Lett.* 5 (2010) 1079.
- [22] T. Kawazu, *Physica E* 44 (2012) 1351.
- [23] D.V. Lang, *J. Appl. Phys.* 45 (1974) 3023.
- [24] C.O. Thomas, D. Kahng, R.C. Manz, *Electrochem. Soc.* 109 (1962) 1055.
- [25] D.K. Schroder, *Semiconductor Material and Device Characterization*, third ed., John Wiley, New Jersey, 2006.
- [26] B. Bouzazi, N. Kojima, Y. Ohshita, M. Yamaguchi, *AIP Conf. Proc.* 1556 (2013) 30.
- [27] D. Korucu, A. Turut, Ş. Altındal, *Curr. Appl. Phys.* 13 (2013) 1101.
- [28] X. Bao, J. Xu, C. Li, H. Qiao, Y. Zhang, X. Li, *J. Alloys Comp.* 581 (2013) 289.
- [29] L. Stuchlíková, L. Harmatha, M. Petrus, J. Rybár, J. Šebok, B. Šciana, D. Radziewicz, D. Pucicki, M. Tłaczala, A. Kósa, P. Benko, J. Kováč, P. Juhász, *Appl. Surface Sci.* 269 (2013) 175.
- [30] S. Sanyal, P. Chattopadhyay, *Solid-State Electron.* 45 (2001) 315.
- [31] M. Kumar, T.N. Bhat, M.K. Rajpalke, B. Roul, N. Sinha, A.T. Kalghatgi, S.B. Krupanidhi, *Solid-Stat Comm.* 151 (2011) 356.
- [32] N. Bazlov, O. Vyvenko, A. Bondarenko, M. Trushin, A. Novikov, A. Vinogradov, M. Brzhezinskaya, R. Ovsyannikov, *Superlattices Microstruct.* 45 (2009) 190.
- [33] B. Güzeldir, M. Saglām, A. Ates, *Superlattices Microstruct.* 52 (2012) 416.
- [34] R. Padma, B.P. Lakshmi, M.S.P. Reddy, V.R. Reddy, *Superlattices Microstruct.* 56 (2013) 64.
- [35] M. Soyulu, F. Yakuphanoglu, *Superlattices Microstruct.* 52 (2012) 470.
- [36] SILVACO-TCAD, ATLAS User's Manual: Device simulation software, SILVACO International, California, 2004.
- [37] L. Pavesi, F. Piazza, M. Henini, I. Harrison, *Semicond. Sci. Technol.* 8 (1993) 167.
- [38] R.H. Mari, *Electrical characterization of defects in III–V compound semiconductors by DLTS*, PhD thesis, Nottingham, 2011.
- [39] S.E. Laux, *Techniques for small-signal analysis of semiconductor devices*, *IEEE Trans. Electron Dev.* 32 (1985) 2028.
- [40] S.M. Sze, *Physics of Semiconductor Devices*, second ed., John Wiley, New York, 1982.