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Simulation de l'effet de la température et les défauts sur les caractéristiques électriques des diodes à base de GaAs

(Simulation of the temperature and the deep traps effect on the electrical characteristics of GaAs diodes)

Présentée par

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Dedication

I dedicate this work to my late Father who believed in me since I was young.

To the best mother in this world “Victoria”.

ملخص

تعتبر الخاصية سعة-جهد واحدة من أهم التقنيات غير التدميرية المستعملة لتحديد جودة وخصائص انصاف النواقل، حيث تسمح بأخذ نظرة بنيوية أو كهربائية عن طبيعة المركّبات.بالإضافة الى التقنية السابقة، هنالك تقنية اخرى جد مهمة تسمى (DLTS)، حيث تستعمل بكثرة لتحديد تواجد و خصائص العيوب في انصاف النواقل. كلتا التقنيتين السابقة الذكر تعتمد وبشكل اساسي على السعة مما يمنحها اهمية كبيرة في مجال انصاف النواقل.

يتمحور هذا العمل حول عينتان من زرنيخ الغاليوم ذات تطعيم ايجابي بواسطة ذرات السيليكون (Si)، تم توضيعهما باستعمال طريقة MBE على طبقتين حاملتين ذات اتجاهي نمو مختلفين " A(311) و A(211)" مكونتين من زرنيخ الغاليوم النصف ناقل لتشكيل ثنائي صمام من نوع شوتكي. حيث " (311) و (211)" تمثل الاتجه البلوري للنمو، أما الحرف "A" فيعني أن السطح مكون من ذرات الغاليوم (Ga). بعد التحقيق في بنية هاتين العينتين باستخدام تقنية C-V عند درجات حرارة مختلفة وتقنية DLTS، اظهرت هذه الاخيرة وجود أنواع مختلفة من العيوب: حيث ظهر في العينة الأولى A(311) نوع واحد من العيوب و هي العيوب ذات المستويات العميقة الخاصة بالثقوب أما في العينة الثانية A(211) فظهر كلا النوعين. من جهة اخرى ، أظهرت هذه العينات سلوكا غريبا في بعض الخصائص الفيزيائية مثل خاصية السعة بدلالة درجة الحرارة (C-T) و السعة بدلالة الجهد (C-V). حيث اظهرت العينة الاولى "A(311) " تفاضل سعوي سالب "NDC" في الخاصية سعة-جهد، اما العينة الثانية "A(211) " فأظهرت ارتباط صغير بين السعة والجهد.

من أجل ربط ظهور هذا السلوك الغريب بتواجد العيوب ذات المستويات العميقة، تم محاكاة هذه العينات باستخدام برنامج محاكاة يدعى (SILVACO-TCAD). حيث استعمل لمحاكاة خصائص (C-V) و (C-T) لهذه العينات مرة بتواجد العيوب و أخرى في غيابها. وجد أن تواجد توزيع غير منتظم لعيب معين من العيوب المتواجدة في العينة "A(311) " هو المسؤول عن ظهور التفاضل السلبي للسعة. بينما تم ربط الارتباط الضعيف بين السعة والجهد في العينة الثانية " A(211)" بالتعويض الحاصل بين العيوب ذات المستويات العميقة الخاصة بالثقوب و الاخرى الخاصة بالالكترونات.

في الأخير وجد أن نتائج المحاكاة تتفق تماما مع السلوك الملاحظ تجريبيا.

Abstract

The capacitance-voltage (C-V) characteristic is one of the most important characteristic which used to evaluate the quality of semiconductors. It is a non-destructive method of characterization and it gives an insight into the devices (structural and electrical information). Deep Level Transient Spectroscopy (DLTS) is another technique frequently used to characterize defects in semiconductors.

In this work two silicon-doped p-type Gallium Arsenide (GaAs) samples were grown by Molecular Beam Epitaxy on (211)A and (311)A oriented GaAs semi-insulating substrates to form Schottky diodes. (211) and (311) indicate the crystallographic orientation of the substrate while the letter A indicates a Ga-terminated surface. They are investigated using C–V measurements at different temperatures and DLTS. These samples showed a strange behaviour of capacitance-voltage and capacitance-temperature characteristics. The C-V characteristics of the (311)A sample showed a negative differential capacitance (NDC) while those of the (211)A sample showed a smaller than usual sensibility to voltage. DLTS revealed the existence of different types of defects in the two samples. In the (311)A structure only majority deep levels (hole traps) were observed while both majority and minority deep levels were present in the (211)A sample.

In order to relate this behaviour to the observed deep levels, a thorough numerical simulation using the SILVACO-TCAD software is carried out to simulate the C–V and the C-T characteristics in the absence and presence of different types of deep levels. It was found that a non-uniform distribution of one of the deep acceptors is responsible for the NDC phenomena in the (311)A sample while the non-sensitivity of the capacitance to voltage is related to compensation between deep acceptors and deep donors in the (211)A sample.

Résumé

La caractéristique capacité-tension (C-V) est une des techniques les plus importantes utilisées pour évaluer la qualité des semiconducteurs. C'est une méthode non-destructive de caractérisation, elle donne une perspicacité dans les composants (informations structurale et électrique). DLTS (*Deep Level Transient Spectroscopy*) est une autre technique fréquemment employée pour caractériser les défauts dans les semiconducteurs. Ces techniques sont basées sur la capacité ce que la donne une grande importance dans le domaine de semiconducteurs.

Dans ce travail, Deux échantillons de GaAs de type p dopés au Si ont été déposés par MBE sur des substrats du semi-isolant GaAs orienté (211)A et (311)A pour former des diodes Schottky. (211) et (311) indiquent l'orientation cristallographique du substrat tandis que la lettre indique que la surface est terminée par des atomes Ga. Ils sont étudiés en utilisant la méthode C-V à différentes températures ainsi qu'avec la technique DLTS. Ces échantillons ont montré un comportement étrange des caractéristiques de capacité-tension et capacité-température. DLTS a indiqué l'existence de différents types de défauts dans les deux échantillons: Dans la structure (311)A, seulement des niveaux profonds des porteurs majoritaires (pièges de trous) ont été observé tandis que des niveaux profonds des deux types des porteurs (pièges de trous et électrons) ont été observé dans l'échantillon (211)A. Les caractéristiques C-V de l'échantillon (311)A ont montré une capacité différentielle négative (NDC) tandis que ceux de l'échantillon (211)A ont montré une sensibilité plus petite qu'habituelle à la tension.

Afin de relier ce comportement aux niveaux profonds observés, une simulation numérique complète est effectuée pour simuler les caractéristiques C–V et C-T dans l'absence et la présence de différents types de niveaux profonds en utilisant le logiciel SILVACO-TCAD. On a constaté que le phénomène de NDC dans l'échantillon (311)A est dû à la distribution non-uniforme d'un des niveaux accepteurs profonds tandis que la non-sensibilité de la capacité à la tension est liée à la compensation entre les niveaux accepteurs profonds et les niveaux donneurs profonds dans l'échantillon (211)A.

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Chapter 1

Introduction

Semiconductors are the base materials for modern electronic and optical devices and play a key role in current technologies including computers, cell phones, light emitting diodes, lasers, detectors, solar cells, optical amplifiers etc. The semiconductor based devices appeared for the first time in1874 by the discovery of rectification in metal–sulfide semiconductor contacts by (F. Braun). In 1938 Schottky suggested that this effect can be realized using a contact between semiconductor and a metal which is later called after him [1]. The Schottky junction has since attract a great interest from Scientists until the discovery of the first P-N junction by V. Lashkaryov in 1941 [2] and the first bipolar transistor by Bardeen and Brattain in 1947[3]. But the Schottky junction gained its importance again by the realization of the MOSFET (metal oxide semiconductor field effect transistor) by D. Kahng and M.M. Atalla in 1960 and MESFET (metal oxide semiconductor field effect transistor) by W.W. Hooper and W.I. Lehrer in 1967 [1]. Both the MOSFET and MESFET are based on a Schottky junction. Its importance in semiconductor materials electrical characterisation is also increased since it is the most suitable device for a DLTS (deep level transient spectroscopy) [4]. That put the Schottky junction on the top of scientific semiconductor subject again.

Historically the main used semiconductors were Silicon and Germanium. But since it was discovered as a semiconductor material, Gallium-Arsenide took a good position in semiconductor based devices world due to its properties. It is known that Silicon still get the majority of semiconductor market till now, due to its low cost and abundance in nature. But from the perspective of performance, no one disagrees that the III-V compound semiconductor (Gallium-Arsenide) is more efficient compared to Silicon. The most important advantage of gallium arsenide is the speed; where electrons travel about five times faster in Gallium-Arsenide than they do in Silicon. This makes GaAs the most used material in high frequency operating range devices such as metal-semiconductor field effect transistors (MESFETs). Intrinsic Gallium arsenide also has a high resistance to electrical current. Thus,

GaAs is considered semi-insulating material, which makes it a good material to use as a wafer, or substrate. Gallium arsenide also offers a wider range of operating temperatures than silicon and much higher radiation hardness, which is a decisive advantage for military and space programs. Another major advantage is that gallium arsenide can be doped in such way that it emits light, which makes it useful for lasers and light-emitting diodes (LEDs). Recently the performance of devices gained a great importance over the cost, making the GaAs market strongly expanded based on required tools in our daily life [5], such as RF devices (power amplifiers, switches…), the development of 3G/4G networks and the increased demand for data communication. Also LEDs and their associated applications are currently booming due to advantages offered over traditional light sources.

The technologically useful properties of a semiconductor often depend upon the types and concentrations of the defects it contains. Take as an example the semiconductor's type (P or N) or even the semiconductor lasers where the population inverse depends on the presence of traps levels in the bandgap. On the other hand, the presence of defects is not always beneficial, especially when we talk about deep levels. These defects severely affect the device performance i.e. their charging can affect numerous aspects of defect properties, including physical structure, rate of diffusion, and interactions with the electrons that give the semiconductor its overall characteristics. For example, the reduction of free carriers life time which affects the mobility, or the presence of non-radiative defects which degrades the efficiency of light emitting diodes and lasers. Overall, there is a general lack of knowledge of the key parameters of the defects involved, and therefore it is very important to characterise these defects and understand their effect on semiconductors. A comprehensive understanding of such behaviour enables "defect engineering" whereby material performance can be improved by controlling bulk and surface defect behaviour. Various forms of "defect engineering" have been developed to control defect behaviour within the solid [6], particularly for applications in microelectronics.

1.1. About simulation

1.1.1. What is the importance of simulation?

The increased importance of semiconductor simulation has been primarily due to the growing complexity of semiconductor fabrication processes, the shrinking device dimensions and the need to reduce the time and the cost of fabrication to competitive levels. Experimental research and development cost and time for electronic product development can be reduced

by taking advantage of TCAD tools, thus making TCAD indispensable for modern devices and process technologies.

Usually, simulation is used when the analytic methods do not adequately represent the system being studied. For example, in some situations, the objective function is nonlinear, some of restrictions cannot be modelled by a set of linear constraints, or the problem is simply too large to solve analytically. Semiconductor analysis is a complex task due to the complexities of the equations describing semiconductor device performance. For semiconductor devices, particle conservation is modelled by several cross-coupled non-linear partial differential equations: the interaction of charged particles due to electric fields is modelled by Poisson's equation, and the carriers concentrations relating to particle fluxes and generation and recombination are modelled by continuity equations. Also, electron and hole concentrations are exponentially related to potentials through Boltzmann, Fermi-Dirac, or other exponentially determined probability distribution functions. These equations are difficult to solve by hand, making simulation a desirable alternative.

Another major motivation for using simulation is the possibility of measuring and controlling any physical phenomena. Some indispensable information about the semiconductor devices is not accessible experimentally. For example, the internal bias of a junction, or even the internal quantum efficiency of solar cells, where its calculation depends on internal unmeasurable quantities. Also, some parameters are very hard to control experimentally, or even uncontrollable, which is not the case for simulation. In simulation logic, everything is reachable and under control. Take as an example the presence of defect in semiconductor. In this case simulation can change any traps parameter making the study of its effect possible.

1.1.2. Challenges of simulation

While discrete-event simulation offers some advantage with respect to analytic capabilities, it takes considerable effort to build a simulation model, mainly because of data gathering and modelling difficulties. Especially when we talk about simulation dedicated to experimental comparison; in this case most allowed approximations in analytic are forbidden in simulation. This makes simulation accurately cares about every single parameter of the simulated structures, which is not always provided. Thus every missing parameter is a variable to scan. At first sight, this looks an easy work to do. But, we have to say that there is an exponential relation between the missing variables and the simulation possibilities.

In order to clarify this idea let's take a simple example, which is the presence of peak of high density of four traps (our case). To define this peak we need to define the following parameters: traps energy levels, degeneracy factors, capture cross section (for electrons and holes), maximum densities, peaks positions and characteristic lengths. These seven (7) parameters must be scanned for four different traps, so we are talking about twenty eight (28) variables. Let's now assume that every variable can take just four possibilities, by a simple mathematic calculation we find that we have: $4^{28} = 7.2 \times 10^{16}$ possibilities. Every possibility is a separate code that has its numerical difficulties. This number of possibilities can be reduced by comparing the simulated and the measured results together, and defining which variable is more important to scan. Even sometimes, luck can be an influencing factor.

1.2. Background and motivations

Silicon (Si) and Beryllium (Be) are the main doping elements in Gallium Arsenide (GaAs) and other III–V based semiconductor devices. While Be is a p-type dopant, Si can be either an n-type or p-type depending on the growth conditions. Despite many efforts hole mobilities in Be-doped structures grown on conventional (100) GaAs substrate remained considerably lower than those obtained by growing on (311)A oriented surface, so called high index substrate, using silicon as p-type dopant [7]. It is important to add that the silicon (a group IVA element) impurity in GaAs grown by Molecular Beam Epitaxy (MBE) can act as either a donor (occupies a Ga site: group V) or acceptor (occupies a As site: group III) [8, 9]. This amphoteric dopant is dependent on the substrate orientation [10-12]. Silicon is mainly a donor when the growth is on the (100) surface. However, silicon incorporates preferentially as a donor in (N11)B and as an acceptor on (N11)A surfaces (N = 1, 2,3). A and B denote a Ga- and As-terminated plane, respectively. In addition, in (111)A, (211)A, and (311)A planes, silicon may act as a donor or as an acceptor depending on the substrate temperature and the arsenic overpressure used during the MBE growth. This amphoteric nature of silicon could lead to the development of novel devices. In fact the amphoteric nature of Si facilitates the MBE growth of p-type GaAs/AlGaAs heterostructures on (311)A that have higher hole mobilities than those based on the conventional Be-doped p-type on (100) GaAs plane [13-17]. Thus, the interest in the growth of III–V compound semiconductors such as GaAs, InAs, InGaAs, GaAsSb and AlGaAs on high index planes, other than the conventional (100) orientation, has increased tremendously and attracted a great deal of attention over the last several years. The structural, optical and electrical properties of III–V based structures are found to improve by growing on (N11) planes. The growth of semiconductor layers and

structures strongly depends on the substrate orientation and hence to surface atomic arrangement [18]. This may lead to some defects which could have deleterious effects on the electrical and optical properties of III–V based devices [19].

A wide variety of structures can be grown on high index planes. For example quantum wire structures [20], quantum dots [21, 22], quantum strings [23], InAs three-dimensional islands [24]. InGaAs strained growth on GaAs surfaces results in zero-dimensional quantum dots and the formation of one-dimensional quantum wires is demonstrated during InGaAs MBE growth on GaAs (311)A at high temperature [25]. InGaAs/GaAs quantum wells grown by MBE on GaAs (100), (210), (311), and (731) substrates were investigated for possible application in superluminescent diodes [26, 27].

Although the Deep level Transient Spectroscopy (DLTS) [28] and capacitance–voltage (C–V) profiling [29] are quite old techniques, they are still extensively used in the characterization of semiconductor devices [30]. The combination of these two techniques is to relate the departure of the shape C–V curves from ideality to the presence of defects in the different regions of the semiconductor device (bulk, surface or interface) [31]. An example of this is the so called negative differential capacitance (NDC) effect [32-34]. NDC behaviour is sometimes related to nonuniform distribution of defects [35]. In other structures it is related to quantum states [36]. The temperature and frequency dependence of the C–V characteristics are some of the effects usually related to deep levels [37-40].

1.3. Objectives

In this work two Si-doped p-type GaAs samples were grown by MBE on (211)A and (311)A oriented GaAs semi-insulating substrates(named hereafter NU928 and NU926, respectively), in School of Physics & Astronomy laboratory at Nottingham university. These samples have the same structure except the substrate orientation, which causes a basic difference between them, where the DLTS measurements revealed that the first sample (NU928) contains majority and minority traps while the second one (NU926) contains only majority traps. They are also investigated using C–V measurements at different temperatures; the experimental measurements show different strange behaviours of the capacitance-temperature and capacitance-voltage characteristics for both samples. These results lead to the hypothesis that the presence of different types of defects is the main reason of the observed strange behaviours. This can’t be proved experimentally, so the simulation is the best solution in this case.

The purpose of this thesis is to relate the strange behaviour observed in C-T and C-V characteristics to the observed deep levels by simulation using the ATLAS module of the commercial software (SILVACO-TCAD).

1.4. Scheme of the thesis

This thesis is organised as follows:

Chapter 1 is an introduction about Schottky junction and the importance of the used material in this thesis (Gallium-Arsenide), then an overview about the importance of simulation and its challenges. It contains also a background of the thesis and research objectives.

Chapter 2 is devoted to the description of the fundamental concepts of semiconductors, crystal structure, the properties of GaAs, the principles of metal-semiconductor junction including Schottky junctions and current and capacitance calculation.

Chapter 3 provides information on defects in semiconductors, from structural and electrical point of view, where different types of defect classification are presented. The effect of defects on the capacitance and techniques for the characterisation of deep levels are also covered.

Chapter 4 explains the software used in this thesis (SILVACO TCAD) including its modules (DECKBUILD, ATHENA, ATLAS…) by adopting a Schottky junction as an example.

Chapter 5 is divided into three sections: the first section gives the details of the samples investigated in this thesis and the experimental measurements. The second one describes the different parameters simulated to complete the simulation programme, and presents the capacitance-temperature simulation results including discussions. The last one studies the effect of shallow and deep levels on the capacitance-voltage characteristics for different cases; with uniform and non-uniform distribution, such as different regions with different densities, gradient densities and the presence of a peak with a high density at a certain distance from the surface.

Chapter 6 is based on the overall conclusion of the research work carried out in this thesis and suggestions for a possible future work.

Chapter 2

Schottky diodes

2.1. Introduction

Semiconductors are the base materials for modern electronic and optical devices and play a key role in current technologies including computers, cell phones, transceivers, light emitting diodes, lasers, detectors, solar cells, optical amplifiers etc.

This chapter describes the fundamental concepts of semiconductors, starting by how materials are classified into conductors, semiconductors and insulators and explain the concepts of energy bands, energy band gaps. Then we show the different types of semiconductors. Next, we discuss the space charge region, the capacitance and the current transport in Schottky junction discussing the basic concepts of metal-semiconductor junction. In addition, some important properties of GaAs, the semiconductor used in this work, are discussed generally.

2.2. Materials types

For an isolated atom; the electron distribution relies on Bohr model, which describes the atom as a solar system: a nucleus surrounded by electrons moving in specific orbits depending on

their energy level. If we consider two identical atoms, each one has one orbit, when we bring these atoms closer, the orbit will split into two levels by the interactions between the atoms, considering the Pauli principle which suggest that no more than two electrons can occupy the same energy state at the same time. Now if we consider N atoms brought together to form a solid crystal, in this case the orbit will split into N levels (Figure 2-1). So if N is big enough, the energy levels will form a band, called an energy band.

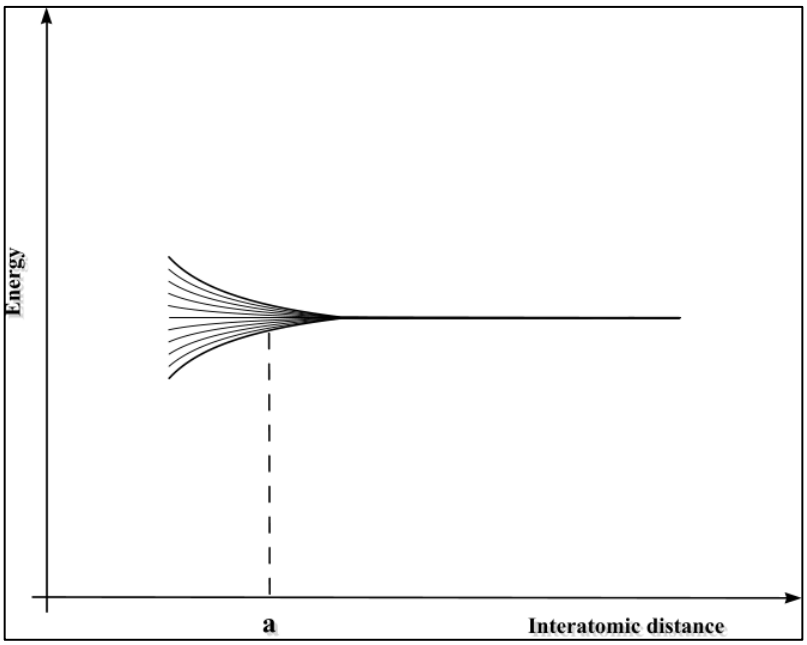


Figure 2-1: Orbit splitting when several atoms come close to each other.

These bands may have a distance between them, merge together, or even separate again after merging according to the Linear Combination of Atomic Orbitals approach [41]. So the final energy band diagram depends on the interatomic distance and the number of electrons. Taking as an example the silicon atom, which has 14, electron and are distributed as follow:

$$1S^2\ 2S^2\ 2P^6\ 3S^2\ 3P^2 \qquad (2\text{-}1)$$

Because the electrons of the first orbits are strongly attracted to the nucleus, they contribute neither to the chemical reactions nor to the electric transport. So only the outer orbits ($3S^2\ 3P^2$) are taken into consideration. Figure 2-2 shows the energy band structure of the outer orbits.

The first band, fully filled with electrons at 0°K, is called the Valence Band (E_V), and the second (empty of electrons) the conduction Band (E_C). The latter is the band that may contains some free electrons that are responsible for conduction of electric current if the

temperature is elevated above 0°K. And finally the gap between the conduction and the valence bands called the forbidden gap. As its name indicates; the space is forbidden for electrons because it doesn't contain any allowed energy level. The position of these bands is very important to define electrical and optical properties of materials. Based on these bands we can classify materials into three main types (Figure 2-3):

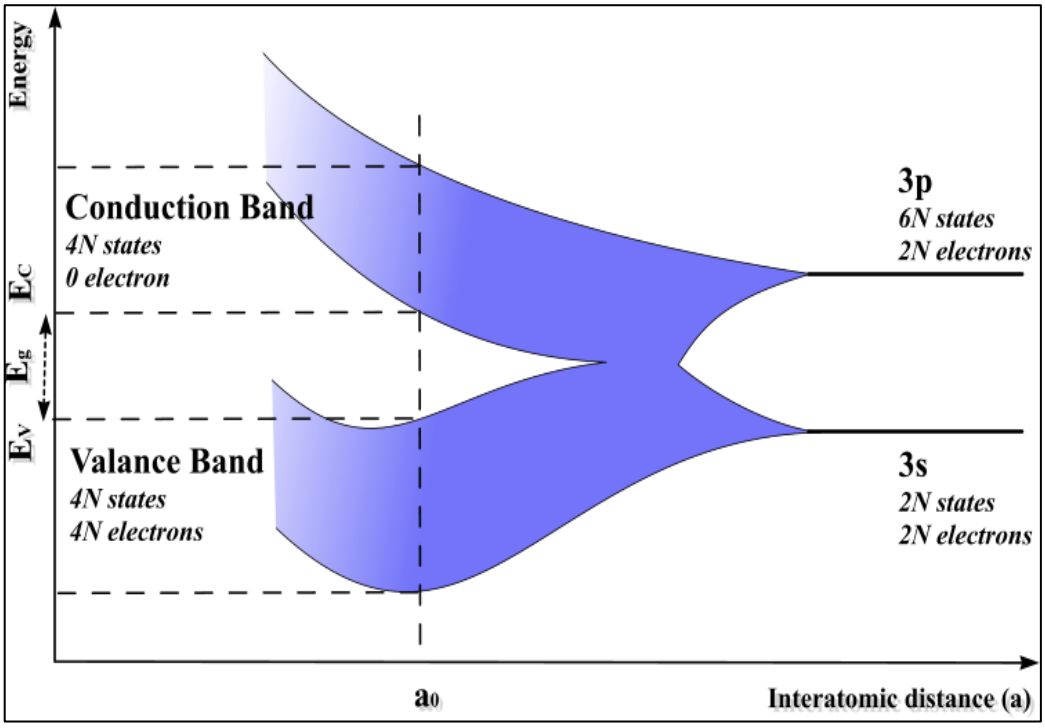


Figure 2-2: Formation of the energy band structure.

2.2.1. Conductors

In this case there is no space between the filled levels and the empty ones. Either the last band is partially filled (as in Copper, Cu), or the valence band is overlapped by the conduction band (as in Zinc, Zn or Lead, Pb). The upper electrons can move freely by applying a small electric field. So they are considered as a free charge carriers, which gives these materials a resistivity smaller than $10^{-3}\Omega.m$ [42].

2.2.2. Insulators

These materials have a very big energy gap (E_g), usually more than 3 eV [42]. In this case, big activation energy is required to shift the electrons from the valence band to the conduction band. This gives the insulators a resistivity range from 10^4 to beyond $10^{17}\Omega.m$ [42].

2.2.3. Semiconductors

Between conductors and insulators there is a third type of material known as semiconductors, these materials have an energy gap less than 3 eV [42] which make them act as an insulators at 0°K. At higher temperatures, the thermal energy can shift the electrons from the valence band to the conduction band, so that they can move freely through material by applying small electric field, and this gives semiconductors a resistivity range from 10^{-9} to $10^{-3}\ \Omega.m$ [42].

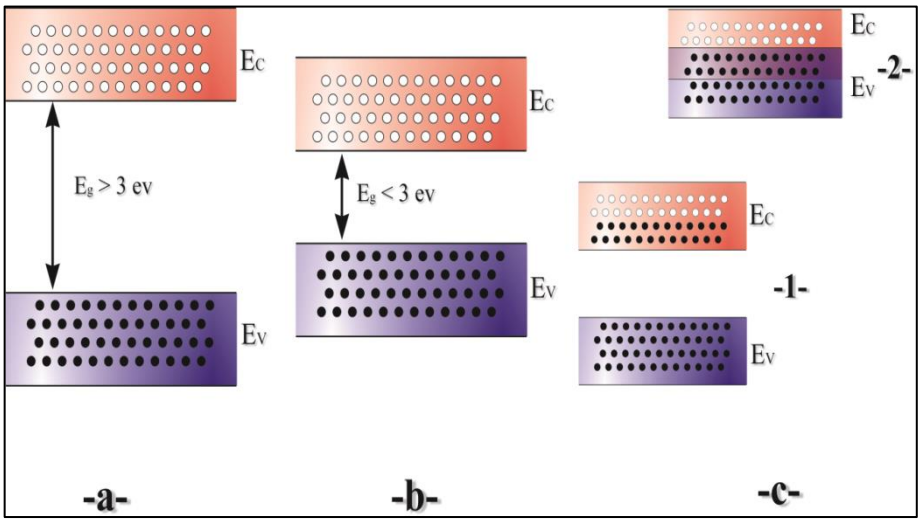


Figure 2-3: Energy band structure for different type of material: a- insulators, b- semiconductors, c- conductors.

2.3. Semiconductors

In semiconductors the current doesn't depend only on electrons, it depends also on the positive vacancies that are left in atoms by electrons, known as "Holes". So we have two different types of carriers (electrons and holes).

2.3.1. Intrinsic semiconductors

In pure semiconductors (which are also known as intrinsic semiconductors) there are no mobile carriers at 0° K. As temperature is raised, electrons from the valence band are thermally excited into the conduction band, and in equilibrium there is an electrons density (n) and an equal holes density (p).

2.3.1.1. Carrier concentration

The electrons density is given by the density of states $N(E)$ in conduction band multiplied by the occupancy $F(E)$ integrated over the conduction band:

$$n = \int_{E_C}^{\infty} N(E).F(E).dE \tag{2-2}$$

The density of states is defined as the number of allowed states per unit energy. It can be approximated by the density near the bottom of the conduction band for low-enough carrier densities and temperature [1]. It is given by [43]:

$$N_c(E) = \frac{1}{2\pi^2}\left(\frac{2m_e^*}{\hbar^2}\right)^{3/2}(E - E_C)^{1/2} \tag{2-3}$$

Where m_e^* is the effective mass of electrons and E_C is the bottom conduction band edge. A similar expression exists for the valence band except that the energy term is replaced by $(E_V - E)$ and the density of states available below the valence band edgeE_V.

The occupancy is the probability of transition of electrons from the valence band to conduction band, which is a strong function of temperature and energy, and it is given by the Fermi-Dirac distribution as:

$$F(E) = \frac{1}{1+\exp[(E-E_F)/KT]} \tag{2-4}$$

Where $E_F$is the highest energy level occupied by electrons at 0° K, and it is called Fermi level. $K$is Boltzmann constant.

For small values of n (non-degenerate case) the term $(E - E_F)$ is bigger than (KT), so the exponential becomes much bigger than the unit (1). Then we can simplify the Fermi-Dirac distribution to:

$$F(E) = \exp[(E_F - E)/KT] \tag{2-5}$$

By replacing equations (2-3) and (2-5) into (2-2) we get:

$$n = N_C . \exp[(E_F - E_C)/KT] \quad (2\text{-}6)$$

We get also a similar equation for the holes:

$$p = N_V . \exp[(E_V - E_F)/KT] \quad (2\text{-}7)$$

Where the effective densities of states N_C and N_V are given by:

$$N_C = 2 \left(\frac{m_e^* KT}{2\pi\hbar^2}\right)^{3/2} \quad (2\text{-}8)$$

$$N_v = 2 \left(\frac{m_h^* KT}{2\pi\hbar^2}\right)^{3/2} \quad (2\text{-}9)$$

For a pure semiconductor (intrinsic) where the creation of electron creates also a hole, we generally talk about creation of an electron-hole pair, which means that the concentration of free electrons equal to that of holes: $n = p = n_i$ where n_i is the intrinsic carrier concentration, which is one of the most important semiconductors characteristics. It can be easily verified that:

$$n_i{}^2 = n.p \quad (2\text{-}10)$$

This relation is known as the Mass-action law.

Using equations (2-6) and (2-7) we get:

$$n_i{}^2 = n.p = N_C N_V . \exp[(E_V - E_C)/KT] \quad (2\text{-}11)$$

Then:

$$n_i = \sqrt{N_C N_V} \, . \exp\left[\frac{-E_g}{2.KT}\right] \quad (2\text{-}12)$$

Where E_g is the forbidden gap and it is equal to:

$$E_g = E_C - E_V \quad (2\text{-}13)$$

Note that $n.p$ is a function only of the temperature and material properties, so it is a constant for a given material at a fixed temperature.

2.3.1.2. Fermi level

The Fermi level is an energy level defined as the highest level occupied by electrons at temperature of 0° K. We can calculate the intrinsic Fermi level E_{Fi} by using equations (2-6) and (2-7) and ($n = p = n_i$)

$$E_{Fi} = \frac{E_C + E_V}{2} + \frac{1}{2}\text{K.T}\, ln\left(\frac{N_C}{N_V}\right) \qquad (2\text{-}14)$$

The intrinsic Fermi energy is typically close to the middle of the energy gap, half way between the conduction and valence band edges.

2.3.2. Extrinsic semiconductors

Semiconductor materials possess exclusive characteristics (such as negative resistance, holes and electrons concentration…) which can be controlled by adding impurities that produces two types of semiconductors:

N-type: By adding donor atoms. For example, in the case of silicon; we can add Phosphor atoms which have five electrons in its external orbit. By making four covalent bonds, the phosphor atoms release the fifth electron. This electron is bound to the Phosphor atom via the Coulomb interaction since the ion core is positively charged compared to the Silicon cores. If the electron is separated from the phosphor atom, by a thermal energy for instance, a fixed positive charge remains at the phosphor site. Then we get an additional electron in the structure for every phosphor atom (Figure 2-4).

P-type: In this case a third group element, like Boron, of the periodic table is added to silicon. This element has three electrons in the external orbit. The Boron atom captures a free electron to make four covalent bonds with the neighbouring Silicon atoms, which produces extra holes in the semiconductor crystal (Figure 2-4).

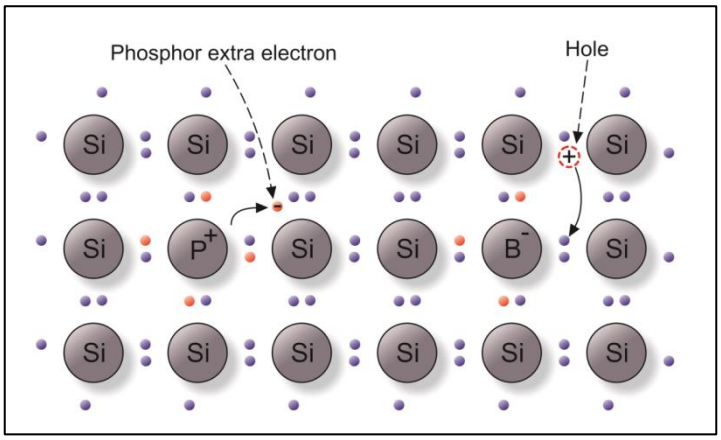


Figure 2-4: The process of capture and release of electrons by impurity atoms when silicon is doped with boron or phosphor respectively.

2.3.2.1. Carrier concentration

When semiconductor doped with a density N_a of acceptors and N_d of donors, the total negative charge must equal the total positive charge. Assuming that all the dopants are ionized in the ambient temperature, we have:

$$n + N_a = p + N_d \tag{2-15}$$

Let us rewrite the mass-action law (2-10) as:

$$p = n_i^2/n \tag{2-16}$$

By replacing (2-16) into (2-15) we get:

$$n - (n_i^2/n) = N_d - N_a$$

$$\Rightarrow n^2 - (N_d - N_a).n - n_i^2 = 0 \tag{2-17}$$

The solution of the equation (2-17) considering n as a variable is:

$$n = \frac{1}{2}\left[(N_d - N_a) + \sqrt{(N_d - N_a)^2 + 4n_i^2}\right] \tag{2-18}$$

Generally, in doped semiconductors, N_d, N_a and $(N_d - N_a)$ are much bigger than n_i, so that we can write the electron concentration, in an N-type semiconductor, as follow:

$$n \approx N_d - N_a \tag{2-19}$$

Taking the mass-action law into account, we can write the hole density as:

$$p \approx n_i^2/(N_d - N_a) \qquad (2\text{-}20)$$

We can get similar equations for a p type semiconductor.

2.3.2.2. Fermi level

Adding of dopants to a semiconductor crystal, changes the free carrier concentration, which affect the Fermi level, this implies a different formula to describe Fermi level than (2-14).

The Fermi level formula of N type semiconductors (E_{Fn}) is calculated by using equations (2-6) and (2-19), thus:

$$N_d - N_a = N_C . \exp[(E_{Fn} - E_C)/KT]$$

$$\Rightarrow E_{Fn} = E_C - KT \ln(\frac{N_C}{N_d - N_a}) \qquad (2\text{-}21)$$

Similarly we can calculate the Fermi level of P type semiconductors (E_{Fp})

$$E_{Fp} = E_V + KT \ln(\frac{N_v}{N_a - N_d}) \qquad (2\text{-}22)$$

As we can see in the last equations (2-21) and (2-22), the Fermi level does no longer depend only on semiconductor intrinsic characteristics, but also on impurities concentration. Figure 2-5 shows the variation of Fermi level in Gallium Arsenide (GaAs) with temperature for different doping type and density temperature.

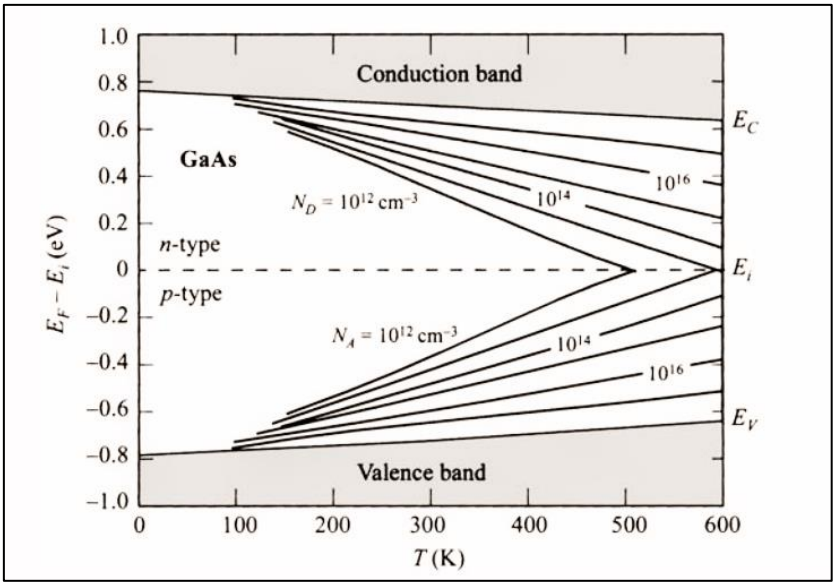


Figure 2-5: The Fermi level in GaAs with temperature for different doping type and density [1].

2.4. General properties of Gallium-Arsenide (GaAs)

2.4.1. Crystal structure

In modern computer and telecommunication applications the most important semiconductors for high-speed devices are Silicon and Gallium-Arsenide. Silicon availability, low cost and advanced technology make it a popular. But the III-V semiconductor compounds (a combination of group III and group V elements of the periodic table) have certain speed advantages over Silicon in their higher carrier mobilities and thus higher effective carrier velocities. Among them, GaAs is the most familiar and most investigated. It was first produced by Goldschmidt in 1920's, but its properties remained unexplored up to 1952 [44].

GaAs is crystallized in a cubic sphalerite (zinc blend) structure [45]. It consists of two face centred cubic lattices of Ga and As, which are mutually penetrated and shifted relative to each other by a quarter of the body diagonal as it is shown in Figure 2-6.

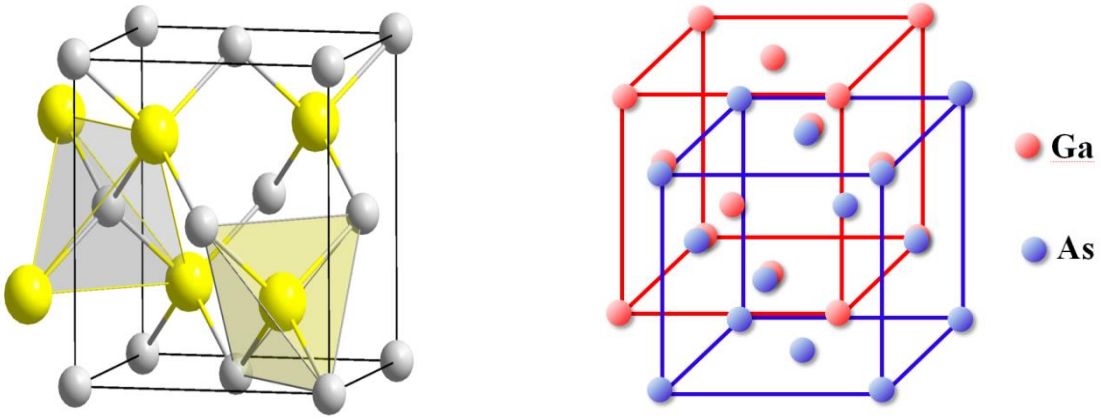


Figure 2-6: Zinc-blende structure of gallium arsenide

The crystal properties along different planes are different (anisotropic), and the electrical characteristics are dependent on a crystal's orientation, which gives importance to the orientation of deposition and the interface's planes. A convenient method of defining the planes in a crystal is to use the Miller indices. If we take as an example the {111} family for GaAs, which contains eight planes, four planes containing only gallium atoms, they are symbolized by the letter "A" [i.e. (111)A]. The other four planes are comprised entirely of arsenic atoms and symbolized with the letter "B" [i.e. (111)B]. These planes are located alternately along the [111] direction (Figure 2-7). The importance of these planes appears when the crystal is chemically etched, subjected to the ion implantation or covered by a passivating dielectric layer. They may affect even the type of doping [10-12].

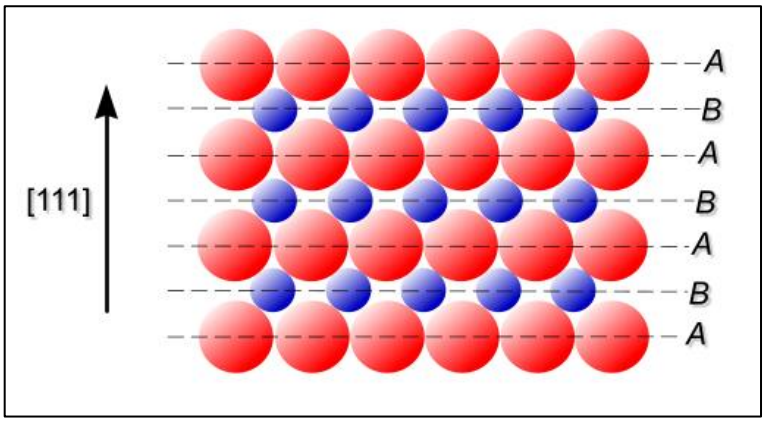


Figure 2-7: Schematic representation of gallium-arsenide structure shows the difference between (111B) and (111A) planes (-A- and -B-respectively).

2.4.2. The energy band structure

The band structure of GaAs is shown in Figure 2-8. It can be seen that both the conduction band minima and the valence band maxima lie at the same value of wave vector at $k = 0$. Therefore, the transition of an electron from valence band to conduction band needs a change in energy, but no change in momentum is required. According to energy band diagram definition the nature of the GaAs band gap is direct. This is an important property, as compared to Si which has an indirect band gap, for devices used in optoelectronics applications.

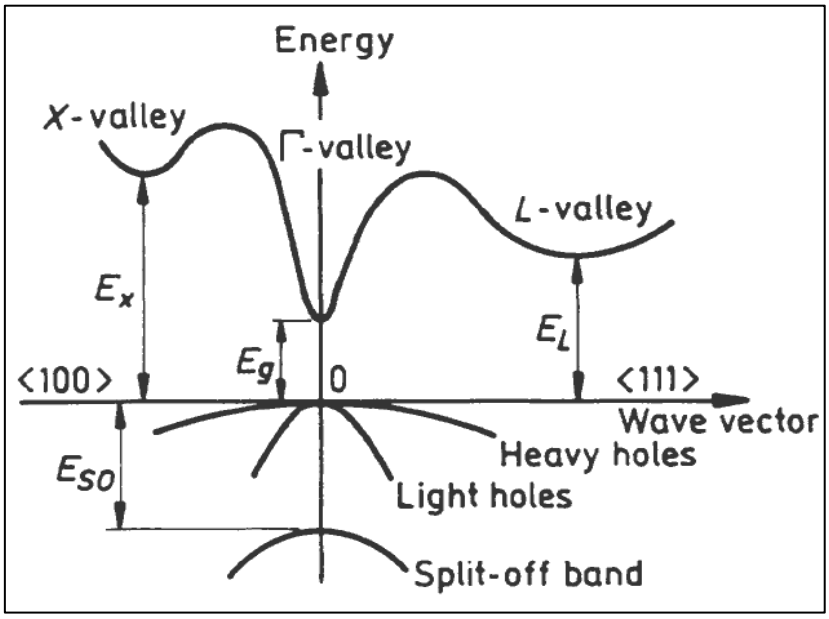


Figure 2-8: Band structure of GaAs at 300°K [46].

2.4.3. Electrical properties

Moreover, GaAs possesses higher carrier mobility than Si, and is preferably used in high frequency devices [45, 47, 48]. The resistivity of GaAs is very high ($\sim 10^8 \Omega cm$) compared to Si ($6.4 \times 10^2 \Omega cm$) [49, 50], which makes it more suitable to be used as a semi-insulating substrate for integrated circuits. In addition, due to the fact that the energy gap of GaAs is higher than that of Si, the GaAs devices are more reliable to operate at higher temperatures than Si devices. Beside the above mentioned selected properties, some other important properties of intrinsic GaAs at room temperature (300°K) are given in Table 2-1.

Parameter	Value	Unit	Parameter	Value	Unit
Crystal structure	Zincblende	-	Electron effective mass	$0.063\ m_0$	-
Lattice constant	5.6533	A°	Hole effective mass	$0.62m_0\ (h_h)$ $0.087m_0\ (l_h)$	-
Crystal density	5.360	g/Cm^3	Dielectric constant	12.85	static
Energy band gap	1.42	eV	Specific heat	0.08	$Cal/g.K$
Band type	Direct	-	Electron affinity	4.07	eV

Table 2-1: Some important properties of intrinsic GaAs at 300K; h_h and h_l stand for heavy hole and light hole, respectively [51, 52].

2.5. Metal-Semiconductor junction

Because all semiconductor devices require connection to metallic wires in order to join components together; the metal semiconductor junction is one of the most important subjects in this area. And it is considered also as the oldest semiconductor device [53]. We will first define some basic terms in this structure before treating the conduction phenomenon in some details.

2.5.1. The work function

The work function of a material is defined as the minimal energy required to extract an electron from it. In term of energy levels, it is the difference between the Fermi level and vacuum level, and it is noted $q\phi_m$ for metals and $q\phi_s$ for semiconductors.

$$q\phi = E_{Vacuum} - E_f \tag{2-23}$$

The work function of metals is in the range of $4 - 6\ eV$ [54] as shown in Figure 2-9 [55],

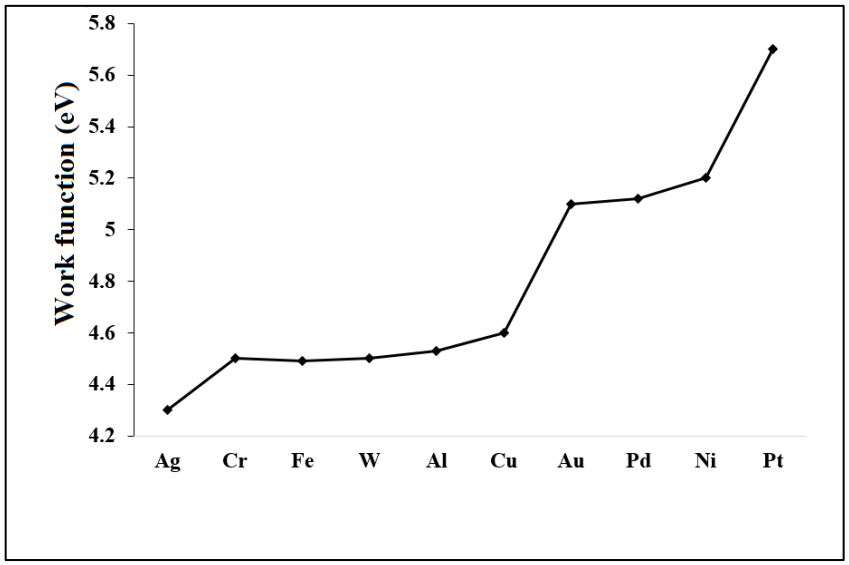


Figure 2-9: The work function of different metals [55].

2.5.2. The electronic affinity

Because the Fermi level is in the forbidden gap in insulators and semiconductors; and which depends mainly on the semiconductor doping density, it is not worth to talk about the work function of a semiconductor. In this case we must use another definition instead of the work function, which is the electronic affinity. It is the difference between the vacuum level and the minimum of the conduction band, and it is noted $q\chi$ where:

$$q\chi_s = E_{Vacuum} - E_C \tag{2-24}$$

2.5.3. The energy band diagram

When a metal and a semiconductor are brought together, two conditions must be taken in consideration. The first one is the Fermi level alignment which is due to the thermodynamic equilibrium. The second is the continuity of the vacuum level (a discontinuity in the vacuum

level would imply an infinite electric field [53]). These two requirements give rise to the energy band diagram for the metal-semiconductor system shown in Figure 2-10.

If the work functions of the metal and semiconductor used are different there will be a bend of the band structure near the junction in the semiconductor side. This bend is due to the electrons movement across the junction. Note that since the metal side has an enormous electron density, the metal Fermi level or the band profile does not change when a small fraction of electrons are added or taken out.

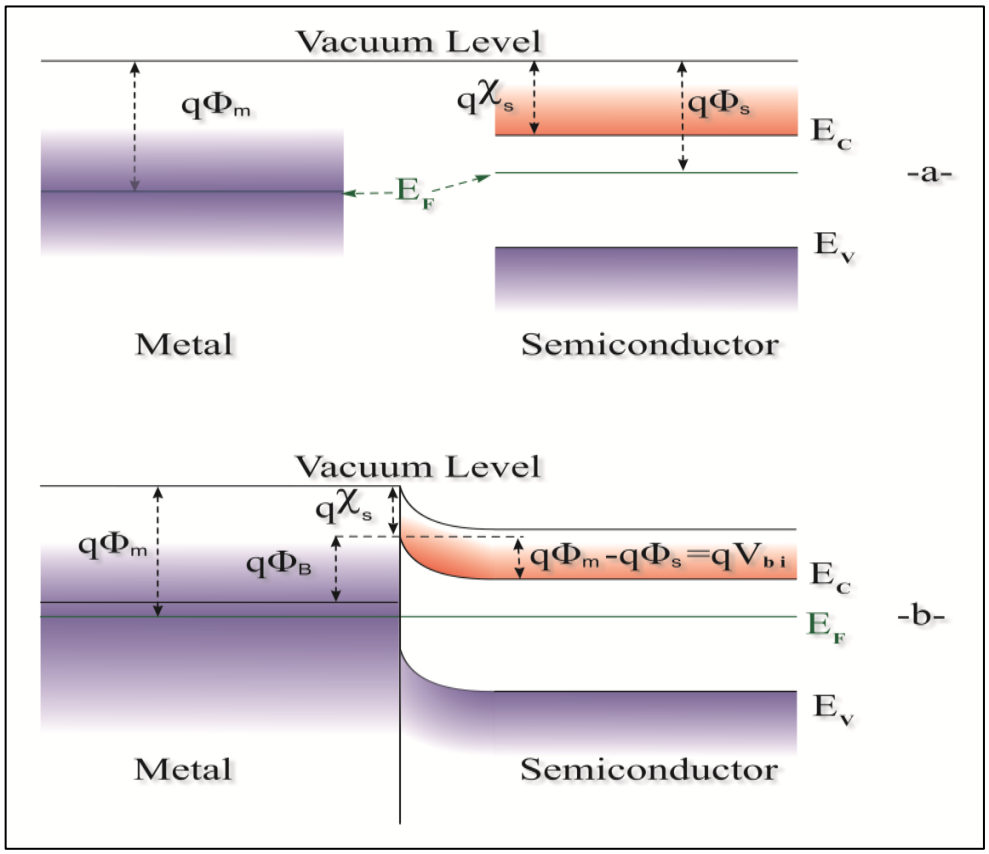


Figure 2-10: The band diagram of metal and semiconductor: (a) before contact and (b) after contact.

The importance of the difference between the metal and semiconductor work functions implies two cases; even the semiconductor work function is bigger than the metal work function, or the inverse.

2.5.3.1. The first case $\phi_m > \phi_s$

Before the contact, the energy band diagram is shown in Figure 2-11 for an N-type and P-type semiconductor respectively. After the contact, the Fermi level must be aligned and the electrons move out from semiconductor side to metal side. The conduction and valance bands will bend upwards as shown in Figure 2-11 and Figure 2-12.

If the semiconductor is an N-type, this electron movement leaves behind a decrease in electron concentration and the Fermi level moves away from the conduction band. A positively charged fixed due to doping element and a deserted region near the metallurgic junction is thus created. This produces a dipole in the vicinity of the metal semiconductor junction (Figure 2-11-a). In this case the junction will be rectifying and it is known as a Schottky contact.

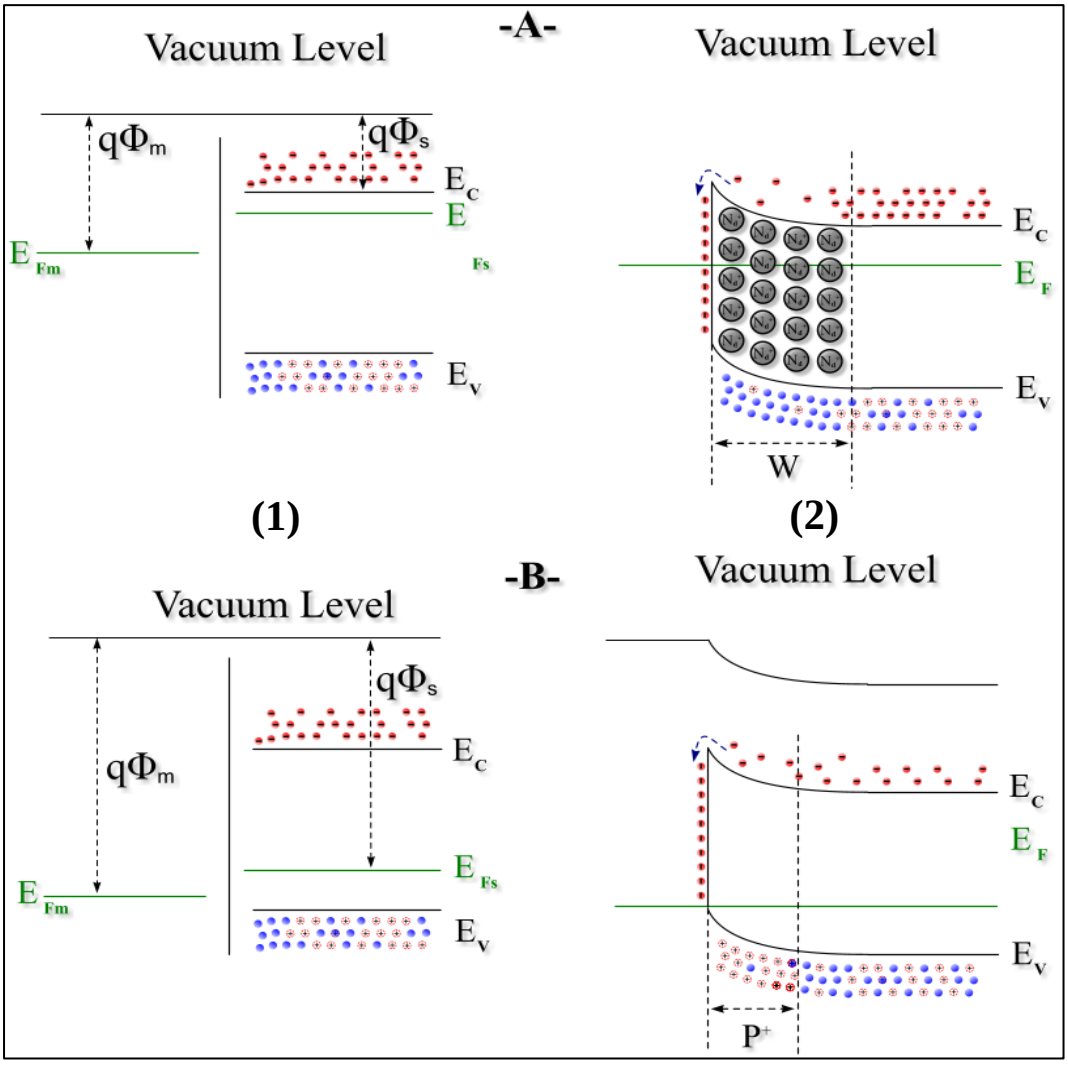


Figure 2-11 Metal-semiconductor band diagram before and after contact (1 and 2 respectively) when $\Phi_m > \Phi_s$: A- N-type semiconductor, B- P-type semiconductor.

A hole concentration increase is obtained if the semiconductor is a P-type, thus holes accumulate near the metallurgic junction. This region acts as a heavily doped region (P^+), and will be an ohmic contact (Figure 2-11-b).

2.5.3.2. The second case $\phi_m < \phi_s$

Before the contact, the energy band diagram is shown in Figure 2-12-a and b for an N-type and P-type semiconductor respectively. After the contact, the Fermi level must be aligned and the electrons move out from the metal side to the semiconductor side. The conduction and valance bands will bend downward as shown in Figure 2-12-a & b.

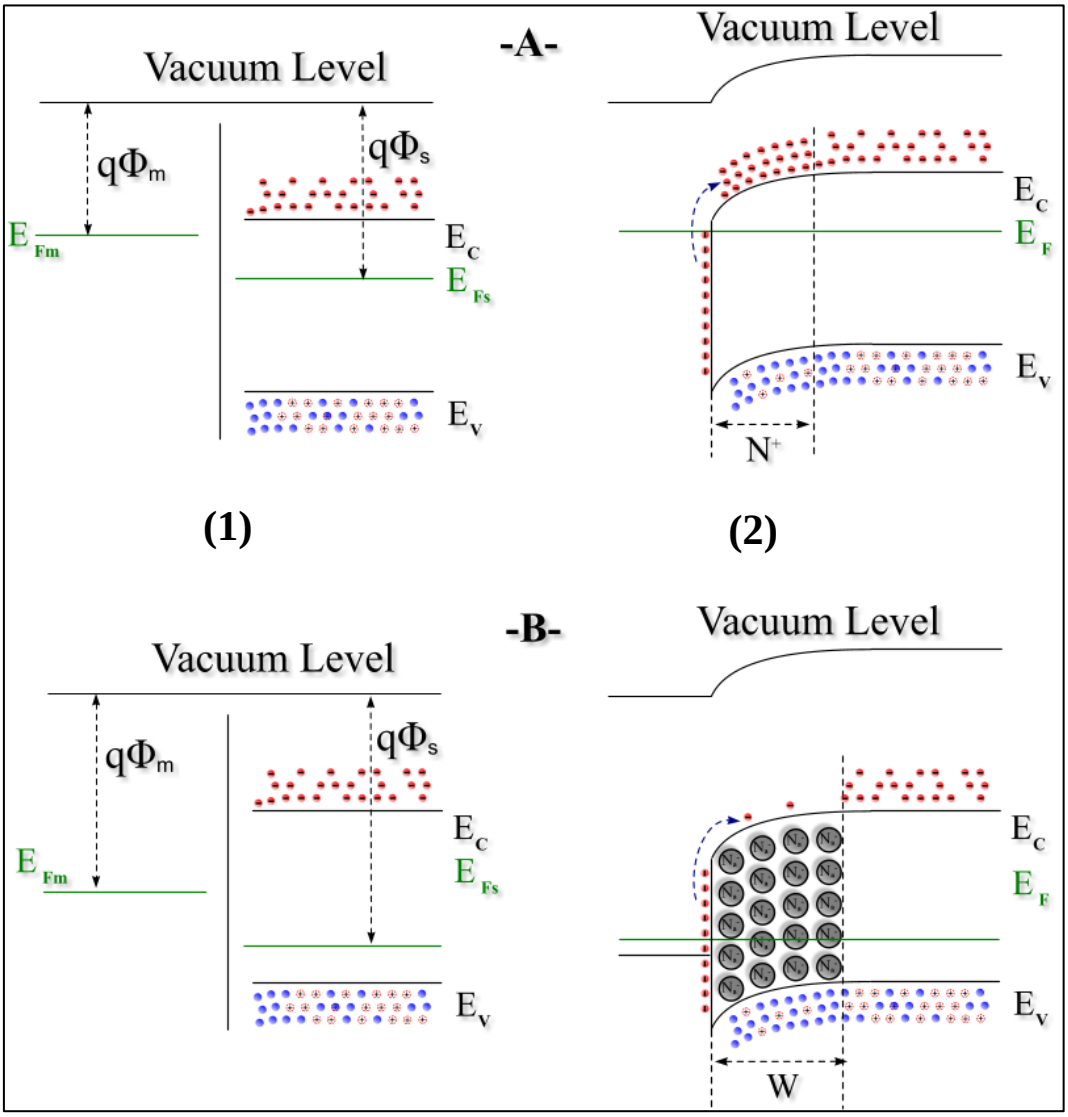


Figure 2-12: Metal-semiconductor band diagram before and after contact (1 and 2 respectively) when $\Phi_m < \Phi_s$: A- N-type semiconductor, B- P-type semiconductor.

Unlike the previous case, the electrons this time move out from metal side to semiconductor side causing an increase of electron concentration, which leads to a band bending as it is shown in Figure 2-12-a & b. In this case, the N-type semiconductor makes an ohmic contact (Figure 2-12-a) while the p-type makes a Schottky junction (Figure 2-12-b).

2.6. Schottky junction

In this section, the Schottky junction will be detailed, which means the n-type semiconductors in case of$\phi_m > \phi_s$, or p-type in case of$\phi_s > \phi_m$.

2.6.1. Schottky barrier and built-in voltage

The difference between metal and semiconductor's work function in Schottky junction imposes a barrier for electrons (n-type) and holes (p-type) that move across this junction. For n-type semiconductor-metal junction, the barrier height at the junction for the injection of electrons from metal to semiconductor conduction band is the difference between the metal work function and the electron affinity of semiconductor as shown in Figure 2-10. It is known as Schottky barrier (ϕ_B), where:

$$q\phi_B = q\phi_m - q\chi_s \tag{2-25}$$

And for p-type semiconductor the barrier is equal to:

$$q\phi_B = E_g - q(\phi_m - \chi_s) \tag{2-26}$$

On other hand, the bands bending impose another barrier for the injection of electrons from semiconductor to metal. This barrier is known as the built-in voltage, and it is equal (for n-type case) to:

$$V_{bi} = \phi_m - \phi_s \tag{2-27}$$

And for p-type:

$$V_{bi} = \phi_s - \phi_m \tag{2-28}$$

2.6.2. Space charge region

To determine the deserted area in n-type Schottky junction, first we consider that the charge density "ρ" in this area is equal to doping concentration "$q(N_A^- - N_D^+)$" and equal to zero outside it. Now we can determine the potential by using the one dimensional Poisson's equation:

$$\frac{d^2\varphi(x)}{dx^2} = -\frac{\rho}{\epsilon_s} \tag{2-29}$$

Where $\epsilon_s$is the static dielectric constant of the semiconductor.

by taking into account as a boundary conditions that the charge density "ρ" in the space-charge region is given by the doping density:

$$\rho(x) = q(N_D - N_A) \qquad 0 \le x \le w \tag{2-30}$$

And the electric field outside the depletion region equals to zero:

$$\xi(x) = 0 \qquad x \ge w \tag{2-31}$$

The electric field is then obtained by integrating the equation (2-29):

$$\frac{d\varphi(x)}{dx} = -\xi(x) = -\frac{q(N_D - N_A)}{\epsilon_s}x + \xi_m \tag{2-32}$$

By replacing the electric field by its value at the depletion region edge which is zero we can find the constant "ξ_m", Where $\xi_m$is the maximum field at $x = 0$.

$$-\xi(w_0) = -\frac{q(N_D - N_A)}{\epsilon_s}w_0 + \xi_m = 0 \tag{2-33}$$

$$\Rightarrow \xi_m = \frac{q(N_D - N_A)}{\epsilon_s}w_0 \tag{2-34}$$

$$\Rightarrow \frac{d\varphi(x)}{dx} = -\xi(x) = -\frac{q(N_D - N_A)}{\epsilon_s}(x - w_0) \tag{2-35}$$

Finally, by integrating the above equations, We can find:

$$\varphi(x) = -\frac{q(N_D - N_A)}{\epsilon_s}\left(\frac{1}{2}x^2 - w_0 x\right) + c \tag{2-36}$$

Now, by taking into account that the potential at the junction is equal to $(-V_{bi})$.we can find that the constant "c" is:

$$c = -V_{bi} \tag{2-37}$$

$$\Rightarrow \varphi(x) = -\frac{q(N_D - N_A)}{\epsilon_s}\left(\frac{1}{2}x^2 - w_0 x\right) + -V_{bi} \qquad (2\text{-}38)$$

Taking into account the condition $\varphi(w_0) = 0$ and the equation (2-38) we obtain:

$$w_0 = \sqrt{\frac{2\epsilon_s}{q(N_A - N_D)} V_{bi}} \qquad (2\text{-}39)$$

The assumption we made at the beginning of this section is not accurate behind the limit of space charge region, where the concentration of free carriers is significant compared to the dopant ions concentration. In this case equation (2-39) is corrected to[55, 56]:

$$w_0 = \sqrt{\frac{2\epsilon_s}{q(N_A - N_D)} (V_{bi} - \frac{KT}{q})} \qquad (2\text{-}40)$$

When an external potential (V_{ext}) is applied to the junction the internal field will decrease and therefore reduce the total potential difference, the formula (2-40) becomes:

$$w = \sqrt{\frac{2\epsilon_s}{q(N_A - N_D)} (V_{bi} - V_{ext} - \frac{KT}{q})} \qquad (2\text{-}41)$$

2.6.3. Capacitance

To calculate the capacitance the charge density stored in the space charge region which is mainly due to ionized dopant atoms must be defined first. So, the charge density per unit surface at the thermodynamic equilibrium is given by:

$$Q(V) = q(N_A - N_D)w = \sqrt{2q\epsilon_s(N_A - N_D)(V_{bi} - V_{ext} - \frac{KT}{q})} \qquad (2\text{-}42)$$

From (2-42) the capacitance $C = |dQ(V)/dV|$ of the space charge region is equal to:

$$C = \sqrt{\frac{q\epsilon_s|N_A - N_D|}{2\left(V_{bi} \pm V_{ext} - \frac{KT}{q}\right)}} \qquad (2\text{-}43)$$

Where the "+" sign applies to p-type ($N_A > N_D$) and the "–" sign to n-type ($N_D > N_A$) junctions and V_{ext} is the reverse-bias voltage. For n-type junctions$N_D > N_A$,$V_{bi} < 0$and$V_{ext} < 0$, whereas for p-type junctions $N_A > N_D$, $V_{bi} > 0$ and $V_{ext} > 0$. The (KT/q) in the denominator accounts for the majority carrier tail in the space-charge region which is omitted in the depletion approximation.

Equation (2-43) shows that the depletion layer capacitance is inversely proportional to the square root of the applied voltage. This means that the capacitance will decrease with increase bias, this will appear clearly if we draw the capacitance as a function of bias (Figure 2-13-A). It is also worth to mention that the capacitance is proportional to temperature (note that the temperature appears in the dominator with a negative sign) (Figure 2-13-B).

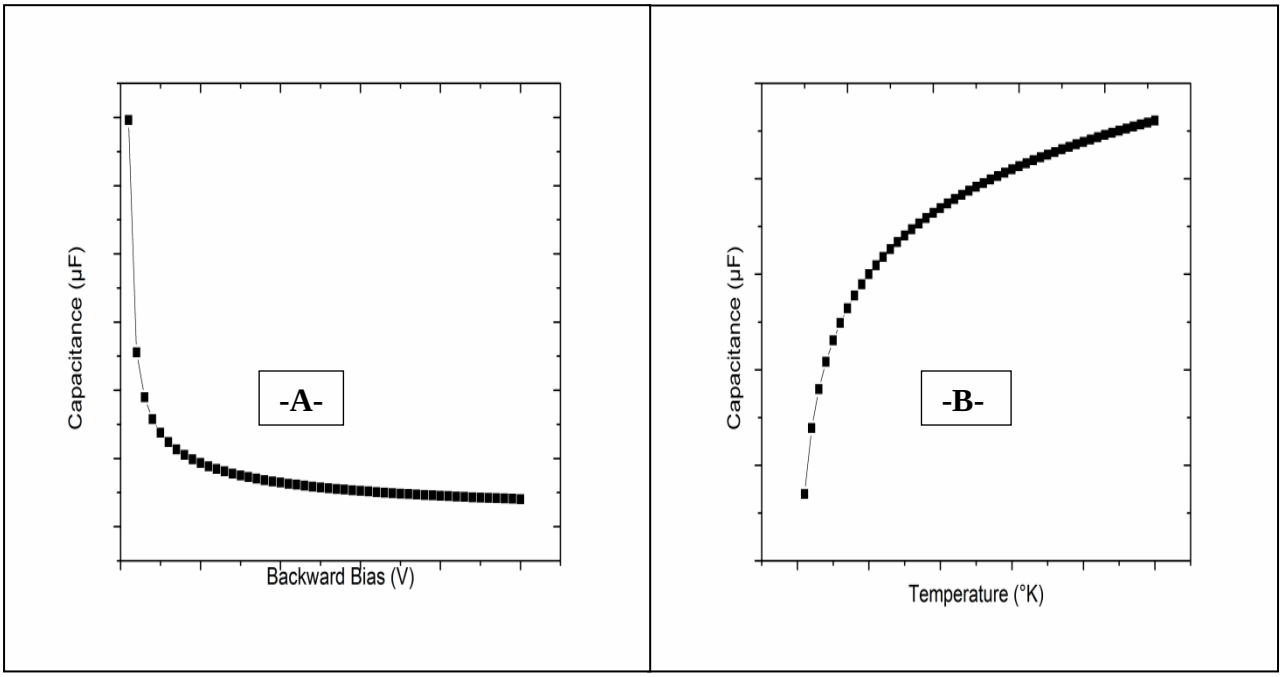


Figure 2-13: Analytic capacitance versus (A) Bias, (B) Temperature.

We can also write the equation (2-43) as follow:

$$\frac{1}{C^2(V)} = \frac{2\left(|V_{bi}| - V_{ext} - \frac{KT}{q}\right)}{q\epsilon_s N_D} \qquad (2\text{-}44)$$

This formula (2-43) is very important because we can use it in experiment to determine the doping concentration of semiconductor, which is proportional to the slope of the graph ($1/C^2 = f(V)$), and the built-in voltage.

2.6.4. Current transport

Unlike the p-n junction where the minority carriers are the responsible for the current, in Schottky junction the current is due mainly to majority carriers. The current transport can be

described by two theories depending on semiconductor properties (thermionic emission theory, diffusion theory). The first one (thermionic) locates the current limitation at the interface between metal and semiconductor, and suggests that the depletion region and the neutral zone do not affect the current. So, in these two regions, the Fermi level is considered constant, and the variation of the Fermi level is located at the interface as a discontinuity. Crossing barrier by carriers is then based on the probability of having energy bigger than the barrier height. On the other hand, the diffusion theory locates the current limitation in the depletion region, it suggests that the Fermi level change progressively along that region and there's no discontinuity at the interface.

2.6.4.1. Thermionic emission theory

In this method the transport phenomena are related to the metal-semiconductor interface. The neutral zone doesn't contribute to the current conduction, neither the space charge region. In these both regions, the pseudo-Fermi level is considered almost constant. The change of the pseudo-Fermi level is located at the interface, therefore it presents a discontinuity. The crossing of barrier is then based on the probability of having free carriers whose energy (due to thermal agitation) is greater than the height of the barrier they must cross, and whose speed component normal to the metal plane is oriented towards the metal. So the current density due to electrons flow from semiconductor to metal is equal to:

$$J_{S\to M} = \int_{E_F - q\phi_B}^{\infty} (-q)\, v_x\, dn \tag{2-45}$$

Where v_x is the electron's velocity normal to the metal plane, and dn is the electron density in a small energy interval (dE), where:

$$dn = N(E).F(E).dE \tag{2-46}$$

$$dn \approx \frac{4\pi(2m^*)^{3/2}}{h^3}\sqrt{E - E_c}\,.\exp\left(-\frac{E-E_F}{KT}\right).dE \tag{2-47}$$

Considering that:

$$E - E_F = E - E_c + E_c - E_F \tag{2-48}$$

The electron density will be:

$$dn \approx \frac{4\pi(2m^*)^{3/2}}{h^3}\sqrt{E - E_c}\,.\exp\left(-\frac{E-E_c}{KT}\right).\exp\left(-\frac{E_c-E_F}{KT}\right).dE \tag{2-49}$$

Now, assuming that the electrons in conduction band have a kinetic energy, we can write:

$$E = E_c + \frac{1}{2}\, m^* v^2 \tag{2-50}$$

$$\Rightarrow E - E_c = \frac{1}{2}\, m^* v^2 \tag{2-51}$$

$$\Rightarrow \sqrt{E - E_c} = v\sqrt{m^*/2} \tag{2-52}$$

And:

$$dE = m^*.v.dv \tag{2-53}$$

Substituting equations (2-52) and (2-53) into (2-49) gives:

$$dn = 2\left(\frac{m^*}{h}\right)^3 \exp\left(-\frac{m^* v^2}{2KT}\right).\exp\left(-\frac{E_c - E_F}{KT}\right) 4\pi v^2 dv \tag{2-54}$$

If the velocity is resolved into its components along the x-axis parallel to the transport direction, we have

$$v^2 = v_x^2 + v_y^2 + v_z^2 \tag{2-55}$$

With the transformation from a Cartesian velocity space to a polar velocity space $4\pi v^2 dv = dv_x dv_y dv_z$, we obtain from (2-45) and (2-54):

$$J_{S\to M} = 2q\left(\frac{m^*}{h}\right)^3 \exp\left(-\frac{E_c - E_F}{KT}\right) \int_{v_{0x}}^{\infty} v_x \exp\left(-\frac{m^*.v_x^2}{2KT}\right) dv_x \,.\int_{-\infty}^{\infty} \exp\left(-\frac{m^*.v_y^2}{2KT}\right) dv_y.$$

$$\int_{-\infty}^{\infty} \exp\left(-\frac{m^*.v_z^2}{2KT}\right) dv_z \tag{2-56}$$

Using integration by change of variable, the current formula is written as follow:

$$J_{S\to M} = \left(\frac{4\pi q m^* K^2}{h^3}\right) T^2 \exp\left(-\frac{E_c - E_F}{KT}\right) \exp\left(-\frac{m^*.v_{0x}^2}{2KT}\right) \tag{2-57}$$

The velocity v_{0x} is the minimum velocity (perpendicular to the metal plane) required to surmount the barrier, which means that the kinetic energy gained from this velocity must be equal to the barrier, so:

$$\frac{1}{2}\, m^* v^2 = q(V_{bi} - V_{ext}) \tag{2-58}$$

Where V_{ext} is the applied voltage. From (2-57) and (2-58), we find:

$$J_{S\to M} = \left(\frac{4\pi q m^* K^2}{h^3}\right) T^2 \exp\left(-\frac{E_c - E_F}{KT}\right) \exp\left(-\frac{qV_{bi}}{KT}\right) \exp\left(\frac{V_{ext}}{KT}\right) \quad (2\text{-}59)$$

$$\Rightarrow J_{S\to M} = \left(\frac{4\pi q m^* K^2}{h^3}\right) T^2 \exp\left(-\frac{q\phi_B}{KT}\right) \exp\left(\frac{V_{ext}}{KT}\right) \quad (2\text{-}60)$$

The final formula is written as:

$$J_{S\to M} = A^* T^2 \exp\left(-\frac{q\phi_B}{KT}\right) \exp\left(\frac{V_{ext}}{KT}\right) \quad (2\text{-}61)$$

Where A^* is the effective Richardson constant for thermionic emission. And it is equal to:

$$A^* = \left(\frac{4\pi q m^* K^2}{h^3}\right) \quad (2\text{-}62)$$

Since the external bias doesn't affect the Schottky barrier, thus it doesn't affect the current due to electrons flow from metal to semiconductor. Which must be equal to the current flowing from the semiconductor into the metal when thermal equilibrium prevails (i.e., when V_{ext}). Therefore the current from the metal into the semiconductor is equal to:

$$J_{M\to S} = -A^* T^2 \exp\left(-\frac{q\phi_B}{KT}\right) \quad (2\text{-}63)$$

Finally, the current–voltage characteristic in the thermionic emission model is the sum of all currents:

$$J = J_{S\to M} + J_{M\to S} = A^* T^2 \exp\left(-\frac{q\phi_B}{KT}\right)\left[\exp\left(\frac{V_{ext}}{KT}\right) - 1\right] \quad (2\text{-}64)$$

$$\Rightarrow J = J_S\left[\exp\left(\frac{V_{ext}}{KT}\right) - 1\right] \quad (2\text{-}65)$$

Where J_S is called the saturation current and it is equal to:

$$J_S = A^* T^2 \exp\left(-\frac{q\phi_B}{KT}\right) \quad (2\text{-}66)$$

2.6.4.2. Diffusion theory

The diffusion theory assumes that the barrier height is much larger than kT, and the carrier concentrations at the interface metal-semiconductor and at the start of depletion region, are unaffected by the current flow (i.e. they have their equilibrium values), and finally, the semiconductor must be non-degenerate.

Since the current in the depletion region depends on the local field and the concentration gradient, we must use the current density equation[57]:

$$j_n = -q\mu_n n(\mathrm{x})\mathrm{E} - KT\mu_n \, {dn(x)}/{dx} \tag{2-67}$$

In stationary state the current density is independent of x, so after integration and using the potential formula we find:

$$j_n = j_s \left[\exp\left(\frac{qV}{KT}\right) - 1\right] \tag{2-68}$$

Where:

$$j_s = -q\mu_n N_c \varepsilon_m \exp\left(\frac{-q\phi_B}{KT}\right) \tag{2-69}$$

2.6.5. Image-Force Lowering (Schottky effect)

The presence of a free porter (electron) in the semiconductor near the metal contacts leads to the creation of an attractive force by electrostatic effect and thus an electric field. This field induces a potential difference and therefore a change in the energy diagram. Because the created force is attractive, the potential difference created is negative, thus corresponds to a lowering of the existing barrier. This lowering is known as the image-force lowering or the Schottky effect.

2.6.5.1. Electron in vacuum fronts a metal plane

To calculate the barrier lowering, we consider first an electron in the vacuum at distance "x" from a metal plane. In this case the attractive force (known also as the image force) is given by:

$$F = \frac{-q^2}{4\pi\varepsilon_0}\frac{1}{(2x)^2} = \frac{-q^2}{16\pi\varepsilon_0 x^2} \tag{2-70}$$

Where $\varepsilon_0$is the permittivity of free space. The work done by this electron to arrive from infinity to the position "x" is:

$$E(x) = \int_{\infty}^{x} F.dx = \frac{-q^2}{16\pi\varepsilon_0 x} \tag{2-71}$$

When an external electric field ($\xi(x)$ oriented in the –x direction) is applied, the total potential energy is given by the sum:

$$E_P(x) = \frac{-q^2}{16\pi\varepsilon_0 x} - q|\xi|x \tag{2-72}$$

Compared to the maximum height of energy barrier, the presence of an electron behind the metal plane causes a barrier lowering of ΔE (Figure 2-14), which can be deduced by calculating the position where the total potential energy is at its maximum value.

$$\left.\frac{dE_P(x)}{dx}\right|_{x=x_m} = 0 \tag{2-73}$$

$$\Rightarrow \frac{q^2}{16\pi\varepsilon_0 x_m^2} - q|\xi| = 0 \tag{2-74}$$

$$\Rightarrow x_m = \sqrt{\frac{q}{16\pi\varepsilon_0|\xi|}} \tag{2-75}$$

And the barrier lowering is equal to:

$$\Delta E = 0 - E_P(x_m) = q\sqrt{\frac{q|\xi|}{4\pi\varepsilon_0}} \tag{2-76}$$

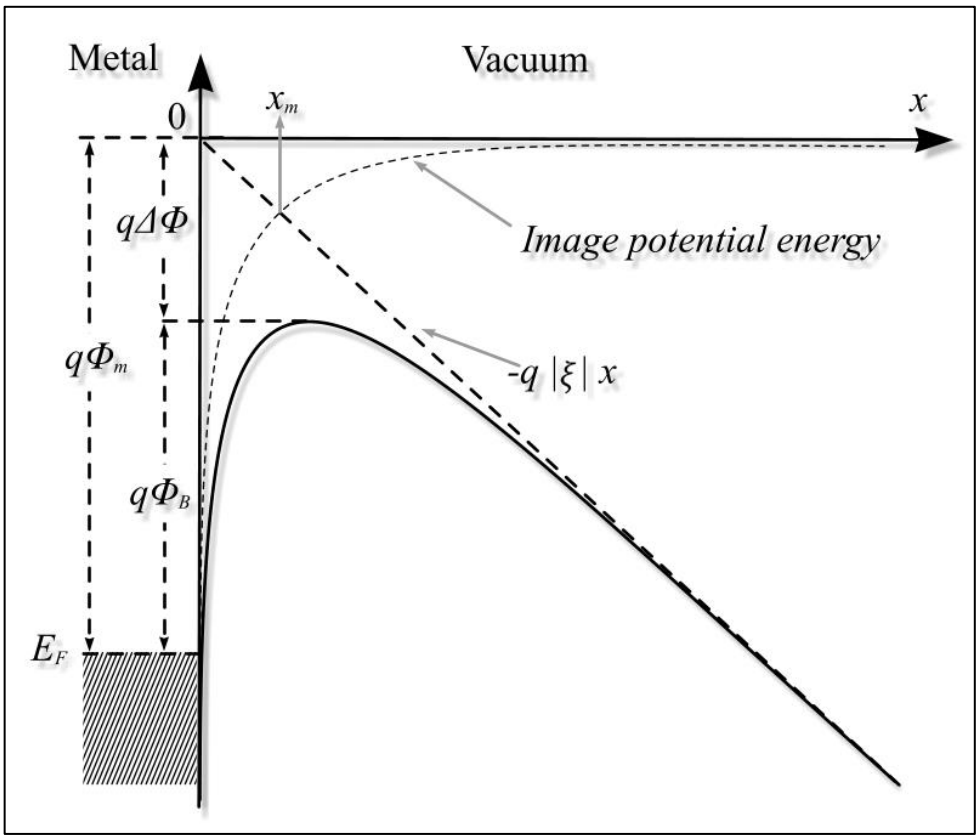


Figure 2-14: Energy-band diagram between a metal surface and a vacuum.

2.6.5.2. Electron in semiconductor front of a metal plane (Schottky junction)

In the case of Schottky junction where the electron is in a semiconductor, the electric field in the space charge region is generated by the ionized dopants, and it is calculated by the integration of the Poisson equation. For a constant doping, the electric field changes linearly as a function of "x". In this case the barrier lowering calculation is much complicated. Assuming that the value of "x_m" is much smaller than the depletion region width, the electric field is considered constant and equal to its maximum value, which can be deduced using (2-38), and it is equal to:

$$\xi(x_m) \approx \xi_{max} = \frac{q(N_D - N_A)}{\varepsilon_s}.w \tag{2-77}$$

Where $\varepsilon_s = \varepsilon_r \varepsilon_0$ is the static dielectric constant of the semiconductor, and w is the depletion region width (see equation (2-41)).

Finally, the value of the Schottky barrier lowering ($\Delta\Phi$) is deduced by substituting (2-77) into (2-76):

$$\Delta\Phi = \sqrt{\frac{q|\xi|}{4\pi\varepsilon_s}} = \sqrt{\frac{q^2(N_D - N_A)}{4\pi\varepsilon_s^2}w} \tag{2-78}$$

The Schottky barrier will take a corrected value, as follow:

$$\Phi_B = \Phi_{B0} - \Delta\Phi \tag{2-79}$$

The Figure 2-15 shows the energy diagram incorporating the Schottky effect for a metal on n-type semiconductor under different biasing conditions.

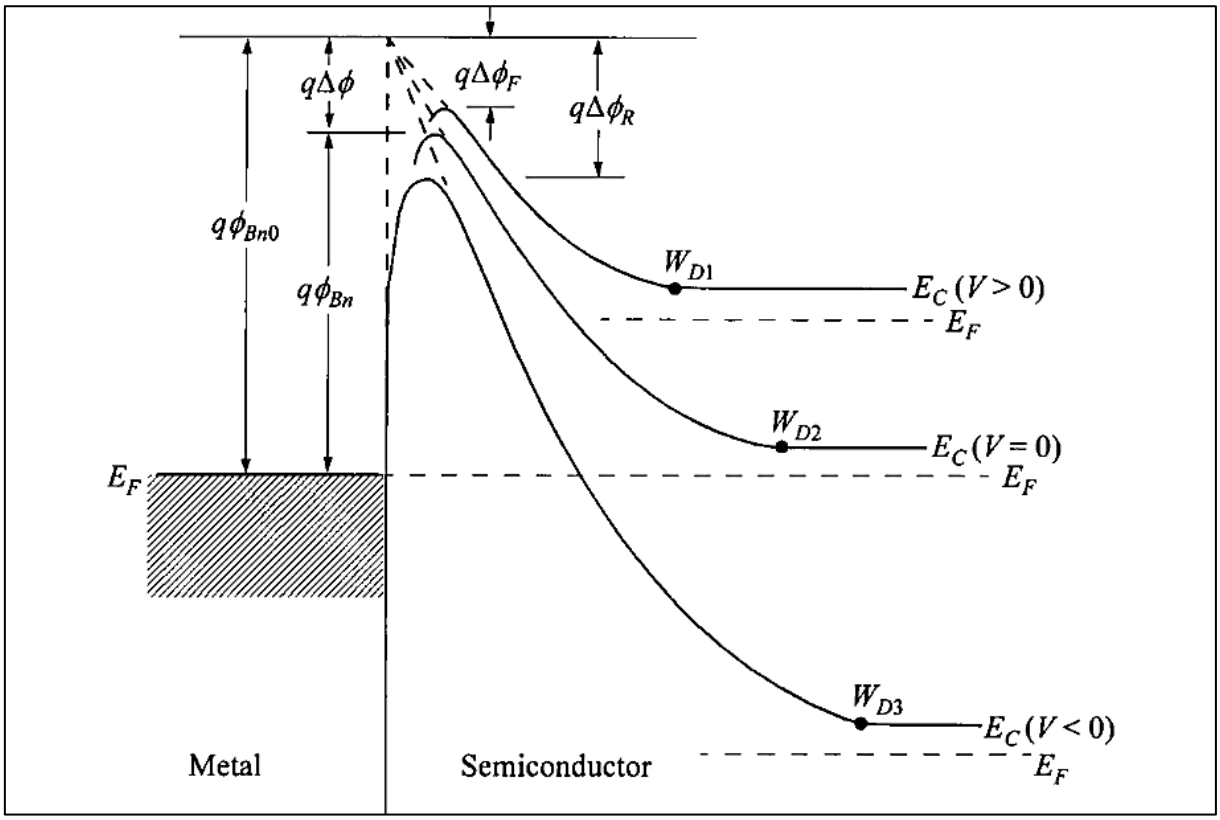


Figure 2-15: Energy-band diagram incorporating the Schottky effect for a metal n-type semiconductor contact under different biasing conditions. The intrinsic barrier height is $q\Phi_{Bn0}$. The barrier height at thermal equilibrium is $q\Phi_{Bn}$. The barrier lowering under forward and reverse bias are $\Delta\Phi_F$ and $\Delta\Phi_F$ respectively.

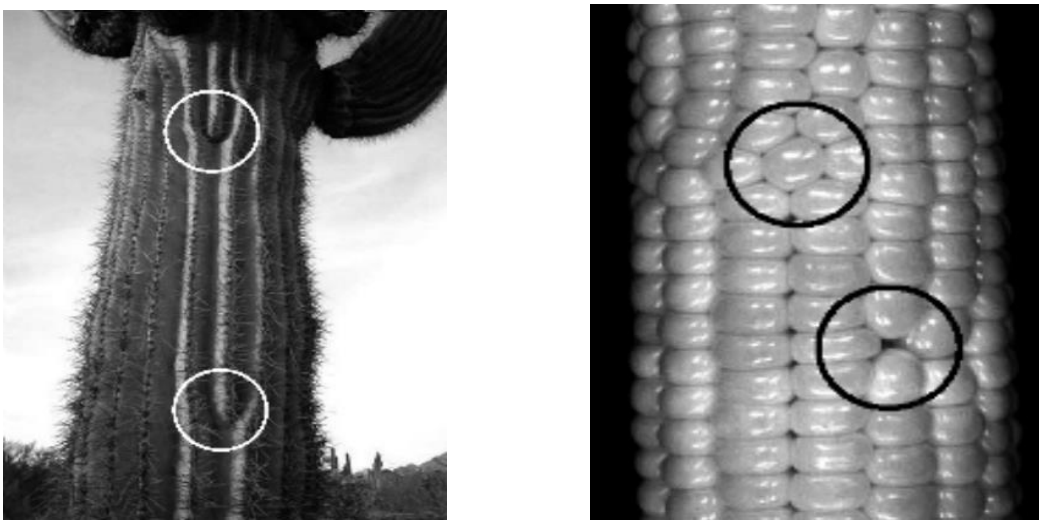
Chapter 3

Semiconductor Defects

3.1. Introduction

A crystal (perfect structure) is defined as a strictly periodic repetition of a motif of atoms in the three directions of space. Between this ideal case and the other one (amorphous materials) there are intermediate situations that include most real solid crystals. The arrangement of the atoms in most of these solids always differs from the perfect structure, this difference is called defects.

The presence of defects in the solid crystal affects its properties, such as the mechanical, electrical and optical characteristics. Figure 3.1 presents examples of defects in some common everyday life natural objects.



-a- **-b-**

Figure 3.1: Schematic representation of some defects in nature, a tree (a) and a corn (b).

The word "defect" should not be taken only in its negative sense. If some are undesirable, in other cases the defects have a beneficial effect on many properties, and sometimes, they are absolutely necessary to achieve desired properties. Good examples are the case of semiconductor's doping and the semi-insulating properties of semiconductor substrates for devices and integrated circuits.

Defects can be classified in several ways. First, taking into account their location in the crystal, they can be classified into bulk defects and interfaces defects. Second, they can be classified also by their creation method (structural viewpoint: vacancies, interstitial, substitution … etc.) or by their energy level (shallow and deep defects). Also by taking into account their mechanical effects or electrical effect or optical…etc. In this chapter we will present the different type of structural defects, than we will interest by their electrical classification.

3.2. Types of defects

3.2.1. Zero dimension defects (Point defects)

The point defects are those which are not extended in space in any dimension. There is no strict limit for how small a "point" defect should be. But typically the term is used to describe defects which involve at most a few extra or missing atoms without an ordered structure of the defective positions (defects of the atomic order size). The point defects have a local effect that means they usually affect only a few interatomic distances. They may be built-in with the original crystal growth, or activated by heat. Moreover, they may be the result of radiation, or electric current …etc. Figure 3.2 presents few types of point defects in real structure.

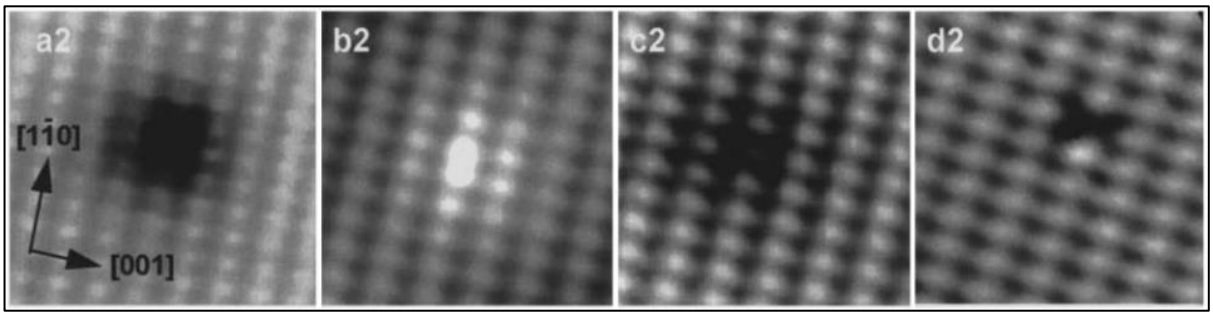


Figure 3.2: Images of the major defects in Si-doped GaAs (110) surfaces (a2) show a V_{Ga}, (b2) Si_{Ga} donor, (c2) Si_{As} acceptor, (d2) a ($Si_{Ga}V_{Ga}$) complex. Adopted from [58].

3.2.1.1. Vacancy

The vacancy is one of the most common intrinsic point defects. It is defined as the absence of an atom from its original position on a node of the crystal lattice, which is supposed to be filled. This is illustrated in Figure 3.3.

In order to form a vacancy by removing an atom from its lattice site, its bonds have to be broken. The broken bonds can form new bonds depending on the charge state of the vacancy, which is just the number of electrons occupying the dangling bonds; this bonding causes small inward or outward displacements of neighbouring atoms. This either preserves the local symmetry (relaxation) or alter it (distortion), and affect the crystal properties.

The number of vacancies increases exponentially with the absolute temperature, and can be estimated using the expression [59]:

$$n_V = N.\exp\left(-\frac{E_{Va}}{K.T}\right) \qquad (3.1)$$

Where n_V is the number of vacancies, N is the total number of lattice sites and $E_{Va}$the energy necessary to form a vacancy.

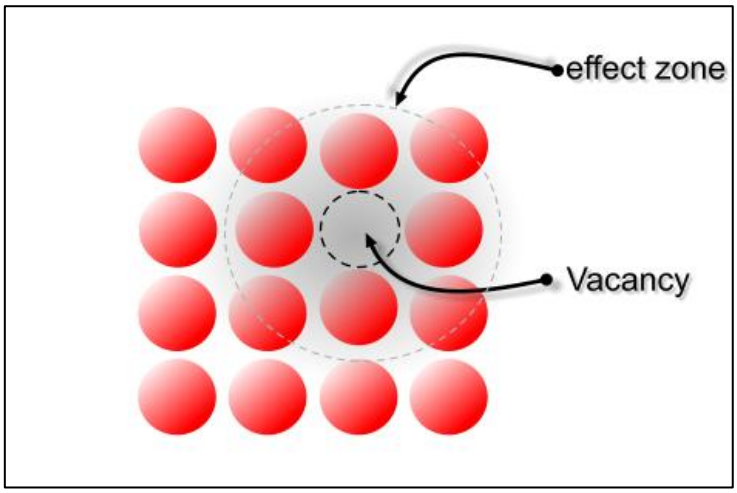


Figure 3.3: Schematic representation of vacancy defect at the atomic scale

3.2.1.2. Interstitial

As its name implies; the interstitials are sites located between the ordinary crystal sites. These sites are considered as defects when they are occupied by atoms. If the interstitial atom is of the same species as the lattice atoms, it is called selfinterstitial (or intrinsic interstitial). This type requires a high energy to be formed, thus, they have generally a high potential energy. Otherwise, if the interstitial atom is a different type then the matrix, it is called interstitial impurity (or extrinsic interstitial). Small atoms in some crystals can occupy interstices without high energy, such as hydrogen in palladium [60] (Figure 3.4).

The presence of interstitial atom may create a local stress, which affects the interatomic distance and changes the crystal properties.

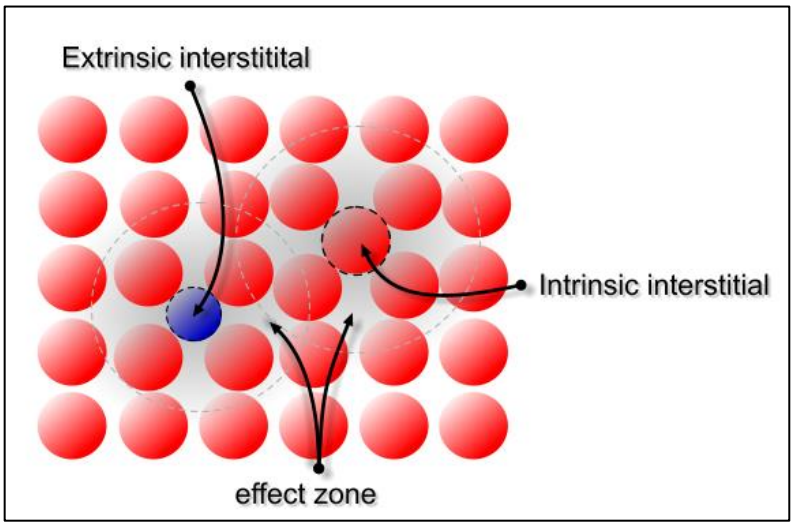


Figure 3.4: Different types of interstitial defects at the atomic scale.

3.2.1.3. Substitution

The substitution is considered as an extrinsic defect, and it is defined as a presence of a foreign atom on a site that belongs (in the ideal case) to an atom of the crystal (see Figure 3.5). This type of defect occurs when the size difference between the foreign and the crystal atoms is in order of 15%.

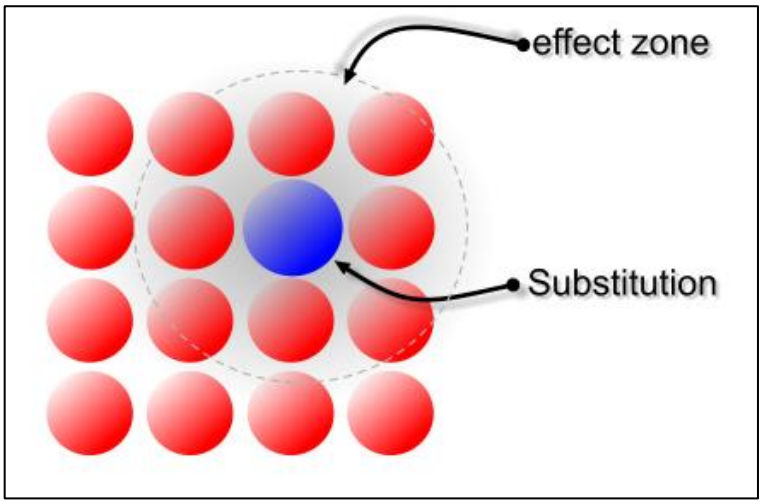


Figure 3.5: Representation of substitution defect at the atomic scale

3.2.1.4. Anti-site

In compound semiconductors, every type of atoms has its position in the crystal (site). The breach of this condition produces a defect known as Anti-site, which is neither a vacancy nor an interstitial, nor a substitution. It occurs when an anion (cation) replaces a cation (anion) on a regular cation (anion) site (for example the presence of "Ga" atom on "As" site in "GaAs") as shown in Figure 3.6.

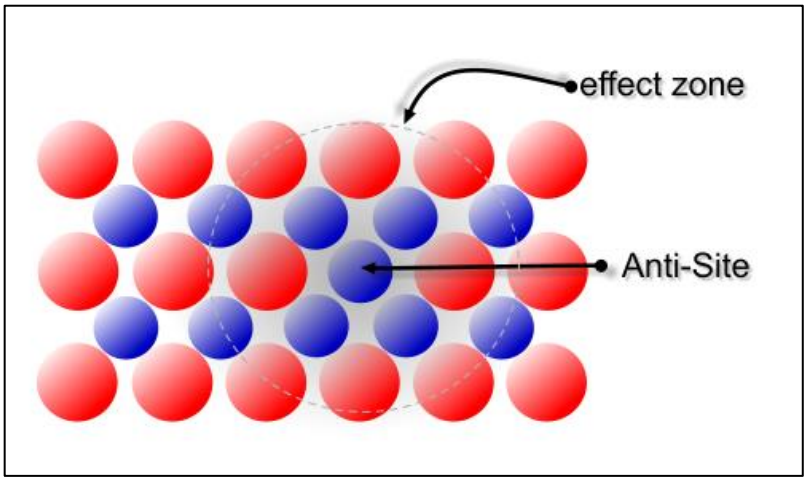


Figure 3.6: Representation of Anti-site defect at the atomic scale in compound materials.

3.2.1.5. Frenkel and Schottky defects (complex defects)

The creation of vacancies in ionic crystals can create different type of complex point defect. If the missing atom has moved into an adjacent interstitial site, it is known as a Frenkel defect. Thus, a Frenkel defect is in reality a pair of defect which consist of an empty lattice site (vacancy) and an extra interstitially positioned atom (see **Figure 3.7**.a). On the other hand, if the missing atom is no longer in the vicinity of the vacancy or has migrated to the surface, in this case the vacancy can form a pair with another close vacancy of opposite charge and creates a Schottky defect (see Figure 3.7.b).

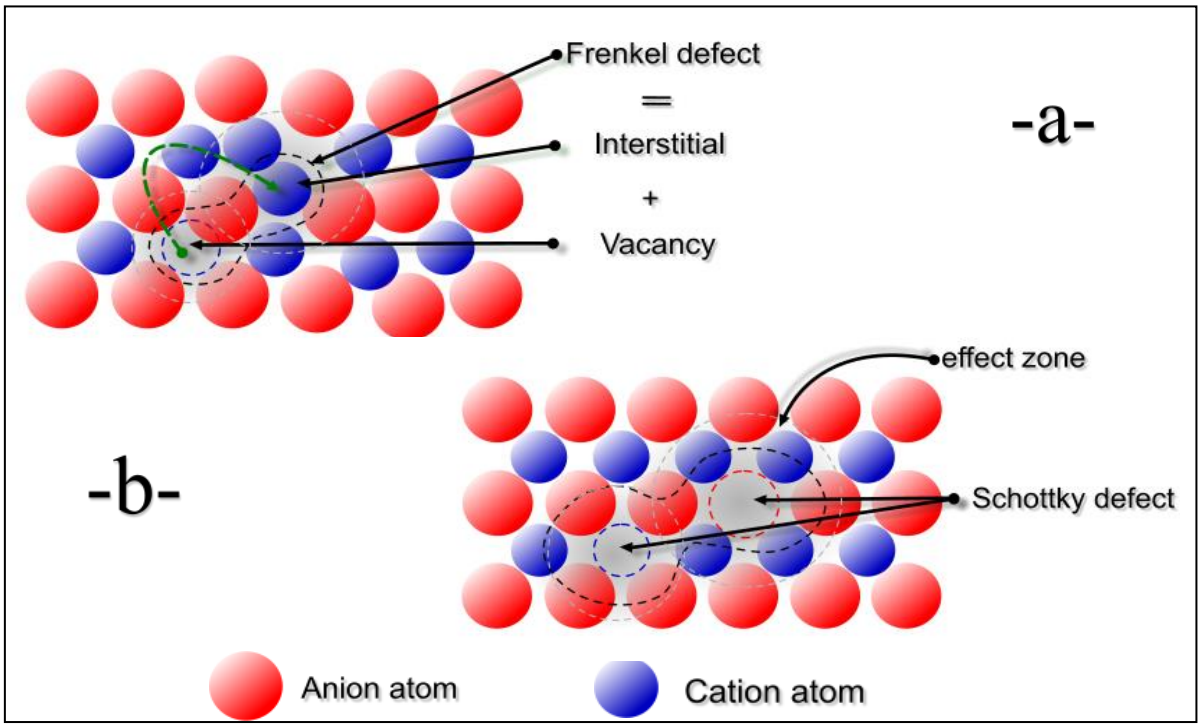


Figure 3.7: Schematic representation defect clusters in compound materials.
-a- Frenkel defect -b- Schottky defect.

3.2.1.6. Point defects notation

A notation has been developed to describe the different types of defects called Kroger-Vink notation. It symbolizes every type of defect by a letter, and its location by a subscript and finally its charge by a superscript as shown in Table 3.1.

The notation	represents
V	Lattice vacancy
M (e.g. Ca, Al …)	Cation atom
X (e.g. O, Cl …)	Anion atom
Subscripts	
I	Interstitial
M	Cation lattice position
X	Anion lattice position
Superscript	
•	Positive charge
'	negative charge

Table 3.1: Summary of Kröger-Vink notation[61].

Taking as an example, the vacancy in compound materials such as GaAs, where there can be two types of vacancies: one created by removing Ga atom, in this case it designed by V_{Ga}, or by removing As atom (V_{As}). Similarly, in the case of interstitial defect, the atom occupying the interstitial position is indicated by Ga or As, thus Ga_i represents a Gallium atom interstitial. Finally, the substitution represented by Ga_{As} if the Ga atom is on an As site and vice versa.

Defect clusters are enclosed in parentheses, for example (V_{Ga} V_{As}) for Schottky defect, or (Ga_i Ga_{AS}) for Frenkel defect to indicate that the individual defects are associated with one another.

3.2.2. One dimension defects (Dislocations)

The concept of dislocation was first proposed by Taylor et al in 1934 [62]. Dislocations are areas were a group of atoms located on the same plane are out of position in the crystal structure. They are considered as a one dimension defect because the locus of defective points produced in the lattice by the dislocation lies along a line. There are two basic types of dislocations, the edge dislocation and the screw dislocation, which are actually extreme forms of the possible dislocation structures that can occur. In real crystals, most dislocations are probably a hybrid of the edge and screw forms and often form complete loops [63].

3.2.2.1. Edge Dislocations

The edge defect can be easily visualized as a missing half-plane of atoms in a lattice. The line of defective points is the first line of the plane opposite the missing plane. The inter-atomic bonds are significantly distorted only in the immediate vicinity of the dislocation line. As it is shown in Figure 3.8.a, the defective line of defective points is surrounded by a red dashed circle.

3.2.2.2. Screw Dislocations

There is a second basic type of dislocation, called screw dislocation. The screw dislocation is slightly more difficult to visualize. It can be described by a cube with a shear stress applied across one end so that the cube begins to rip. This is shown in the Figure 3.8.b.

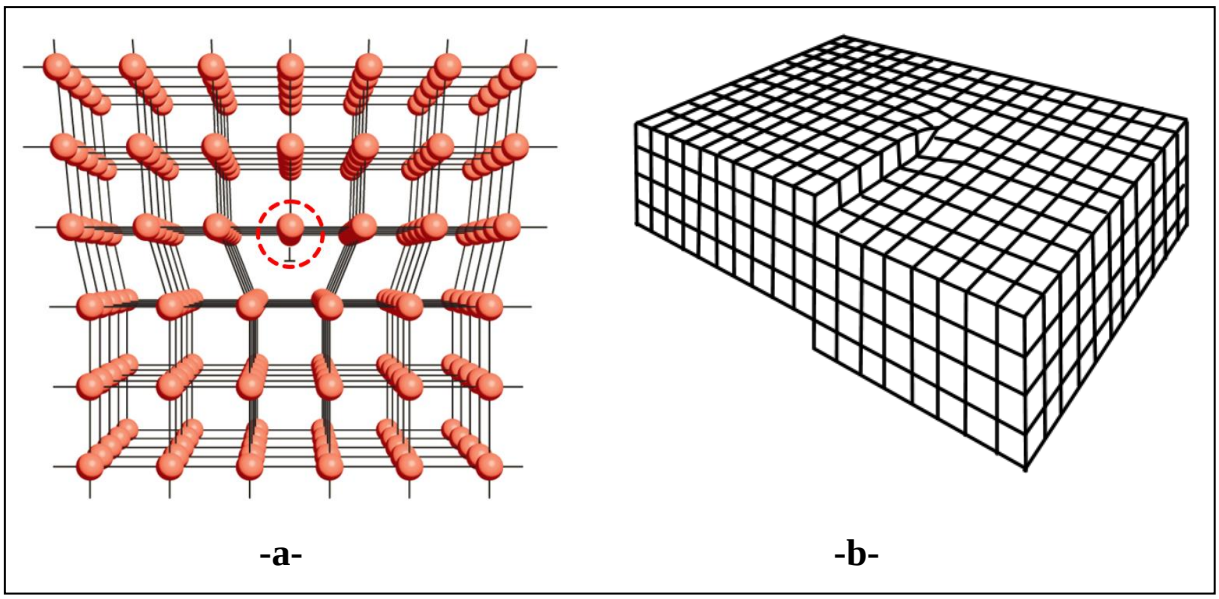


Figure 3.8: Schematic representation of: -a- Edge dislocation in a cubic crystal [64], -b- Screw dislocation

3.3. Electronic Defect States:

Creation of a defect always changes or ruptures atoms' bonds. This leads neighboring atoms to readjust their positions by relaxations of various kinds, and sometimes form new bonds with other neighbors. The relaxations and rebounding produce new orbitals localized in the vicinity of the defect that often have the capacity to capture excess charge from the valence or conduction bands. The capture represents defect ionization, and depends upon charge

availability within the solid as quantified by the Fermi level. The ion cores of semiconductors interact electrostatically with localized charge. That may affect the semiconductor properties.

Electrically active defects in semiconductor crystals have different characteristics. This allows classifying the defects into two main families: shallow levels and deep levels.

3.3.1. Classification

Defects can modify the electrical conductivity of semiconductors as they add new energy levels, which can provide carriers to the conduction or valence bands at energies very much lower than the gap energy. Shallow defects have energy levels within a few tens millielectron volts from the band edges. Whereas deep defects typically reside within the middle third of the semiconductor energy band gap [65]. For example, an impurity which belongs to the groups of the periodic table closest to that of the semiconductor then it tends to create a shallow defect. While, deep levels are created by impurities not belonging to the closest groups in the periodic table [66].

In fact the above simple definition is no longer generally applicable after the discovery of some deep defects which have energy levels close to the bands edges or even within them [56]. Instead, the degree of localization of the defect state is used to classify it. Deep levels have highly localized wave functions whereas shallow level functions are as extended as the far reaching coulomb potential [65]. That means, an impurity for which the long-range Coulomb part of the ion-core potential determines the energetic level is termed a shallow impurity. The extension of the wave function is given by the Bohr radius. This situation is in contrast to a deep level where the short-range part of the potential determines the energy level. The extension of the wave function is then of the order of the lattice constant [56].

3.3.2. Shallow Defects

The shallow defects are produced usually by extrinsic defects (by introducing foreign atoms). The shallow defects affect the semiconductor properties depending on dopant or impurity type, atomic radius, charge, and bulk crystal structure.

For example, consider a semiconductor of Group IV such as Silicon, doped with an atom from column V of the periodic table, such as Arsenic. In the crystal lattice, the arsenic atom replacing a silicon atom establishes links with its four neighbors. The arsenic atom is then

surrounded by nine electrons of which eight of them saturate the binding orbitals of the crystal. The ninth electron occupies an orbital more delocalized within the field of the positive ion As^+. The ionization energy (E_D) of this electron is obtained using the simplest calculation based on the hydrogen-atom model. The ionization energy for the hydrogen atom in vacuum is:

$$E_H = \frac{m_0 q^4}{32\pi^2 \varepsilon_0^2 \hbar^2} = 13.6\ eV \qquad (3.2)$$

where $\hbar$ is the reduced Planck constant. The ionization energy (E_D) is calculated by replacing the electron rest mass (m_0) by the conductivity effective mass of electrons (m_{ce}), and the vacuum permittivity (ε_0) by the permittivity of the semiconductor (ε_S):

$$E_D = E_C - E_d = \left(\frac{\varepsilon_0}{\varepsilon_S}\right)^2 \left(\frac{m_{ce}}{m_0}\right) E_H \qquad (3.3)$$

The ionization energy for donors as calculated from (3.3) is 25 meV for Si and 7 meV for GaAs[1].

On the other hand, if the Silicon atom is replaced by an atom from column III, such as Gallium. In this case, there's a missing electron, which can easily be replaced by an electron from a neighboring atom. The transition of an electron from an intrinsic bond to the atom of Gallium leads to the creation of a hole in the valence band and a negative charge excess in the Gallium atom, which is called acceptor. The hydrogen-atom calculation for the ionization level for the acceptors is similar to that for the donors. The calculated acceptor ionization energy (measured from the valence-band edge $E_A = E_a - E_V$) is 50 meV for Si and GaAs[1].

These energy levels are important in calculating the fraction of dopants being ionized, or electrically active. Also, since these small ionization energies are comparable to the thermal energy (KT), ionization is usually complete at room temperature. Figure 3.9 shows the measured ionization energies for various impurities in Si.

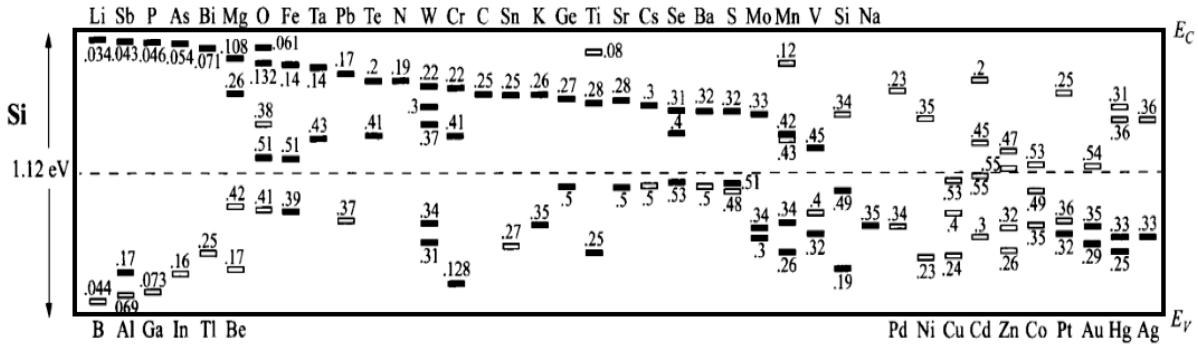


Figure 3.9: Measured ionization energies for varies impurities in Si. Levels below the gap centre are measured from E_V, Levels above the gap centre are measured from E_C, Solid bars represent donor levels and hollow boxes represent acceptor levels [1].

In compound semiconductors, the concept of doping is much complicated, where the dopants in some cases can act as a donors or acceptors. For example, when GaAs is doped with group IV atoms such as Si, Sn, and Ge, isolated substitutional defects form. Foreign atoms that occupy Ga lattice sites become shallow donors, while those that occupy As lattice sites become shallow acceptors. This Amphoteric behavior depends on the growth conditions [8, 9]. Figure 3.10 shows the measured ionization energies for various impurities in GaAs.

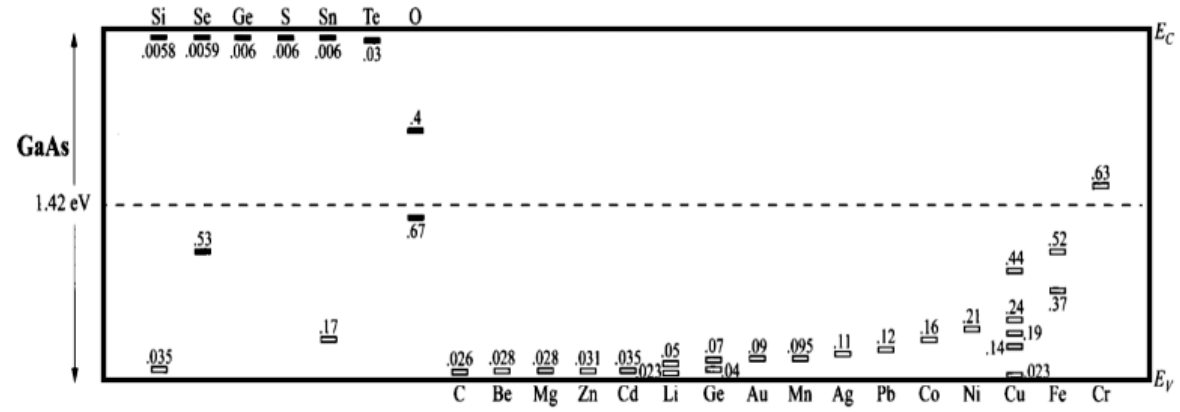


Figure 3.10: Measured ionization energies for varies impurities in Si. Levels below the gap centre are measured from E_V, Levels above the gap centre are measured from E_C, Solid bars represent donor levels and hollow boxes represent acceptor levels [1].

3.3.3. Deep defects

Unlike the shallow defect, the deep defect microscopic origin can be intrinsic or extrinsic defect; even in some cases the microscopic origin cannot be determined. Due to the difficulty of linking the deep level to its origin a few methods can be used, include theoretical modelling of defects and correlation with experimental results, paramagnetic hyperfine interactions [67].

While some defect origin still unknown (the DX-centre which is linked to a donor and another unknown defect [68]) a lot of deep levels has been linked to their responsible defects, such as vacancies in compound semiconductor. For example, Gallium vacancy in GaAs (V_{Ga}) creates four broken bonds pointing out from the four Arsenic atoms towards the V_{Ga} which is considered as a deep level [69]. Vice versa, The V_{As} also can act as a deep defect [70]. Furthermore; the local relaxation of atoms around the vacancy causes initially degenerate levels to split. This effect is called the static Jahn–Teller effect [71, 72]. In short, a deep level may be related to either a chemical impurity or physical defect.

Generally, due to the larger distance to the band edges, deep levels are not efficient at providing free electrons or holes. Quite the opposite, they rather capture free carriers, and behave as a carrier traps or generation-recombination centres. The difference between traps and G-R centres is mainly attributed to their different interactions rates with both bands: if a carrier reemitted to the band it comes from, the deep level is considered as a trap. But, if another carrier of opposite type gets captured on the same level before the first is reemitted, the two carriers will recombine, and then this level is considered as a recombination centre.

Deep levels play an important role in semiconductors whether they are traps or recombination centres. As traps they can capture free carriers supplied by shallow levels, thus compensating them and reducing the effective doping density, which lead to a reduction of conductivity. This can be detrimental in some devices, as it can be beneficial in the case of very high levels of compensation, where the material takes on intrinsic-like properties; a good example of this is the semi-insulating GaAs, which is used as a substrate for devices and integrated circuits. As recombination centres, deep levels may also be beneficial or detrimental. An example of the desirable effects, the capture of electrons (or holes) through the deep level into the valence band (or conduction band) leads generally to nonradiative recombination, which considered as a non-desirable effect for LEDs and lasers [50, 56]. On the other hand, the Gold centre in Silicon acts as a life time killer since it reduces the free carrier life-time which gives fast recombination and, hence, increases the switching frequency (switchers) [66] and gives fast time response (photodetectors) [56].

- **Definitions**

The deep level behaviour depends on its capability to capture an electron or hole (capture rate) or emit them (emission rate), which are not constant. This gives rise to different definitions and names of deep levels. To avoid this confusion, the definitions given by Miller et al. will be adopted here [66]. This method defines the deep levels based on their location, a trap or a recombination centre is defined in terms of capture rates in a neutral region of a semiconductor and in terms of thermal emission rates in depletion region of p-n junction or Schottky barrier.

First in a neutral semiconductor, a deep level is called a recombination centre if the capture rates for electrons and holes are large and comparable (the same range). A deep level is referred to as an electron trap when its capture rate for electrons is much bigger than its capture rate for holes, that is $c_n \gg c_p$. Vice versa, the hole trap is a deep level for which $c_p \gg c_n$.

In depletion region where the density of electrons and holes (n and p) is very small (tend relatively towards zero), it is not useful to talk about capture. Instead the thermal emission process will dominate. If a deep level has a comparable (and large) emission rates for electrons and holes then it is referred to as a generation centre (an equivalent to recombination centre in neutral region). For traps, it is also useful to differentiate between majority and minority traps. A majority trap is a trap which has a thermal emission rate for majority carriers much larger than it has for minority carriers. So an electron trap for example is a majority trap in an n-type semiconductor and a minority trap in a p-type semiconductor. These definitions are summarised in Figure 3.11. Last, it is worth to mention that electron traps are also called donor traps, and hole traps are called acceptor traps.

Since the occupation of traps is controlled by the Fermi level, it is useful to clarify the charge state of electron and hole traps corresponding to their position with respect to the Fermi level. Again the definitions of Miller et al are adopted here. An electron trap is full (of electrons) and therefore neutral when it is below the electron quasi-Fermi level (E_{fn}), and it is empty (of electrons) and therefore positively charged when it is above E_{fn}. A hole trap is full (of holes) and therefore is neutral when it is above the hole quasi-Fermi level (E_{fp}) and it is empty (of holes) and therefore negatively charged when it is below E_{fp}.

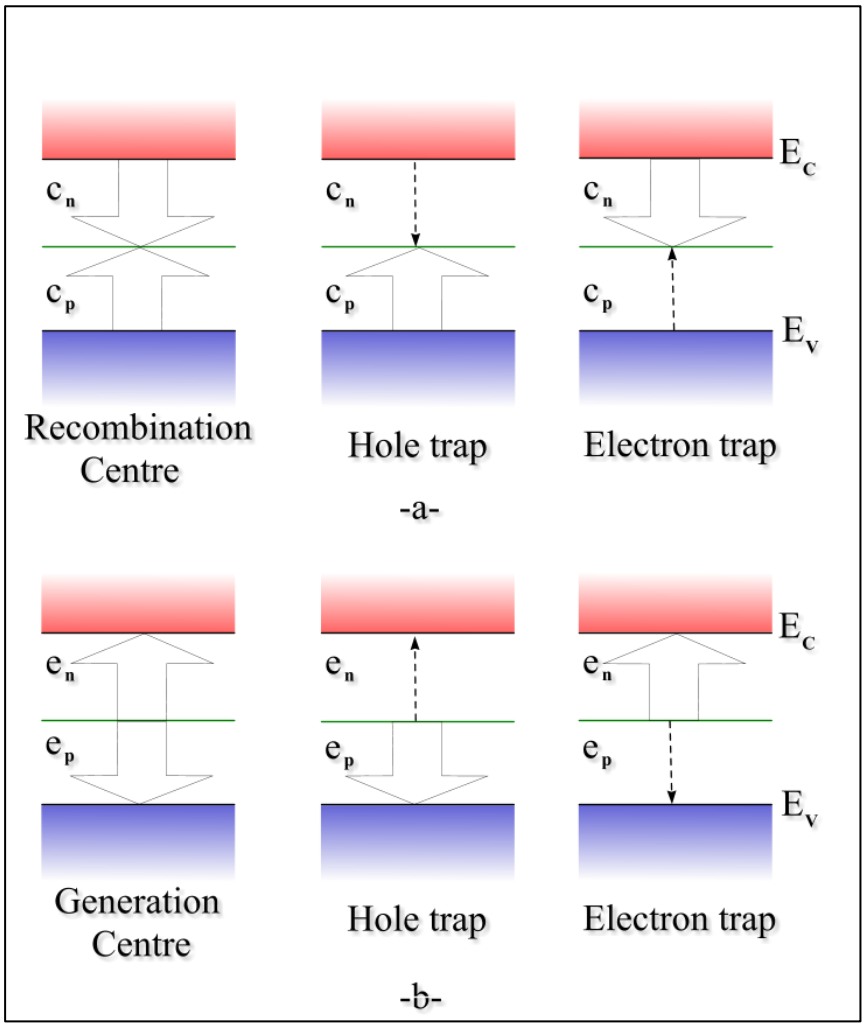


Figure 3.11: Definition of the terms (electron trap) and (hole trap) and (generation-recombination centre) by means of the relative magnitudes of the capture and emission rates by the width of the arrows. -a- in neutral region, -b- in depletion region.

3.3.4. Generation-Recombination statistics

Electron transitions occur in the presence of traps within the forbidden gap of the semiconductor. This is essentially a two-step process, the theory of which was first derived by Shockley and Read [73] and then by Hall [74]. Therefore these deep levels are referred usually to as Shockley-Read-Hall (SRH) centres. There are four basic processes involved in the carrier generation recombination at a trap. These are electron capture, electron emission, hole capture and hole emission, these are labelled a, b, c and d respectively in Figure 3.12. These processes could be due to a thermal or optical process, only thermal process will be taken into account since no optical methods were used in this work.

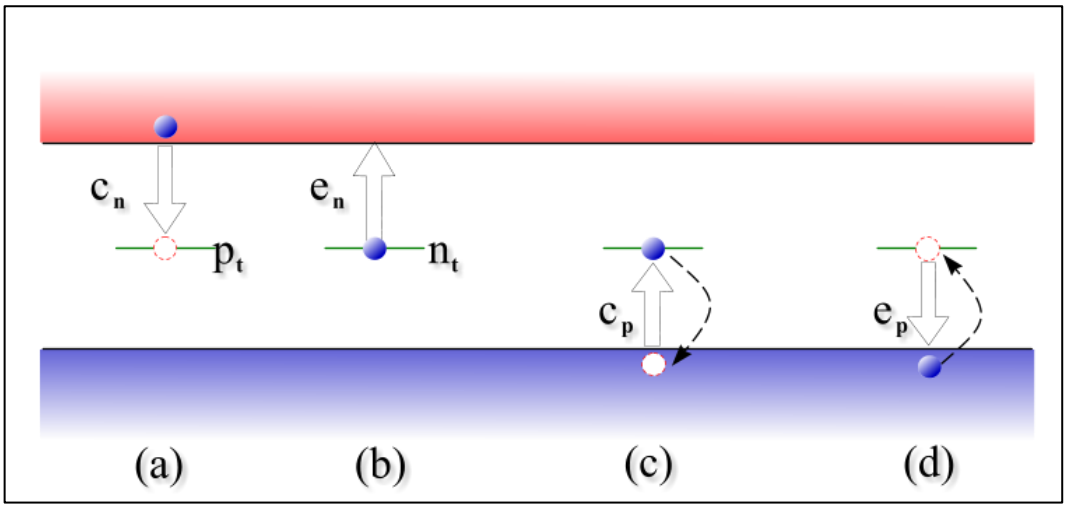


Figure 3.12: The four carriers' transition processes. a- electron capture, b- electron emission, c- hole capture and d- hole emission.

3.3.4.1. Capture and emission rates

We consider electron traps (see **Figure 3.12**) with a concentration N_t with an energy level E_t. In thermodynamic equilibrium they have an electron population probability equals:

$$f_t = \frac{1}{1+\exp(\frac{E_t - E_F}{KT})} \tag{3.4}$$

Where f_t is the nonequilibrium population of the trap.

A G-R centre can exist in one of two states. When occupied by an electron, it is in the n_t state and when occupied by a hole, it is in the p_t state (both shown in Figure 3.12). Only the unoccupied traps can capture electrons from the conduction band. Thus, the capture process (a) in Figure 3.12 is proportional to the unoccupied traps and the electron concentration.

$$(a) = c_n . n . p_t = v_{th} . \sigma_n . n . N_t (1 - f_t) \tag{3.5}$$

Where n is the free electron density, v_{th} is the thermal velocity ($v_{th} = \sqrt{3KT/m^*}$), σ_n is the capture cross section which a measure of how to the centre the free carrier has to come to get captured. In other words, we merely assume that the defect has a sphere of influence and ascribe it a cross-sectional area so that any carrier intercepting that area will be captured[75]. c_n is the capture coefficient and it is defined by:

$$c_n = v_{th} . \sigma_n \tag{3.6}$$

The emission process (b) is defined as the multiplication of the emission rates (e_n) and the occupied traps density:

$$(b) = e_n . n_t = e_n . N_t f_t \tag{3.7}$$

In thermodynamic equilibrium, capture and generation rates are equal (i.e. $(a) = (b)$). Thus, the emission probability is equal to:

$$e_n = v_{th} . \sigma_n . n_0 . \frac{1 - f_t^0}{f_t^0} \tag{3.8}$$

Where:

$$\frac{1 - f_t^0}{f_t^0} = \exp(\frac{E_t - E_F}{KT}) \tag{3.9}$$

Using (3.9) the emission rate can be written as:

$$e_n = v_{th} . \sigma_n . N_c . \exp\left(\frac{E_t - E_c}{KT}\right) \tag{3.10}$$

The emission rate can be written in a more useful form in terms of temperature. Usually, the temperature dependence of the thermal velocity is $v_{th} \alpha T^{1/2}$, and the temperature dependence of the band-edge density of states is $N_c \alpha T^{3/2}$. Therefore, the temperature dependence of the emission rate is:

$$e_n = \gamma_n . \sigma_n . T^2 . \exp\left(\frac{E_t - E_c}{KT}\right) \tag{3.11}$$

A similar equation can be obtained for holes, thus:

$$e_p = \gamma_p . \sigma_p . T^2 . \exp\left(\frac{E_V - E_t}{KT}\right) \tag{3.12}$$

Where γ_n and γ_p are constants independent of temperature. In GaAs, for example, $\gamma_n \approx 2.28\ 10^{20} cm^{-2} s^{-1} K^{-2}$ and $\gamma_p \approx 1.7\ 10^{21} cm^{-2} s^{-1} K^{-2}$ [66].

3.3.4.2. Ionized traps density

The density of G-R centres occupied by electrons n_t and holes p_t must equal the total density N_t:

$$N_t = n_t + p_t \tag{3.13}$$

In other words, a centre is either occupied by an electron or a hole. When electrons and holes recombine or are generated, the electron density in the conduction band n, the hole density in the valence band p, and the charge state of the centre n_t or p_t are all functions of time. The electron density in the conduction band is diminished by electron capture (process (a)) and increased by electron emission (process (b)) and the electron time rate of change due to G-R mechanisms is given by [66]:

$$-\frac{dn}{dt} = (a) - (b) = c_n.n.p_t - e_n n_t \tag{3.14}$$

For holes we find the parallel expression:

$$-\frac{dp}{dt} = (d) - (c) = c_p.p.n_t - e_p p_t \tag{3.15}$$

Whenever an electron or hole is captured or emitted, the traps occupancy changes. By combining (3.14) and (3.15) and making use of (3.13) we obtain the rate of change of traps occupied by electrons, thus:

$$\begin{aligned}\frac{dn_t}{dt} &= (a) - (b) + (c) - (d)\\ &= c_n.n.p_t - e_n n_t + e_p p_t - c_p.p.n_t\\ &= \left(c_n.n + e_p\right)p_t - (c_p.p + e_n)n_t\\ &= (c_n.n + e_p)(N_t - n_t) - (c_p.p + e_n)n_t\\ &= \left(c_n.n + e_p\right)N_t - (c_n.n + c_p.p + e_n + e_p)n_t\\ &= \left[\frac{c_n.n+e_p}{c_n.n+c_p.p+e_n+e_p}N_t - n_t\right](c_n.n + c_p.p + e_n + e_p)\end{aligned} \tag{3.16}$$

Therefore:

$$\frac{dn_t}{n_t+C_1N_t} = -(c_n.n + c_p.p + e_n + e_p)dt \tag{3.17}$$

Where:

$$C_1 = \frac{c_n.n+e_p}{c_n.n+c_p.p+e_n+e_p} \tag{3.18}$$

This equation is non-linear, with n and p being time dependent variables. If the equation can be linearized, it can be solved easily. Two cases allow this simplification: in a reverse-biased space-charge region or in the quasi-neutral regions. Thus, the solution in both cases is given by [76]:

$$n_t(t) = n_t(0)\exp\left(-\frac{t}{\tau}\right) + \frac{(c_n.n+e_p)N_t}{c_n.n+c_p.p+e_n+e_p}\left[1-\exp\left(-\frac{t}{\tau}\right)\right] \quad (3.19)$$

Where $n_t(0)$ is the density of traps occupied by electrons at $t = 0$, and τ is the decay time constant:

$$\tau = \frac{1}{c_n.n+c_p.p+e_n+e_p} \quad (3.20)$$

the steady-state density as $t \to \infty$ is:

$$n_t = \frac{(c_n.n+e_p)}{c_n.n+c_p.p+e_n+e_p} N_t \quad (3.21)$$

Equation (3.21) shows the steady-state occupancy of n_t to be determined by the electron and hole densities as well as by the emission and capture rates. Equations (3.19) and (3.21) are the basis for most deep-level impurity measurements.

Equation (3.19) can be simplified in some special cases, taking as an example an n-type semiconductor where p can be neglected, and the trap is in the upper half of the band gap with $e_n \gg e_p$ allowing e_p to be neglected. In this case the time constant of (3.20) is reduced to:

$$\tau \approx \frac{1}{c_n.n+e_n} \quad (3.22)$$

A more useful parameter than n_t is introduced, namely the ionised electron trap density N_t^+. In this case, we can distinguish two cases:

1. The first case corresponds to emission in depletion region, where the traps are initially full. Therefore $n \to 0$, $n_t(0) = N_t$ and the emission process dominates the capture process. In this case the time constant is reduced to:

$$\tau \approx \tau_e = \frac{1}{e_n} \quad (3.23)$$

and :

$$n_t(t) = N_t\exp\left(-\frac{t}{\tau}\right) \quad (3.24)$$

and:

$$N_t^+ = N_t - n_t(t) = N_t\left[1-\exp\left(-\frac{t}{\tau}\right)\right] \quad (3.25)$$

2. The second case corresponds to capture in neutral region, where the traps are initially empty. Therefore, $n_t(0) = 0$ and the capture process dominates the emission process. In this case the time constant is reduced to:

$$\tau \approx \tau_e = \frac{1}{c_n.n} \tag{3.26}$$

and :

$$n_t(t) = N_t\left[1 - \exp\left(-\frac{t}{\tau}\right)\right] \tag{3.27}$$

and:

$$\begin{aligned} N_t^+ &= N_t - n_t(t) \\ &= N_t \exp\left(-\frac{t}{\tau}\right) \end{aligned} \tag{3.28}$$

Similar equations can be obtained for a hole trap by replacing the appropriate parameters (N_t^+ *by* N_t^-, n by p, $e_n$by e_p and c_n by c_p).

3.3.4.3. Shockley-Read-Hall Recombination

The net rate of electron capture is defined as the difference between the captured electrons (process a) and the emitted electrons (process b)

$$R_n = (a) - (b)$$

$$= v_{th}.\sigma_n.n.N_t(1 - f_t) - e_n.N_t f_t$$

$$= v_{th}.\sigma_n.n.N_t(1 - f_t) - v_{th}.\sigma_n.N_c.\exp\left(\frac{E_t - E_c}{KT}\right).N_t f_t$$

$$\Longrightarrow R_n = v_{th}.\sigma_n.N_t[n.(1 - f_t) - n_1.f_t] \tag{3.29}$$

Where

$$n_1 = N_c.\exp\left(\frac{E_t - E_c}{KT}\right) \tag{3.30}$$

The net rate of hole capture by the trap levels may also be calculated similarly and expressed as:

$$R_p = v_{th}.\sigma_p.N_t[p.f_t - p_1.(1 - f_t)] \tag{3.31}$$

Where

$$p_1 = N_c.\exp\left(\frac{E_t - E_c}{KT}\right) \tag{3.32}$$

Carrier recombination begins whenever there is a departure from the condition of thermal equilibrium. Since, electron hole recombination occurs in pairs, the net rate of recombination is:

$$R = R_n = R_p \tag{3.33}$$

$$\Longrightarrow v_{th}.\sigma_n.N_t[n.(1-f_t) - n_1.f_t] = v_{th}.\sigma_p.N_t[p.f_t - p_1.(1-f_t)]$$

$$\Longrightarrow \sigma_n.n - \sigma_n.n.f_t - \sigma_n.n_1.f_t = \sigma_p.p.f_t - \sigma_p.p_1 + \sigma_p.p_1.f_t$$

$$\Longrightarrow \sigma_n.n + \sigma_p.p_1 = (\sigma_n.n + \sigma_n.n_1 + \sigma_p.p + \sigma_p.p_1)f_t$$

we obtain the population function in non-equilibrium:

$$f_t = \frac{\sigma_n.n + \sigma_p.p_1}{\sigma_n(n+n_1) + \sigma_p(p+p_1)} \tag{3.34}$$

The net recombination rate (R_{SRH}) is calculated by substituting (3.34) in (3.29) or (3.31), thus:

$$R = v_{th}.\sigma_n.N_t\left[n.\left(1 - \frac{\sigma_n.n + \sigma_p.p_1}{\sigma_n(n+n_1) + \sigma_p(p+p_1)}\right) - n_1.\frac{\sigma_n.n + \sigma_p.p_1}{\sigma_n(n+n_1) + \sigma_p(p+p_1)}\right]$$

$$= v_{th}.\sigma_n.N_t\left(\frac{\overbrace{\sigma_n.n^2}^{1} + \overbrace{n.\sigma_n.n_1}^{2} + n.\sigma_p.p + \overbrace{n.\sigma_p.p_1}^{3} - \overbrace{\sigma_n.n^2}^{1} - \overbrace{n.\sigma_p.p_1}^{3} - \overbrace{n_1.\sigma_n.n}^{2} - n_1.\sigma_p.p_1}{\sigma_n(n+n_1) + \sigma_p(p+p_1)}\right)$$

$$= v_{th}.\sigma_n.N_t\left(\frac{n.\sigma_p.p - n_1.\sigma_p.p_1}{\sigma_n(n+n_1) + \sigma_p(p+p_1)}\right)$$

$$\Rightarrow R = \frac{v_{th}.\sigma_n.\sigma_p.N_t}{\sigma_n(n+n_1) + \sigma_p(p+p_1)}(n.p - n_1.p_1) \tag{3.35}$$

Since $n_1.p_1 = n_i^2$, (3.35) can be written using (3.30), (3.32) as:

$$R_{SRH} = \frac{v_{th}.\sigma_n.\sigma_p.N_t.(n.p - n_i^2)}{\sigma_n\left(n + n_i\exp\left(\frac{E_t - E_i}{KT}\right)\right) + \sigma_p\left(p + n_i\exp\left(-\frac{E_t - E_i}{KT}\right)\right)} \tag{3.36}$$

3.4. Defects effect on capacitance

As defined in the previous chapter (2.6.3) the capacitance has a direct relationship with the charge density stored in the space charge region which can be affected by the presence of deep levels. With electrons or holes emitted or captured by traps, the charge density (Q) given by (2.42) will change to:

$$Q(V) = \sqrt{2q\epsilon_s N_{scr}(V_{bi} - V_{ext} - \frac{KT}{q})} \tag{3.37}$$

Therefore, the capacitance equals:

$$C = \sqrt{\frac{q\epsilon_s |N_{scr}|}{2\left(V_{bi} \pm V_{ext} - \frac{KT}{q}\right)}} \tag{3.38}$$

N_{scr} is the ionized impurity density in the space-charge region. It depends on the type of shallow (donors or acceptors) and deep levels (electron or hole trap) in the same time. In the case of shallow levels being donors (which have a positive charge in the space charge region) we can distinguish four cases:

- In presence of deep level hole traps that are negatively charged when occupied by electrons:

$$N_{scr} = N_D^+ - N_t^- \tag{3.39}$$

- In presence of deep level hole traps that are neutral when occupied by holes:

$$N_{scr} = N_D^+ \tag{3.40}$$

- In presence of deep level electron traps that are neutral when occupied by electrons:

$$N_{scr} = N_D^+ \tag{3.41}$$

- In presence of deep level electron traps that are positively charged when occupied by holes:

$$N_{scr} = N_D^+ + N_t^+ \tag{3.42}$$

Similar four equations can be obtained for shallow level acceptors by replacing N_D^+ by $(-N_A^-)$.

Finally, a general capacitance formula can be written as follow:

$$C = \sqrt{\frac{q\epsilon_s \left|N_{A,D}^{\pm} + N_t^{\pm}\right|}{2\left(V_{bi} \pm V_{ext} - \frac{KT}{q}\right)}} \tag{3.43}$$

The capacitance formula can also be simplified to:

$$C = \sqrt{\frac{q\epsilon_s \left| N_{A,D}^{\pm} + N_t^{\pm} \right|}{2\left(V_{bi} \pm V_{ext} - \frac{KT}{q}\right)}}$$

$$C = \sqrt{\frac{q\epsilon_s}{2\left(V_{bi} \pm V_{ext} - \frac{KT}{q}\right)}} * \sqrt{\left| N_{A,D}^{\pm} + N_t^{\pm} \right|}$$

$$C = \sqrt{\frac{q\epsilon_s (\pm N_{A,D}^{\pm})}{2\left(V_{bi} \pm V_{ext} - \frac{KT}{q}\right)}} * \sqrt{1 + \frac{\pm N_t^{\pm}}{\pm N_{A,D}^{\pm}}}$$

$$C = C_0 \sqrt{1 + \frac{\pm N_t^{\pm}}{\pm N_{A,D}^{\pm}}} \qquad (3.44)$$

Where C_0 is the capacitance of a device with no deep level impurities. It is clear that the sign $(+)$ inside the square root depends on the type of shallow and deep levels; if the two levels are the same type, the sign does not change. While, if the two levels are of different types, the sign changes to $(-)$. Thus, it is more useful to talk about majority or minority traps. It is worth to mention that the capacitance is proportional to time. The time dependence of N_t^+ or N_t^- reflects the time dependence of capacitance. This dependence can be demonstrated by replacing $N_t^{\pm}$ in the capacitance formula (3.38) by its values, as follow:

The first case corresponds to emptying traps from majority carriers therefore the capacitance equals to:

$$C = C_0 \sqrt{1 + \frac{\pm N_t}{\pm N_{A,D}^{\pm}} \left[1 - \exp\left(-\frac{t}{\tau}\right)\right]} \qquad (3.45)$$

The second case corresponds to filling traps with majority carriers therefore the capacitance equals to:

$$C = C_0 \sqrt{1 + \frac{\pm N_t}{\pm N_{A,D}^{\pm}} \exp\left(-\frac{t}{\tau}\right)} \qquad (3.46)$$

3.5. Techniques for the characterisation of deep levels

The characterisation of deep levels require evaluation of their activation energy, emission and capture rates for electrons and holes and their density. Since the emission and capture coefficients (e_n and c_n) are proportional to the capture cross section (σ_n), as described above, then it is a common practice to evaluate σ_n instead of e_n and c_n. Since the deep level defects are electrically active, a lot of electrical characteristics are used to investigate their properties. The investigation of deep level defects has traditionally been undertaken of bulk states confined to space charge region as in a p-n junction or Schottky barrier (i.e. Carrier emission and capture by deep levels has been most easily observed by the change in charge state when monitoring capacitance).

In spite of the emergence of the transient related methods as the leading tool in characterizing deep levels, some steady state related methods are still very useful such as Thermally Stimulated Current (TSC), Thermally Stimulated Capacitance (TSCAP). In these techniques, the traps are initially filled at low temperatures. Then the temperature is increased and the capacitance (or current) is measured. A maximum occurs corresponding to emission from traps. The drawbacks of these techniques include the uncertainty in the activation energies and the difficulty in evaluating the emission rates [66].

The admittance spectroscopy in which the junction admittance is measured as a function of temperature is limited to majority traps only. Photo-capacitance is a powerful technique but it requires lengthy analysis and is limited to traps deeper than 0.3 eV [66]. The most widely used modification of transient techniques is deep level transient spectroscopy (DLTS) introduced by Lang [4] and other techniques related to it.

Chapter 4

Device simulation by SILVACO

4.1. Introduction

Simulation is a powerful tool used to reproduce mathematically the operation of devices and systems. It can be considered as a developed analytic method; it is usually used when the analytic methods do not adequately represent the system being studied. For example, in some situations, the objective function is nonlinear; some of the restrictions cannot be modelled by a set of linear equations. In other cases, the simplifications adopted in the analytic methods have a significant effect on the results. Simulation also plays a main role in the development and prediction of the properties of modern technologies. Because of trial manufacturing and circuit redesign, the cost of modern technologies (integrated circuits for example) is very high, which can be easily lowered using simulation. In addition, the simulation allows visualization and better understanding of the microscopic physical phenomenon and effects taking place over very small lengths or over small periods in macroscopic dimensions. So, the goal of the device simulation is to use the simulation output for predictive analysis of the properties and behaviour of the simulated device structure with a unique insight into the internal process and structure operation, along with the possibility of further optimization and development.

In simulation, the semiconductor device is represented by a structure whose electrical and physical properties are discretized onto a mesh of nodes containing information about types of materials, doping profiles in specific regions, and boundaries conditions. An extensive set of physical models is also supplied to characterize the device physical behaviours. A device simulator calculates the output characteristics by solving a set of partial differential equations through iterative numerical techniques.

In this chapter, the numerical simulator SILVACO TCAD (used in this study) will be presented. We will first give an overview of the software. Then we will shed light on the structure creation using ATHENA. Finally, we will explain how to simulate the electric

behaviour using ATLAS. In order to clarify the details, a simple example of a Schottky junction will be simulated. An example code is presented in appendix A.

4.2. SILVACO overview

Since its founding in 1984 by Dr. Ivan Pesic [77], SILVACO has grown to become the most important semiconductor device simulator. SILVACO TCAD is the abbreviation of Silicon Valley Corporation Technology Computer Aided Design. It is a semiconductor process simulation package which consists of several physically based simulators (ATHENA, ATLAS, MERCURY, SSUPREM3 … etc.) gathered under one environment called DECKBUILD. Each of them simulates different processes. Due to the large number of SILVACO's modules and their complexity, only the modules used in this work (see Figure 4.1) will be presented:

- **DECKBUILD:** is an interactive, graphic runtime environment for developing process and device simulation input decks. It is considered as the main window of SILVACO where all simulators can be controlled.
- **ATHENA:** is a physically based process simulator module which predicts the structures that result from specified process sequences. This is done by solving systems of equations that describe the physics and chemistry of semiconductor processes. It provides a platform for simulating diffusion, deposition, etching, ion implantation, oxidation, lithography of semiconductor materials. Costly wafer experiments can be replaced with simulations using ATHENA.
- **ATLAS:** is a physically based device simulator module which predicts the electrical characteristics that are associated with specified physical structures and bias conditions. This is achieved by approximating the operation of a device onto a grid (discretizing). The transport of carriers through this device can be simulated by applying a set of differential equations, derived from Maxwell's laws onto this grid. This means that ATLAS provides a platform to analyse AC, DC and time domain responses for all semiconductor based technologies in two and three dimensions.
- **TONYPLOT:** is a visualization tool which plots the results obtained from simulation. It provides scientific visualization capabilities including xy plots with linear and logarithmic axes, polar plots, surface and contour plots.

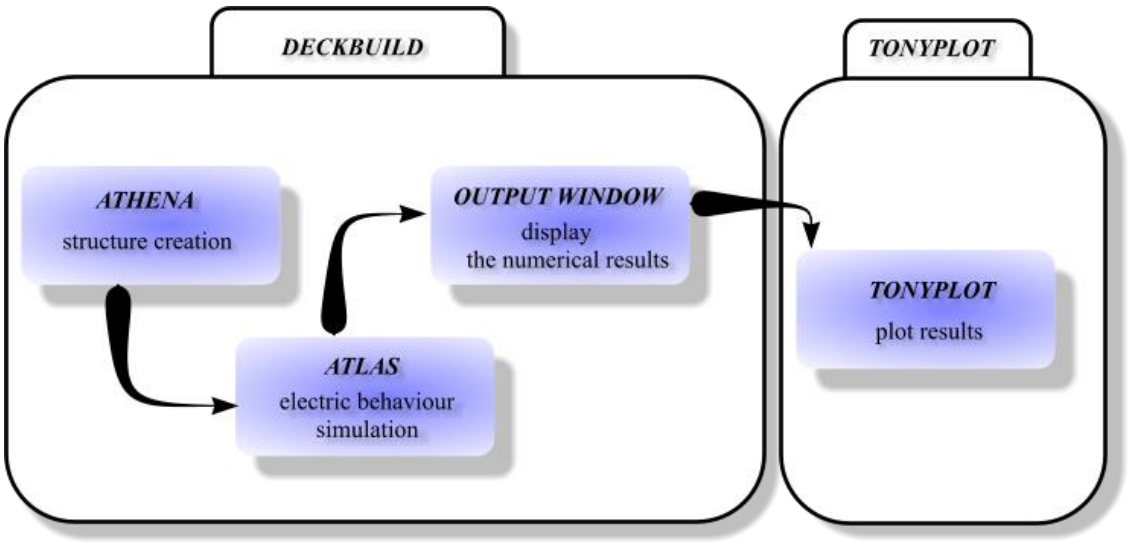


Figure 4.1: The main modules in SILVACO.

4.3. DECKBUILD

It is the graphic interface between the user and simulators. It consists of two windows; one for input deck creation and editing, in this window the simulators can be called and controlled using DECKBUILD commands. The second window is for simulators outputs and results (see Figure 4.2).

DECKBUILD provides a diverse set of controls over the running simulation, and here are some of used controls:

- Calling a simulator:

  This can be done using the "Go" statement, which tells DECKBUILD to shut down the current simulator and start up the specified simulator. Then any statement of the called simulator can be executed (e.g. Go ATLAS)
- Variable declaration:

  The statement "Set" is used to declare variables' names and values (e.g. Set T=300). The variable's value can be used later by preceding its name with a dollar sign "$" (e.g. Set a=$T, in this case "a" will take the value of "T" thus a=300).
- Looping commands:

  In DECKBUILD, a group of statements can be executed many times using the "loop" command, which specifies the start point for looping, followed by the number of repetitions "steps". The end point can be defined by "l.end". The following example demonstrates how to write a loop command:

```
loop steps=10
….
….
l.end
```

- Finishing command line:

  In the end of the deck, the opened simulators must be closed using the "quit" statement.

An example of DECKBUILD window is shown in Figure 4.2.

Note:

Comments in DECKBUILD must be preceded by "#". So any statement preceded by "#" will not be executed.

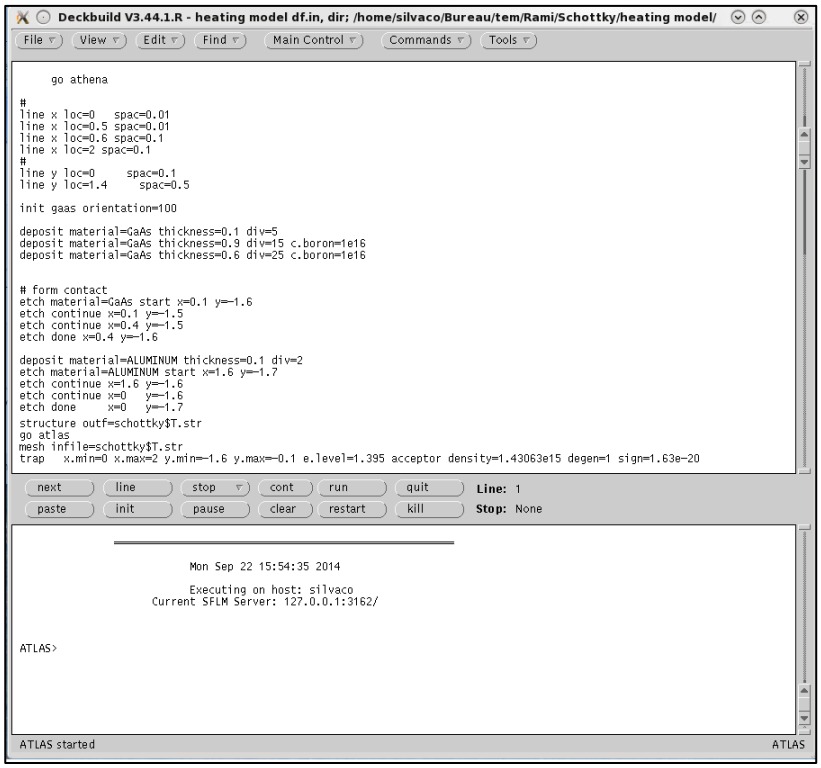


Figure 4.2: DECKBUILD main window.

4.4. DEVICE GENERATION (ATHENA)

ATHENA performs structure initialization and manipulation, and provides basic deposition and etching facilities. Thus, it can be considered as a virtual laboratory where the simulation steps are similar to the real device manufacturing. It starts by defining the initial geometry of the structure to be simulated (substrate) by creating the mesh grid and defining the materials.

Thereafter, deposing the layers one by one by setting the sequence of process steps that are to be simulated (e.g. implantation, etching, diffusion, exposure ... etc.). Finally, the structure process finishes by defining the electrodes and save the structure file.

4.4.1. Substrate

A mesh refers to a collection of elements whose union defines the device (see Figure 4.3.a). It is established by overlapping two sets of parallel lines perpendicular to each other to form a network which has the device shape. The intersections of lines are called nodes, while the spaces between them called elements. Accurate simulation requires a smooth mesh that can resolve all significant requirements of the solution. Numerical efficiency requires a rough mesh that minimizes the total number of grid points thus a fast simulation. Another condition must be taken in consideration is the maximum number of nodes supported by the software; in SILVACO TCAD (ATLAS), a two-dimensional simulations may have up to 20,000 nodes. Three-dimensional simulations may have up to 200,000 nodes and 400,000 elements, with no more than 20,000 in a single plane and a maximum of 200 planes in the z direction [78].

Many distributions are possible for the mesh; some distributions yield much better results than others. Till these days, the mesh generation is still an inaccurate science [78]. However, the following features could give a good mesh:

- Generate enough elements to provide the required accuracy.
- Do not generate unnecessary elements that impair accuracy.
- Generate smooth mesh in critical areas (such as junction, interfaces … etc.) where the required variables (such as n, p… etc.) change quickly in order to prevent information loss.
- Use a rough mesh for non-critical areas.
- avoid generation of narrow elements, which leads to weakened accuracy, convergence, and robustness [78].
- The transition from smooth to rough region must be gradual.

To generate a mesh in ATHENA, three important information must be defined: the direction of the lines (`line x` or `y`) and the locations of the principle lines (`loc`) then the steps between them (`spac`) which explain the distance between secondary lines in micrometre.

Figure 4.3.a shows the substrate's mesh of the considered example which can be generated using the following code:

```
#  x mesh
line x loc=0      spac=0.10
line x loc=0.2    spac=0.01
line x loc=0.8    spac=0.01
line x loc=1.0    spac=0.10
# y mesh
line y loc=0.0    spac=0.1
line y loc=1.2    spac=0.5
```

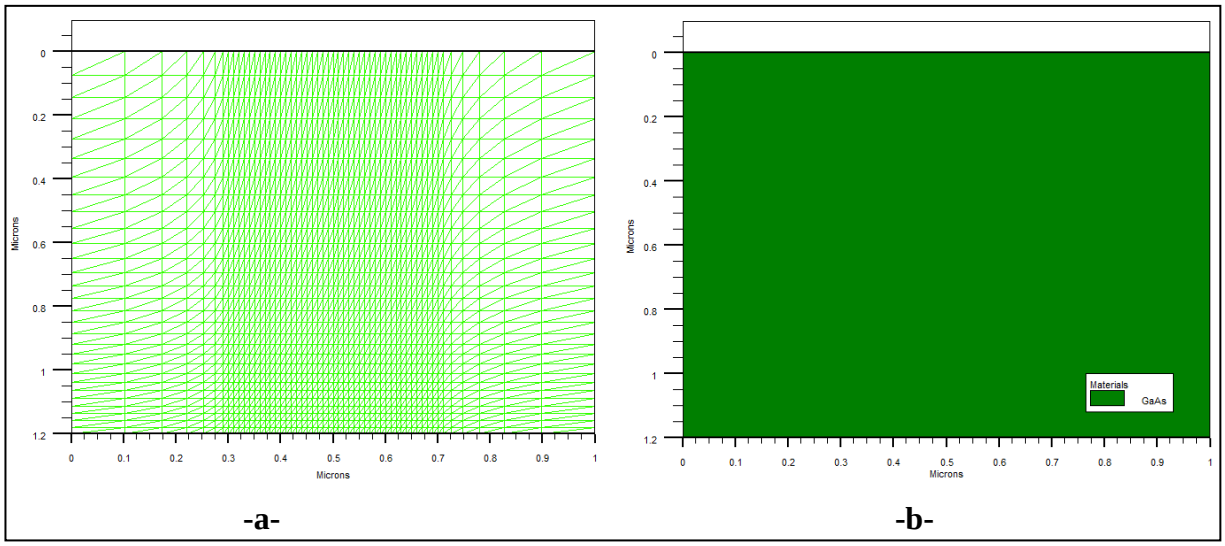


Figure 4.3: Substrate generation: a- Mesh, b- Material.

The next step is the substrate material type definition, which can be done by using the "`init`" statement whose provides a lot of capabilities to describe the substrate, such as: material type (Si, GaAs…etc.), the composition fraction of the ternary or quaternary compound, doping type and density, growth direction (100, 110 …), as shown in the next example where the substrate is made of undoped Gallium Arsenide (to simulate the semi-insulating substrate [79]) grown along the [100] direction (see Figure 4.3.b).

```
init gaas orientation=100 c.boron=1e16
```

4.4.2. Semiconductor deposition

After making the substrate, the other device parts are now ready to be deposited. The deposition step is simulated by the "`deposit`" statement where the material and the thickness of the layer to be deposited must be specified (Figure 4.4.a). Each sub layer is deposited and meshed separately. At this point, the doping type and density can be defined using the "`C.IMPURITY`, `F.IMPURITY`, `C.INTERST`" parameters in the "`DEPOSIT`" statement.

```
deposit material=GaAs thickness=0.8 div=16  c.boron=1e16
```

where "`div`" determines the number of mesh lines which contain each layer.

4.4.3. The electrodes

After creating the substrate and semiconductor layers, the next step is to create contacts on the device. At least one contact must be specified in the script. Due to the metallic nature of the electrodes, a metal must be added to the structure in specific places. Hence, the structure must be prepared for metal deposition according to the following steps:

1. Prepare the semiconductor for the metal deposition using the "`etch`" statement where the quadrilateral to be etched must be specified point to point, as follow:

```
# etching for anode
etch material=GaAs start x=0.7 y=-0.8
etch continue x=0.7 y=-0.7
etch continue x=1.0 y=-0.7
etch done x=1.0 y=-0.8

# etching for cathode
etch material=GaAs start x=0.3 y=-0.8
etch continue x=0.3 y=-0.7
etch continue x=0.0 y=-0.7
etch done x=0.0 y=-0.8
```

   where "x" and "y" in each line specify the vertex of the quadrilateral (see Figure 4.4.b).
2. Deposit the metal layer to form the electrodes using the "`deposit`" statement (Figure 4.4.c).
3. Adjust the structure shape by etching the undesirable parts (Figure 4.4.d).

```
etch material=ALUMINUM start x=1 y=-0.9
etch continue x=1 y=-0.8
```

```
etch continue x=0    y=-0.8
etch done     x=0    y=-0.9
```

4. Declare the metal parts as electrodes by defining their positions and names using the "`electrode`" statement as follow:

```
# set electrodes for ATLAS
electrode name=cathode    x=0.15 y=-0.75
electrode name=anode      x=0.85 y=1.25
```

where "`x`" and "`y`" specify the horizontal and vertical location of the region, which will be defined as an electrode.

5. Once the structure is completely assembled, it must be saved for consequent use by ATLAS using the "`structure`" statement:

```
structure outf=schottky.str
```

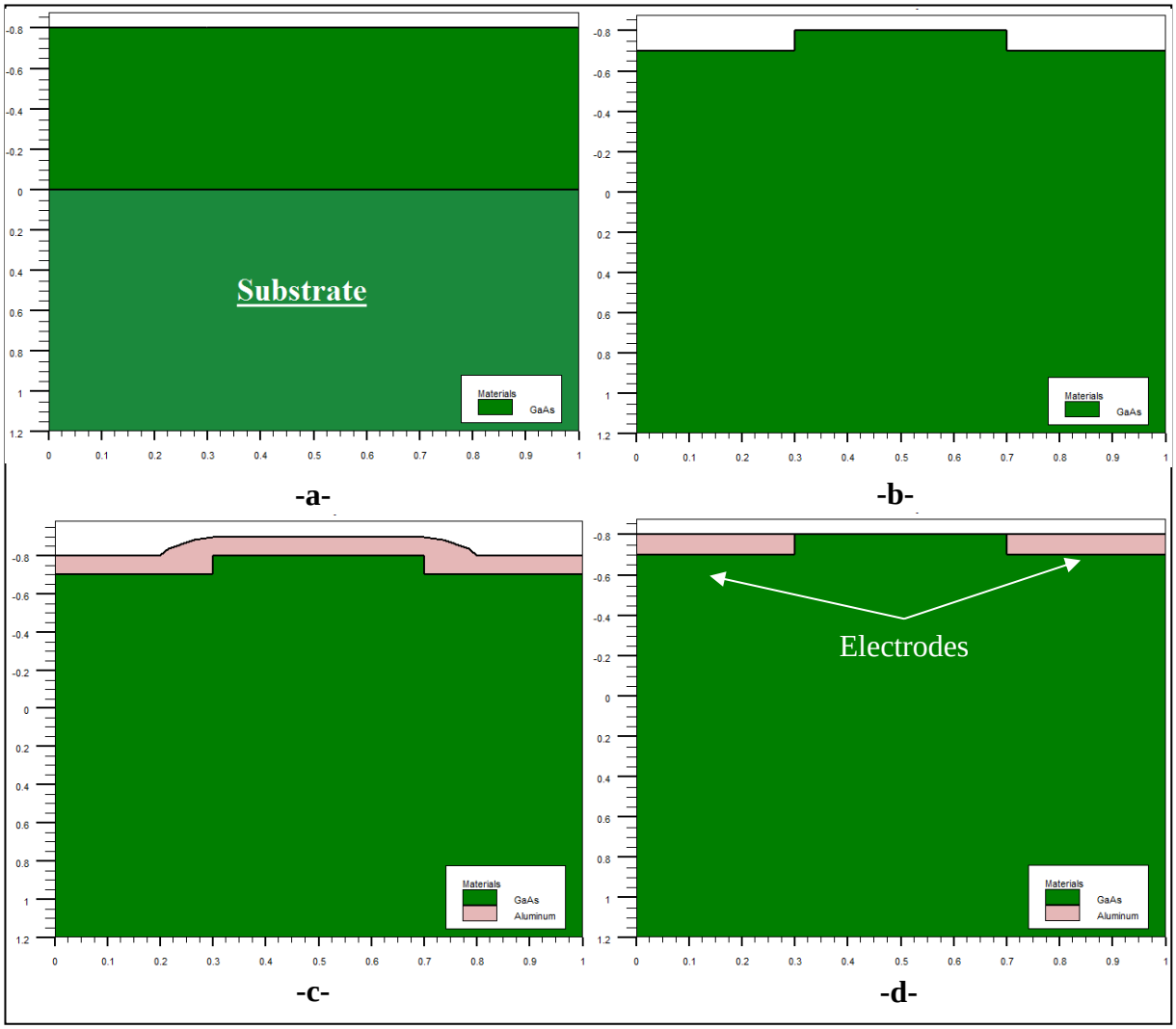


Figure 4.4: Electrodes deposition steps: a- Primary structure. b- Prepared structure for metal deposition. c- Metal deposition. d- Final structure.

Finally, we obtain a virtual structure of a Schottky junction which has dimensions of 2 µm width, 3 µm length, composed from: 1.2 µm GaAs substrate followed by 1.5 µm GaAs doped p-type with density of $1*10^{16}$ cm^{-3}, and two contacts as it is shown in the Figure 4.5.a and b.

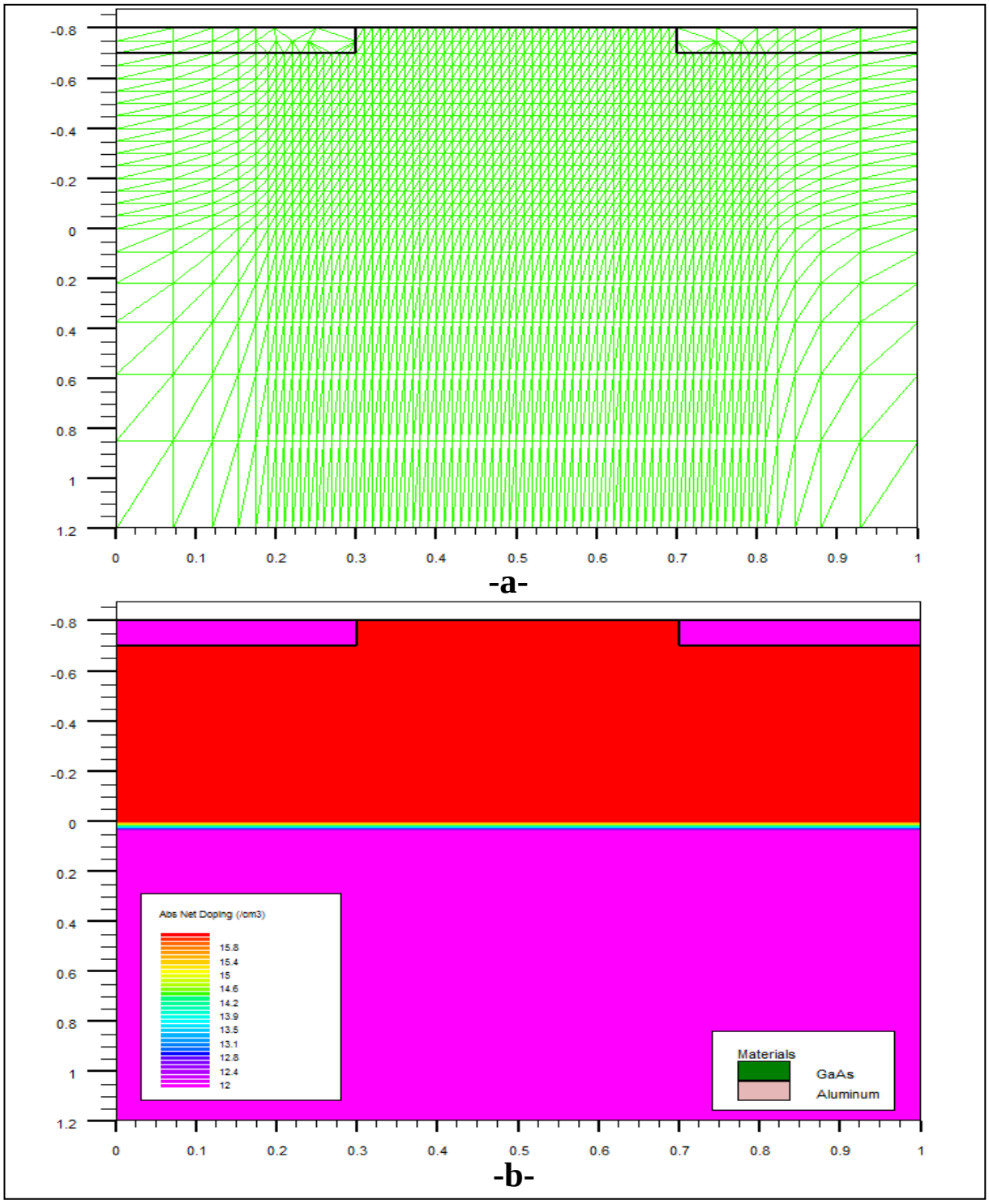


Figure 4.5: Final structure: a- Structure mesh. b- Dopants density.

4.5. Device's electrical properties specification

ATHENA is a physically based process simulator module which can only predicts the structure. Therefore, to simulate the electrical behaviour another SILVACO's module will be used here which is ATLAS. Unlike ATHENA, ATLAS is a physically based device simulator module which predicts the electrical characteristics that are associated with specified physical structures.

Each ATLAS statement is composed of a keyword and a set of parameters. The format is as follows:

```
<STATEMENT> <PARAMETER>=<VALUE>
```

While the statement is the main command (such as `Mesh`, `trap`, `doping`, `models`, `method`, `solve` … etc.), the parameters are used to control and add more specifications about the statement. The parameters can be classified into four groups: real, integer, character, and logical. The logical parameters (such as `UNIFORM`, `gauss` …etc.) can have only values of 'true' or 'false'. ATLAS has a specific default values to a logical parameter unless otherwise instructed. The integer parameters (such as `REGION`, `evsatmod` ... etc.) can only take on integer values. The real parameters (such as `density`, `e.level`, `vstep` … etc.) can take floating point numbers as input values. Last, the character parameters (such as `OUTFILE`, `name` … etc.) can take strings as an input.

The order in which statements occur in an ATLAS input file is important. A standardized structure to follow is outlined in Table 4.1.

Order	Steps	Statements
1	Structure specification (using ATLAS or import it from ATHENA)	MESH INFILE (import structure), MESH, REGION, ELECTRODE, DOPING
2	Material Models Specification	MATERIAL, MODELS, CONTACT, INTERFACE
3	Numerical Method Selection	METHOD
4	Solution Specification	LOG, SOLVE, LOAD, SAVE
5	Results Analysis	EXTRACT, TONYPLOT

Table 4.1: ATLAS statements order with examples of each step.

4.5.1. Structure electrical properties

The device now is almost ready for simulation, except some electrical properties that can be added using ATLAS, such as introducing different traps distributions to the structure or defining the contacts as either Schottky or Ohmic, or even some optical properties such as the complex refractive index (sopra files) … etc.

4.5.1.1. Contacts type

The Schottky barrier is known as the barrier height at the junction for the injection of electrons from metal to semiconductor conduction band, and it is equal to the difference between the metal work function and the electron affinity of semiconductor (relation 2.25, chapter 2). Therefore the metal work function defines if the contact is a rectifying or Ohmic.

The command "contact" is used to tell ATLAS how to treat the electrode. In the default condition, an electrode in contact is assumed to be Ohmic. If the electrode is wanted to be treated like a Schottky contact, then the appropriate work function must be defined according to the relation (4.1) for n type semiconductors:

$$\phi_m = \phi_B + \chi_s \tag{4.1}$$

And for p-type semiconductor the work function is equal to:

$$\phi_m = \left(E_g/q\right) - \phi_B + \chi_s \tag{4.2}$$

For example, if the semiconductor was a p type Gallium Arsenide with an affinity of 4.07 eV and energy gap of 1.42 eV, the metal work function must be less than 5.49 eV. This can be defined by the "`contact`" statement as:

```
contact name=cathode  workf=4.28
```

Figure 4.6 shows the difference between the energy band diagram of an Ohmic contact and a Schottky contact defined using the previous statement.

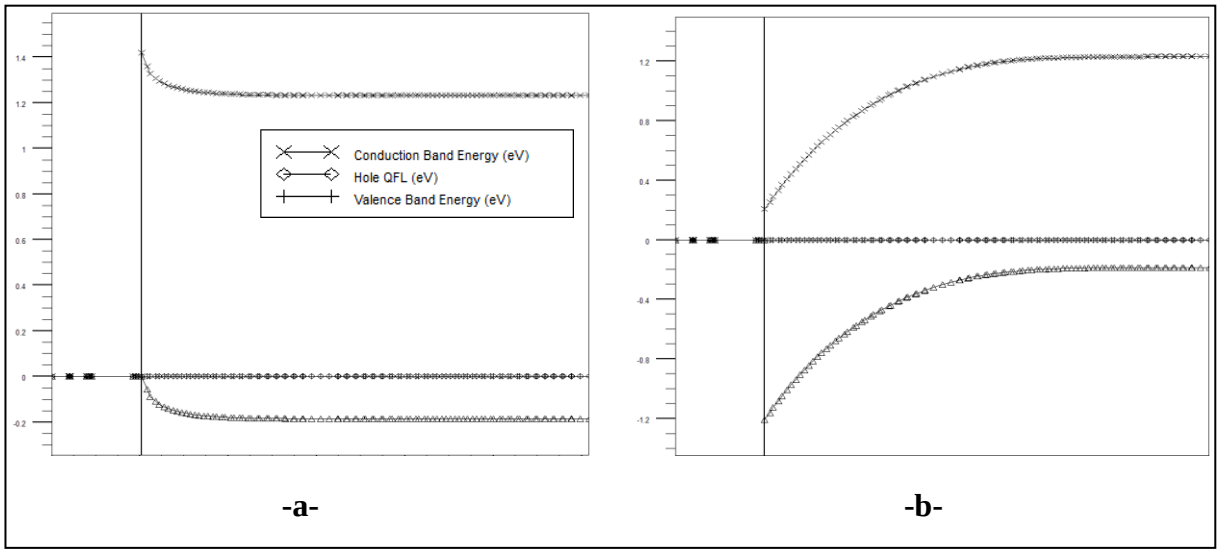


Figure 4.6: Energy band diagram simulated by SILVACO. a- Ohmic contact. b- Schottky contact.

4.5.1.2. Deep defects

The presence of deep defects may significantly influence the electrical characteristics of the device. Two methods are used to introduce deep levels in ATLAS, depending on their spatial distribution: the "trap" statement activates bulk traps at discrete energy levels within the bandgap of the semiconductor with a uniform distribution and sets their parameter values. While the "doping" statement can be used to introduce a non-uniform traps distribution.

As mentioned in chapter 2, deep levels can be defined using their activation energy, emission and capture rates for electrons and holes and their density. These are the required parameters to define traps in ATLAS, in addition to their type and location. The following line of code is an example of the ATLAS syntax for traps definition:

```
trap acceptor x.min=0 x.max=2 y.min=-1.6 y.max=-0.1 \
e.level=1.173 density=1e14 degen=2 sign=7.35e-20 sigp=7.35e-18
```

In this line of code the first word (trap) is the statement and the rest are parameters that describe the trap. Where: "`acceptor`" specifies the traps type, "`x.min, x.max, y.min, y.max`" specify the edges of the region where the traps are located. "`e.level`" specifies the energy level position of traps relative to the conduction band in the case of acceptor traps or valence band in the case of donor traps. The unit here is the electron Volt. Figure 4.7 shows the terminology used within ATLAS to define the energy level position of traps. "`density`" specifies the density of the traps centres in cm^{-3}, "`degen`" specifies the degeneracy factor and

"`sign`, `sigp`" specify the capture cross sections for electrons and holes respectively (in ATLAS, Either the cross section or lifetime parameters should be used to define the capture parameters).

PS: The back slash '\' at the end of the line of code informs ATLAS that the next line of code should be considered as a part of the one preceding it. This is a useful tool to make the code more organized.

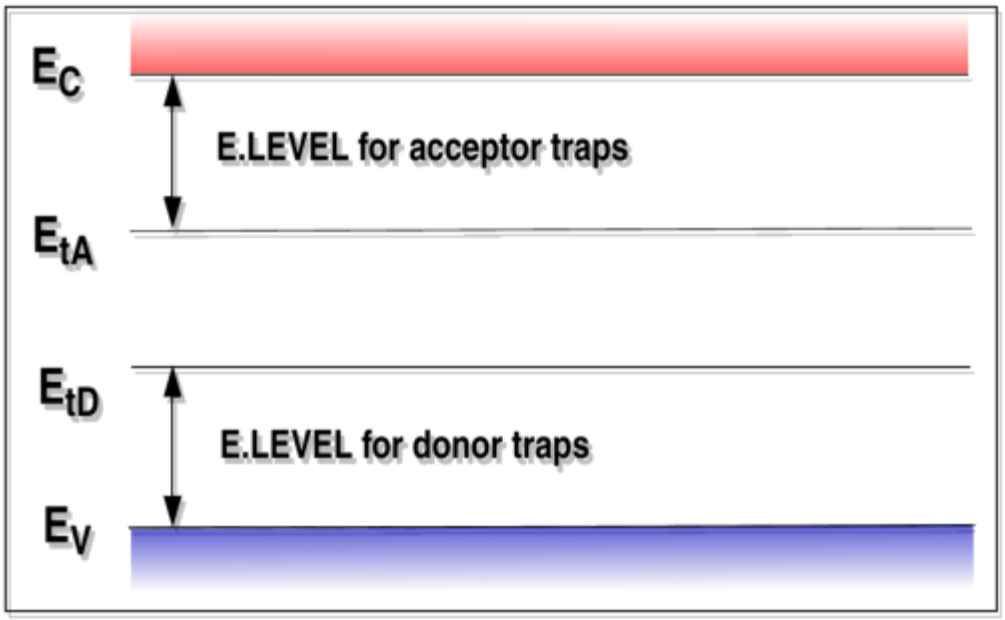


Figure 4.7: ATLAS definition of the trap energy level for acceptor and donor traps in reference to the conduction and valence band edges.

4.5.2. Physical models

To get the simulation to the realistic level, a lot of complex dependencies of the device properties must be taken in consideration such as the mobility variation as a function of carriers' concentration. These complexities are not necessary in some cases, so to avoid the additional calculations, ATALS provides independent models to describe every device property dependence alone, so they can be activated separately. The accuracy of the results obtained depends on the models used in the simulation process.

Physical models are specified using the "`models`" statement. An example of it:

```
models kla fldmob evsatmod=1 hvsatmod=1 srh klaaug incomplete
hcte heat.full temperature=300 print
```

where every parameter of (`kla`, `fldmob`, `evsatmod=1`, `srh`, `auger`, `incomplete`, `hcte`, `heat.full`) enables a specific model. The "`Temperature`" parameter specifies the general temperature of the structure in Kelvin, And "`print`" parameter prints in the output window of DECKBUILD the basic information used in the simulation; such as the status of all models (which models are activated and which are not), basic constants, coefficients used in every model.

4.5.2.1. Mobility

a. CONCENTRATION DEPENDENT MOBILITY

Electrons and holes are accelerated by electric fields, but lose momentum as a result of various scattering processes. These scattering mechanisms include lattice vibrations (phonons), impurity ions, other carriers, surfaces, and other material imperfections. Since the effects of all of these microscopic phenomena are lumped into the macroscopic mobilities introduced by the transport equations, these mobilities are therefore functions of the local electric field, lattice temperature, doping concentration, and so on.

The "`conmob`" parameter is the model that links the mobility to the concentration of dopants. By using it, ATLAS will interpolate the mobilities' values from a predefined empirical data. In fact ATLAS provides a better model for mobility called Klassen's model which can be enabled using the "`KLA`" parameter. This model includes the effects of lattice scattering, impurity scattering (with screening from charged carriers), carrier-carrier scattering, and impurity clustering effects at high concentration as follow:

$$\frac{1}{\mu_{n,p}} = \frac{1}{\mu_{n,pL}} + \frac{1}{\mu_{n,pDAP}} \qquad (4.3)$$

$\mu_{n,p}$ are the total electron and hole mobilities, $\mu_{n,pL}$ are the electron and hole mobilities due to lattice scattering, $\mu_{n,pDAP}$ are the electron and hole mobilities due to donor (D), acceptor (A), screening (P) and carrier-carrier scattering. The model shows excellent agreement between the modelled and empirical data for temperature dependence over the range of 70 K to 500 K [78].

b. PARALLEL ELECTRIC FIELD DEPENDENT MOBILITY

As carriers are accelerated in an electric field their velocity will begin to saturate when the electric field magnitude becomes significant. This effect has to be accounted for by a reduction of the effective mobility since the magnitude of the drift velocity is the product of the mobility and the electric field component in the direction of the current flow. Different models have been adopted in ATLAS [78, 80, 81]. Since the used material in this work is Gallium Arsenide, the Negative Differential Mobility Model of Barnes et al [80] will be enabled using the "`evsatmod=1`" and "`hvsatmod=1`" parameter in addition to "`fldmob`". This model expresses the electric field mobility dependence as:

$$\mu_n(E) = \left[\mu_{n0} + \frac{v_{satn}}{E}\left(\frac{E}{E_0}\right)^{\gamma_n}\right] \Big/ \left[1 + \left(\frac{E}{E_0}\right)^{\gamma_n}\right] \tag{4.4}$$

$$\mu_p(E) = \left[\mu_{p0} + \frac{v_{satp}}{E}(E/E_0)^{\gamma_p}\right] \Big/ [1 + (E/E_0)^{\gamma_p}] \tag{4.5}$$

where v_{satn} and v_{satp} are the electron and hole saturation velocities, E_0, γ_n, γ_p are a constants equal to 4×10^3 V/cm, 4 and 1 respectively. μ_{n0}, μ_{p0} are the total electron and hole mobilities calculated from the Klassen's model. The saturation velocities are calculated by default from the temperature dependent models for GaAs:

$$v_{satn} = v_{satnT0} - v_{satnT1}.T_L \tag{4.6}$$

$$v_{satp} = v_{satpT0} - v_{satpT1}.T_L \tag{4.7}$$

where v_{satnT0}, v_{satpT0} are given by 1.13×10^7 cm/sec, and v_{satnT1}, v_{satpT1} for GaAs are given by 1.2×10^6 cm/sec, and T_L is the lattice temperature in degrees Kelvin.

4.5.2.2. Carrier generation and recombination

Whenever the thermal equilibrium condition of a semiconductor system is disturbed by process, an opposite process exists to restore the system to equilibrium. The first one is the generation while the second is the recombination. ATLAS provides different model them.

a. SHOCKLEY-READ-HALL RECOMBINATION (SRH)

In the presence of defects, the electrons can bridge the semiconductor gap in several smaller steps through these defects instead of making the transition from the valance band to the conduction band and back in a single step. Therefore, the Shockley-Read-Hall generation-recombination process dominates the restoration processes [82]. The Shockley-Read-Hall recombination is modelled using the relation (R_{SRH}) as follows:

$$R_{SRH} = \frac{n.p - n_i^2}{\text{TAUP0}\left(n + n_i \exp\left(\frac{\text{ETRAP}}{KT}\right)\right) + \text{TAUN0}\left(p + n_i \exp\left(\frac{-\text{ETRAP}}{KT}\right)\right)} \qquad (4.8)$$

where ETRAP is the difference between the trap energy level and the intrinsic Fermi level, T is the lattice temperature in degrees Kelvin and "TAUN0" and "TAUP0" are the electron and hole lifetimes which are given by 3.26.

b. SHOCKLEY-READ-HALL RECOMBINATION THROUGH TRAPS

In the presence of traps, the standard Shockley-Read-Hall recombination (which takes into account one trap close to the middle of the gap) is modified as follows:

$$R = \sum_{\alpha=1}^{l} R_{D\alpha} + \sum_{\beta=1}^{m} R_{A\beta} \qquad (4.9)$$

Where "l" is the number of donor like traps, "m" is the number of acceptor like traps. For donor like traps, the function $R_{D\alpha}$ is:

$$R_{D\alpha} = \frac{pn - n_i^2}{\tau_{n\alpha}\left[p + \text{dgen}.n_i exp\left(\frac{E_i - E_{t\alpha}}{KT}\right)\right] + \tau_{p\alpha}\left[n + \frac{1}{\text{dgen}} n_i exp\left(\frac{E_i - E_{t\alpha}}{KT}\right)\right]} \qquad (4.10)$$

For acceptor like traps the function $R_{A\beta}$ is:

$$R_{A\beta} = \frac{pn - n_i^2}{\tau_{n\beta}\left[p + \frac{1}{dgen} n_i exp\left(\frac{E_i - E_{t\beta}}{KT}\right)\right] + \tau_{p\beta}\left[n + dgen.n_i exp\left(\frac{E_i - E_{t\beta}}{KT}\right)\right]} \qquad (4.11)$$

Where τ_n, τ_p are the electron and hole lifetimes. They are related to the carrier capture cross sections through the equations (3.26) and (3.6). Thus:

$$\begin{aligned} \tau_{n\alpha,\beta} &= \frac{1}{v_{th}\sigma_{n\alpha,\beta}N_{\alpha,\beta}} \\ \tau_{p\alpha,\beta} &= \frac{1}{v_{th}\sigma_{p\alpha,\beta}N_{\alpha,\beta}} \end{aligned} \qquad (4.12)$$

Where ($E_{t\alpha,\beta}, \sigma_{n\alpha,\beta}, \sigma_{p\alpha,\beta}, dgen$) are defined by the "trap" statement.

c. AUGER RECOMBINATION

The Auger recombination is a bimolecular recombination where, the released energy during the recombination of an electron and hole is not emitted with a photon but, instead, it is transferred to a third particle (electron or a hole). The energy is eventually transferred non-radiatively from the hot third carrier via phonon emission to the lattice. Auger Recombination is commonly modelled using the expression:

$$R_{Auger} = \text{AUGN}\,(pn^2 - nn_i^2) + \text{AUGP}\,(np^2 - pn_i^2) \qquad (4.13)$$

Where the Auger coefficients AUGN, AUGP are set by default in ATLAS for GaAs as 5.10^{-30}, 1.10^{-31} cm^6/s respectively. More accurate results can be found using the Klassen's temperature dependent Auger model which has been calibrated to work with Klaassen's model for mobility (see page 73) [83]. This model can be activated by specifying the "KLAAUG" parameter. The form of this model is:

$$R_{Auger} = \text{C}_n\,(pn^2 - nn_i^2) + \text{C}_p\,(np^2 - pn_i^2) \qquad (4.14)$$

In this case, the Auger coefficients are temperature dependent according to:

$$\text{C}_n = KAUGCN\left(\frac{T}{300}\right)^{KAUGDN} \qquad (4.15)$$

$$\text{C}_n = KAUGCP\left(\frac{T}{300}\right)^{KAUGDP} \qquad (4.16)$$

Where KAUGCN, KAUGCP, KAUGDN, KAUGDP are constants. Their values are demonstrated in Table 4.2.

Coefficient	Value	Unit
KAUGCN	$1.83*10^{-31}$	cm^6/s
KAUGCP	$2.78*10^{-31}$	cm^6/s
KAUGDN	1.18	/
KAUGDP	0.72	/

Table 4.2: Klassen's constants of the temperature dependent Auger coefficients [84].

4.5.2.3. Space charge

In ATLAS the default is to assume full impurity ionization, and to set the charge due to traps and defects equal to zero. This can be modified using the "`trap`" statement and the "`incomplete`" model.

a. INCOMPLETE IONIZATION

Generally the simulation is carried out at room temperature, where, in most cases, the semiconductor is considered in the full impurities ionization state. However, as temperature is decreased, full ionization of impurities can no longer be assumed. In this case, the dependence of ionized impurities on temperature is modelled using Fermi-Dirac statistics.

The ionized donor and acceptor impurity concentrations are given by:

$$N_D^+ = \frac{N_D}{1+\mathrm{GCB}\,\exp\left(\frac{E_{Fn}-(E_C-\mathrm{EDB})}{KT}\right)} \tag{4.17}$$

$$N_A^- = \frac{N_A}{1+GVB\,\exp\left(\frac{E_V-E_{Fp}-EAB)}{KT}\right)} \tag{4.18}$$

Where `EDB` and `EAB` are the dopant activation energies, `GCB` and `GVB` are the conduction and valence band degeneracy factor (where `GCB`=2 and `GVB`=4 [85]), N_D and N_A are the net compensated n-type and p-type doping, respectively. Net compensated doping is defined as follows:

If ($N_{Tot} = N_{D,total} - N_{A,total} > 0$) Then:

$$N_D = |N_{Tot}| \quad \text{and} \quad N_A = 0$$

Else:

$$N_D = 0 \quad \text{and} \quad N_A = |N_{Tot}|$$

b. TRAPS IONIZATION

Due the probability of being at any energy level within the gap, the temperature has a significant effect on traps ionization compared to impurities ionization. ATLAS simulates the temperature effect on traps ionization according to relation (3.21) as follow:

$$N_{tD}^+ = DENSITY\ \frac{v_{thn}SIGN.n+e_{pA}}{v_{thn}SIGN.n+v_{thp}SIGN.p+e_{nA}+e_{pA}} \tag{4.19}$$

$$N_{tA}^- = DENSITY\ \frac{v_{thp}SIGP.p+e_{nD}}{v_{thn}SIGN.n+v_{thp}SIGN.p+e_{nD}+e_{pD}} \tag{4.20}$$

Where e_{nD}, e_{pD} are electron and hole emission rates for donor like traps, and e_{nA}, e_{pA} are electron and hole emission rates for acceptor like traps respectively. Taking into account that is the "empty" and "filled" conditions of a defect will normally have different spin and orbital degeneracy choices, the emission rates will be written as follows:

$$\begin{aligned} e_{nD} &= \frac{1}{DGEN} \,.v_{thn} \,.\; SIGN \,.\; n_i \exp\left(\frac{E_t - E_{Fi}}{KT}\right) \\ e_{pD} &= DGEN \,.v_{thp} \,.\; SIGP \,.\; n_i \exp\left(\frac{E_{Fi} - E_t}{KT}\right) \\ e_{nA} &= DGEN \,.\; v_{thn} \,.\; SIGN \,.\; n_i \exp\left(\frac{E_t - E_{Fi}}{KT}\right) \\ e_{pA} &= \frac{1}{DGEN} \,.v_{thp} \,.SIGP \,.\; n_i \exp\left(\frac{E_{Fi} - E_t}{KT}\right) \end{aligned} \qquad (4.21)$$

Where $(E_t, SIGN, SIGN, DGEN)$ are defined by the "trap" statement.

4.5.2.4. Band gap model

Band gap changes with higher temperature mainly arise from the change of the lattice constant. Experimental results show that the band gaps of most semiconductors decrease with increasing temperature [1]. The variation of the band gap with temperature is modelled in ATLAS by a universal function:

$$E_g(T) = E_g(0) - \frac{\alpha.T^2}{T+\beta} = E_g(300) + \alpha\left[\frac{300^2}{300+\beta} - \frac{T^2}{T+\beta}\right] \qquad (4.22)$$

Where $(E_g(300) = 1.42$ eV, $\alpha = 5{,}4 * 10^{-4}\, eV/K$, $\beta = 204\, K)$ for GaAs [1]. This model can be activated by setting the "`Eg300`" parameter in the "`Material`" statement.

4.5.2.5. Device's Self-Heating

ATLAS can account for lattice heat flow and general thermal environments using the Wachutka's model of lattice heating [86], which accounts for Joule heating, heating, and cooling due to carrier generation and recombination, and the Peltier and Thomson effects. ATLAS will also account for the dependence of material and transport parameters on the lattice temperature. By adopting this model, the lattice heat flow equation will be added to the dynamic continuity equations for electrons and holes flow:

$$c\left(\frac{\partial T}{\partial t}\right) = div\left(k\vec{\nabla}T\right) + H \qquad (4.23)$$

Where "c" is the heat capacitance per unit volume, "k" is the thermal conductivity, and "H" is the heat generation rate which equal to:

$$H = H_J + H_{PT} + H_{GR} \tag{4.24}$$

Where "H_J, H_{PT}, H_{GR}" are the joule, Peltier and Thompson, generation and recombination heating and cooling respectively. By specifying the "`Hcte`" parameter, ATLAS will use a simple model that accounts only a simplified Joule heating equation. The other effects will be included only if the "`HEAT.FULL`" parameter is specified in the MODELS statement.

4.6. Numerical solution and methods

The device electrical properties are modelled using numerical solutions of fundamental partial differential equations that link the electrostatic potential with the carrier densities. For each mesh point of a given device, ATLAS solves a system of three partial differential equations which are the Poisson's equation and the holes and electrons equations of continuity. ATLAS produces numerical solutions by calculating the values of the unknowns at each grid point of the device. An internal discretization process converts the original continuous model into a discrete nonlinear algebraic system that has identical behaviour. The discrete algebraic system is solved using an iterative process that refines the solution. The solution is obtained if the convergence criteria are satisfied. Otherwise, the iterations continue and stop after a limited number of iterations predefined, after that, the system is considered as a non-convergent system. The nonlinear iterative method starts from an initial guess. Corrections are calculated by solving a linear version of the problem. The linear sub-problems are solved by using direct or iterative techniques.

ATLAS provides several numerical methods to calculate the solutions of semiconductor device problems. There are three main types of numerical methods:

The first method is the GUMMEL type which is useful where the system of equations is weakly coupled but has only linear convergence [78, 87]. This method will solve for each variable in turn keeping the other variables constant (their most recently computed values), repeating the process until a stable solution is achieved. GUMMEL iteration typically tolerate relatively poor initial guesses, it converges relatively slowly.

The second method is NEWTON, which is useful when the system of equations is strongly coupled and has quadratic convergence [88]. Unlike GUMMEL method, each iteration of the

NEWTON method solves a linearized version of the entire non-linear algebraic system (the total system of unknowns together). This method requires a more accurate initial guess to obtain convergence and causes ATLAS to spend extra time solving for quantities which are essentially constant or weakly coupled. Therefore, each iteration takes a relatively long time (compared to GUMMEL[78]) but it requires fewer iteration.

The final method is the BLOCK method which can provide faster simulation times in situations where the NEWTON method struggles. BLOCK iterations involve solving subgroups of equations in various sequences. For example, in non-isothermal drift-diffusion simulation, specifying the BLOCK method means that NEWTON's method is used to solve the three basic equations (holes and electrons and Poisson's equations), after which the heat flow equation is solved in a decoupled step.

The solution can also be done using a combination of the previous mentioned methods by starting the solution with the GUMMEL method then switching to BLOCK or NEWTON if convergence has not occurred within a certain number of iterations. By adopting this strategy, GUMMEL method can refine initial guess to a point from which NEWTON iteration can converge.

Numerical methods are given in the METHOD statements of the input file. An example of a "METHOD" statement is:

```
METHOD GUMMEL NEWTON
```

4.7. Solution Specification

After the specification of device structure, materials properties and physical models, the simulation is ready to be taken to the next step (the solution). This section of the input deck to ATLAS is where the simulation does its calculations to solve for the device specified. It is divided up into four parts: LOG, SOLVE, OUTPUT and SAVE.

4.7.1. The "LOG" statement

The "LOG" statement creates a save file where all results of a run will be saved; Any DC, transient or AC data generated by "SOLVE" statements after the "LOG" statement will be saved. An example of "LOG" statement in which data is saved into file named "Schottky.log" is:

```
LOG OUTFILE = Schottky.log
```

4.7.2. The "SOLVE" statement

The "SOLVE" statement calculates information at one or more bias points for D.C. or A.C. But first, a simplified initial solution must be done (which solves only Poisson's equation) to get an initial guess for the final solution. An example of "SOLVE" statement for a D.C analysis that ramps the Anode voltage from (0.0 V) to (1.0 V) with (0.05 V) steps:

```
SOLVE INIT

SOLVE VANODE=0.0 VSTEP=0.05 VFINAL=1.0 NAME=ANODE
```

Another parameter must be added to the "solve" statement to get the device capacitance and conductance is "AC". By specifying this parameter an A.C. sinusoidal small signal analysis will be performed after each D.C. condition solve. An example of "SOLVE" statement for an A.C. analysis that ramps the Anode voltage from (0.0 V) to (1.0 V) with (0.05 V) steps and calculates the capacitance and conductance for each bias point. A small A.C. signal with frequency of (100 Hz) is applied to each electrode in the device:

```
SOLVE INIT

SOLVE VANODE=0.0 VSTEP=0.05 VFINAL=1.0 NAME=ANODE ac freq=1e2
```

4.7.2.1. Direct current simulation

The model used in ATLAS consists of a set of fundamental equations, which link together the electrostatic potential and the carrier densities, within some simulation domain. These equations, which are solved inside any general purpose device simulator, have been derived from Maxwell's laws and consist of Poisson's equation, the carrier continuity equations and the transport equations.

The current density equations, or charge transport models, are usually obtained by applying approximations and simplifications to the Boltzmann Transport Equation. These assumptions can result in a number of different transport models. The simplest model of charge transport that is useful is the drift–diffusion model. This model is adequate for nearly all devices that were technologically feasible [1]. This model is based on the two first equations cited above. The Poisson's equation which relates the electrostatic potential to the space charge density:

$$div(\varepsilon \nabla \psi) = -\rho \quad (4.25)$$

Where "ψ" is the electrostatic potential, "ε" is the local permittivity, and "ρ" is the local space charge density.

And the continuity equations for electrons and holes, given respectively by:

$$\frac{\partial n}{\partial t} = \frac{1}{q} div\overrightarrow{J_n} + G_n - R_n \quad (4.26)$$

$$\frac{\partial p}{\partial t} = \frac{1}{q} div\overrightarrow{J_p} + G_p - R_p \quad (4.27)$$

where "n" and "p" are the electron and hole concentration, "J_n" and "J_p" are the electron and hole current densities, "G_n" and "G_p" are the generation rates for electrons and holes, "R_n" and "R_p" are the recombination rates for electrons and holes, and "q" is the electron charge.

In steady state these equations becomes:

$$0 = \frac{1}{q} div\overrightarrow{J_n} + G_n - R_n \quad (4.28)$$

$$0 = \frac{1}{q} div\overrightarrow{J_p} + G_p - R_p \quad (4.29)$$

By default ATLAS includes both equations (4.26) and (4.27). In some circumstances, however, it is sufficient to solve only one carrier continuity equation.

In the drift–diffusion model, the current densities are expressed in terms of the quasi-Fermi levels as:

$$\overrightarrow{J_n} = -q\mu_n n \nabla \phi_n \quad (4.30)$$

$$\overrightarrow{J_p} = -q\mu_p p \nabla \phi_p \quad (4.31)$$

where "μ_n" and "μ_p" are the electron and hole mobilities. The quasi-Fermi levels are then linked to the carrier concentrations and the potential through the two Boltzmann approximations:

$$n = n_i exp\left(q\frac{\psi - \phi_n}{KT}\right) \quad (4.32)$$

$$p = n_i exp\left(-q\frac{\psi - \phi_p}{KT}\right) \quad (4.33)$$

where "n_i" is the effective intrinsic concentration and "T" is the lattice temperature. These two equations may then be rewritten to define the quasi-Fermi potentials:

$$\phi_n = \psi - \frac{KT}{q}\ln\left(\frac{n}{n_i}\right) \tag{4.34}$$

$$\phi_p = \psi + \frac{KT}{q}\ln\left(\frac{p}{n_i}\right) \tag{4.35}$$

By substituting these equations into the current density expressions, the following current relationships are obtained:

$$\overrightarrow{J_n} = qD_n\nabla n - q\mu_n n\nabla\psi - \mu_n nKT\nabla\ln(n_i) \tag{4.36}$$

$$\overrightarrow{J_p} = -qD_p\nabla p - q\mu_p p\nabla\psi + \mu_p pKT\nabla\ln(n_i) \tag{4.37}$$

assumed that the Einstein relationship holds:

$$D_n = \frac{KT}{q}\mu_n \tag{4.38}$$

$$D_p = \frac{KT}{q}\mu_p \tag{4.39}$$

The final term in (4.36) and (4.37) account for the gradient in the effective intrinsic carrier concentration, which takes account of bandgap narrowing effects.

The conventional formulation of drift–diffusion equations is:

$$\overrightarrow{J_n} = qD_n\nabla n + q\mu_n n\overrightarrow{E_n} \tag{4.40}$$

$$\overrightarrow{J_p} = -qD_p\nabla p + q\mu_p p\overrightarrow{E_p} \tag{4.41}$$

where:

$$\overrightarrow{E_n} = -\nabla\psi - \frac{KT}{q}\nabla\ln(n_i) \tag{4.42}$$

$$\overrightarrow{E_p} = -\nabla\psi + \frac{KT}{q}\nabla\ln(n_i) \tag{4.43}$$

The electrical characteristics are calculated following the specified physical structure and bias conditions. This is achieved by applying the set of differential equations (Poisson's and continuity equations) onto the mesh grid (or equation's discretisation), then, the transport of carriers through the structure can be simulated.

4.7.2.2. Alternating current simulation

Once the D.C. solution is obtained, it can be developed into an A.C. solution (sinusoidal steady state analysis). The frequency-domain perturbation analysis of a D.C. solution can be used to calculate small-signal characteristics at any specified frequency [89]. The calculation proceeds in the following manner:

- Variables are represented as the sum of the known D.C. component and a small unknown sinusoidal A.C. component. Therefore we write:

$$F\left(X_s + dX_s.exp(j\omega t)\right) = DC.exp(j\omega t) \qquad (4.44)$$

  Where "F" can be equal ψ, n or p.
- All equations are expanded.
- Differentiation in time becomes multiplication by the value of ω ($\omega = 2\pi f$).
- Products of A.C. quantities are neglected since they are small with respect to other quantities.
- The D.C. solution is subtracted.
- Small unknown sinusoidal A.C. component means that the D.C. solution is not perturbed and everything is linear.
- What remains is a complex system whose unknowns are the A.C. components of the solution, now we can solve the A.C. part directly from the D.C. solution. The results are complex, the real parts are converted into conductance values and the complex parts are converted into capacitances.

4.7.3. "OUTPUT" and "SAVE" statements

Some of the obtained results have different values along the structure (distribution) such as electron and hole densities, potential …etc. this requires a structural presentation. For that purpose, ATLAS provides the possibility of saving these data into a structure file (.str) using the "save" statement. Figure 4.8 shows the dopants concentration distribution at 1V. An example of the "save" statement which stores the data into a file named (Schottky_Vanode_1.str) is:

```
save outf=Schottky_Vanode_1.str
```

N.B. These statement save the structure electrical data at the last solved bias point.

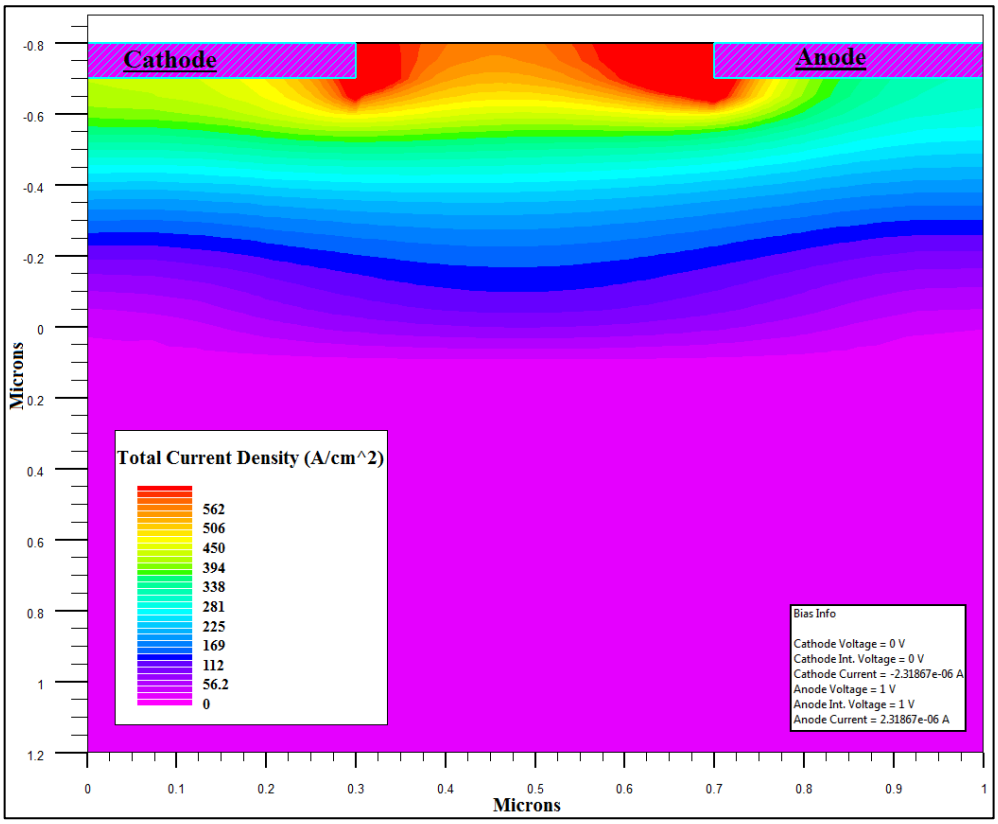


Figure 4.8: Current density distribution in the device with applied bias equal to 1V.

By using the save statement ATLAS will save a basic data such as (dopants, ionized dopants, electrons and holes concentration ….etc.). ATLAS can add to the structure file other quantities specified by user such as (conduction and valence bands, electrons and holes quasi Fermi levels … etc. see Figure 4.6).

Chapter 5

Results and discussion

5.1. Introduction

Silicon (Si) and Beryllium (Be) are the main doping elements in III–V semiconductors like Gallium Arsenide (GaAs). Be is an acceptor (p-type) dopant. However Si can be either a donor (n-type) or an acceptor. This mainly depends on the growth conditions which force Si to occupy a Ga or As site. Hole mobilities in Be-doped GaAs grown on conventional (100) GaAs substrate are considerably lower than those obtained by growing on (N11)A oriented surface (N = 1, 2,3), so called high index substrate, using silicon as p-type dopant [7]. the growth of semiconductor layers and structures strongly depends on the substrate orientation and hence to surface atomic arrangement [18, 90]. Since the (100) direction is the conventional (natural) GaAs orientation, other orientations may lead to the creation of defects. Usually defects have undesirable effects on the electrical and optical properties of III-V based devices [91].

Several structures of Si -doped p-type GaAs samples were grown by MBE on GaAs of different orientations and characterised by the Nanoelectronics group at the University of Nottingham (UK) [76]. In this work two of these devices grown on (211)A and (311)A oriented GaAs semi-insulating substrates, named hereafter NU928 and NU926, respectively are studied in detail using SILVACO simulation to understand some of the strange behaviour of the capacitance-voltage (C-V) characteristics. At Nottingham, these devices are investigated using C–V measurements at different temperatures and deep level transient (DLTS) technique. The C-V characteristics give valuable information about the device structure while DLTS reveals the presence or absence of defects in these devices. The C-V characteristics showed a strange behaviour. The C-V characteristics also had unusual temperature dependence. Different types of defects were found in these structures. In order to relate the capacitance–temperature relationship to the observed deep levels, the ATLAS module of the commercial software (SILVACO-TCAD) is used to calculate these characteristics of the two samples [78]. The experimental and simulation results are then compared.

5.2. Experimental details

5.2.1. Samples used in this study

The samples investigated in this work were grown in a Varian Gen-II MBE machine. The growth temperature was 580 °C and the As:Ga beam equivalent flux ratio determined by an ionization gauge was 12:1 (As overpressure was $1 \times 10^{-5}\ Torr$). The growth rate was one monolayer per second ($\sim 1\ \mu m/h$) as measured by the Reflection High Energy Electron Diffraction (RHEED) technique. The samples were rotated during the growth to enhance uniformity. A schematic representation of the grown Schottky diode is shown in figure 5.1.

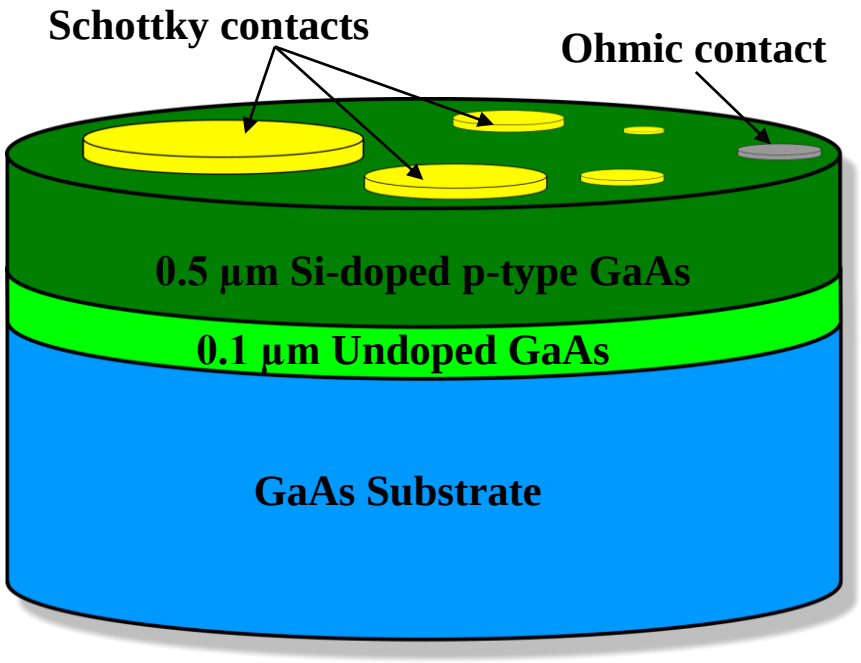


Figure 5.1: Schematic representation of the grown structures.

The NU926Sample is grown on a semi-insulating (311)A GaAs substrate. The NU928 sample has the same structure except that it is grown on (211)A GaAs substrate. First an undoped GaAs buffer layer, 0.1 μm thick, is grown on the GaAs substrate. Then it is followed by a 0.5 μm thick Si-doped p-type GaAs layer. The silicon source cell was set to a temperature which normally gives an effective doping level of $N_{eff} = 1 \times 10^{17} cm^{-3}$ for the (100) samples. A carrier concentration of the (211)A and (311)A samples of $N_{eff} = 0.8 \times 10^{17} cm^{-3}$ was evaluated at room temperature using the Hall Effect and capacitance–voltage

measurements. refers to the acceptor concentration and to the donor concentration. Although these measurements indicate that the auto-compensation is similar in both substrate orientations, previous detailed assessment of the low-temperature photoluminescence spectra of p-type Si-doped (311)A and (111)A samples with a carrier concentration of $2 \times 10^{16} cm^{-3}$ suggested that the (31l)A samples are more compensated than the (111)A samples [92].

The structure was processed into mesa where the Schottky contacts were realised by evaporating Ti/Au on the top of the doped GaAs layer. The top layer was etched up for the deposition of Ohmic contacts using an Au/Ni/Au alloy.

5.2.2. Capacitance–voltage-temperature measurements

First the capacitance–voltage characteristics are measured at different temperatures ranging from 10 to 300 K for the two samples. The C–V characteristics are measured using a BOONTON 7200 Capacitance Meter, which is controlled by a computer. These characteristics are shown in Figure 5.2 and 5.3 for the NU926 NU928 samples respectively. The characteristics are presented using similar scales so that a comparison can be made.

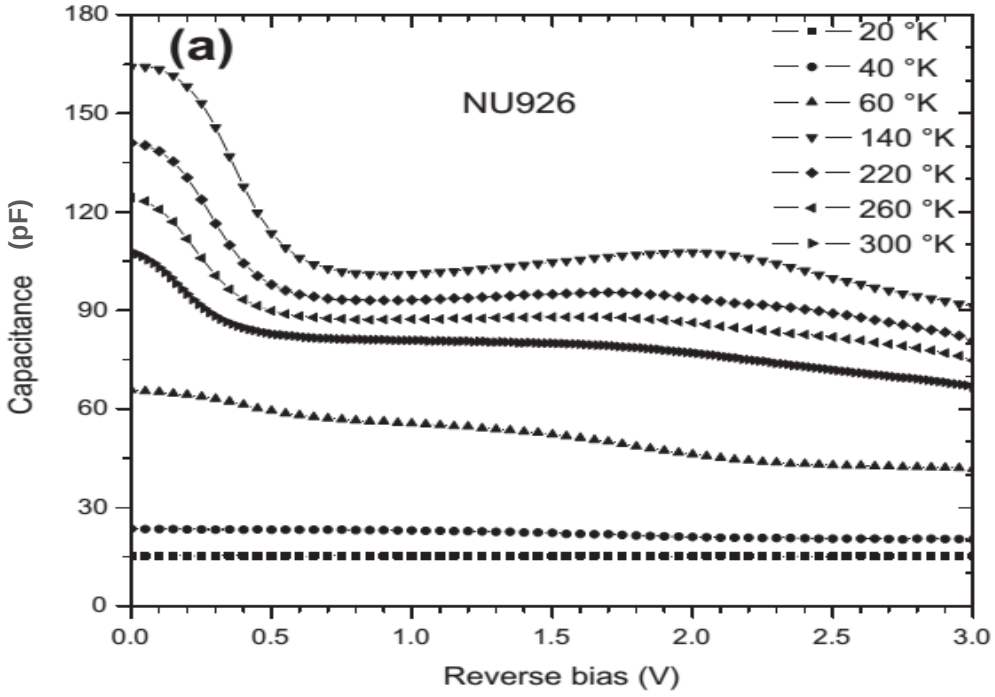


Figure 5.2: The capacitance–voltage characteristics at different temperatures for the NU926 sample.

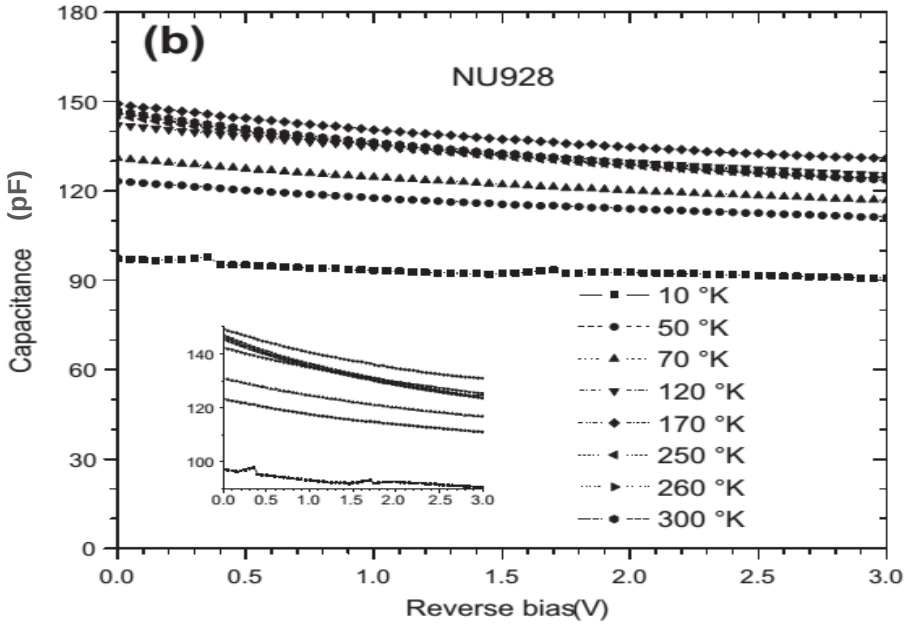


Figure 5.3: The capacitance–voltage characteristics at different temperatures for the NU928 sample.

The first observation is that the NU926 sample characteristics have a more complicated shape and are more affected by the temperature. It is evident that for this sample the C–V curve departs from the conventional shape characterized by the proportionality

$$C \propto 1/\sqrt{(V_{Bi} + |V_R|)} \qquad (5.1)$$

Here V_{Bi} and V_R are the built-in voltage and the reverse voltages, respectively. Instead the C-V characteristics show a negative differential capacitance (NDC) phenomenon in particular at higher temperatures. The departure of the C-V characteristics from the usual behaviour will be shown later that is due to the presence of different types of deep levels in the two structures. The deep levels are revealed by DLTS measurements. It is also worth to note the scale difference in the capacitance of the two samples as shown by the insert in Figure 5.3.

The second observation is that the capacitance initially increases with increasing temperature then starts to drop at temperatures of 120 and 170 °K for NU926 and NU928, respectively. This behaviour is more pronounced for the NU926 sample. The temperature behaviour of the capacitance is better illustrated by plotting the capacitance–temperature characteristics at a fixed voltage as shown in Figure 5.4.

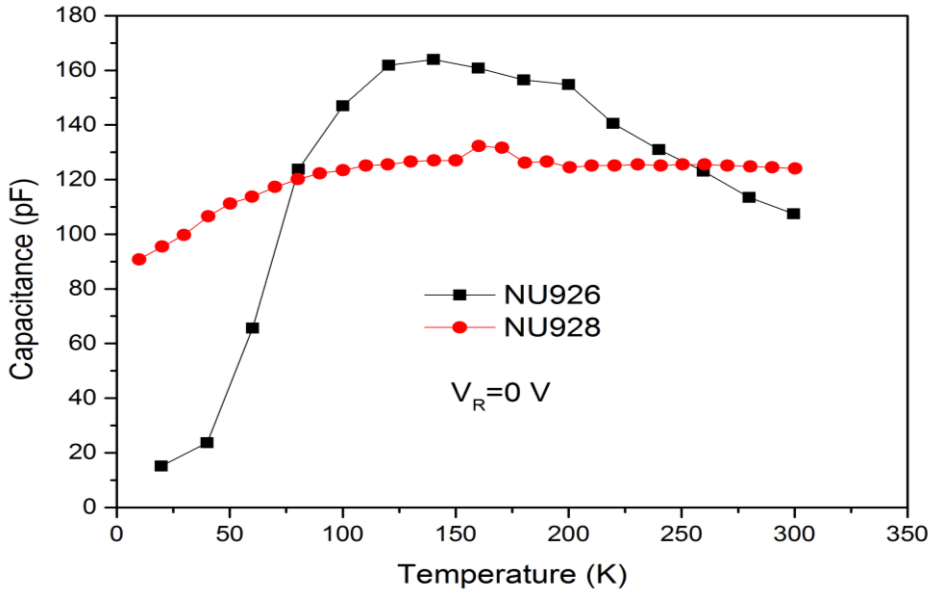


Figure 5.4: The capacitance–Temperature characteristics at fixed bias (V=0) for the samples (311)A (NU926) and (211)A (NU928).

The analysis of the C–V characteristics provides important indications about the values of the Schottky diode parameters such as the built-in voltage, the background doping concentration and concentration depth profile. For the example the evolution of the effective doping density with temperature is shown in Figure 5.5. The importance of these parameters evaluation lies in the fact DLTS data analysis relies on these parameters.

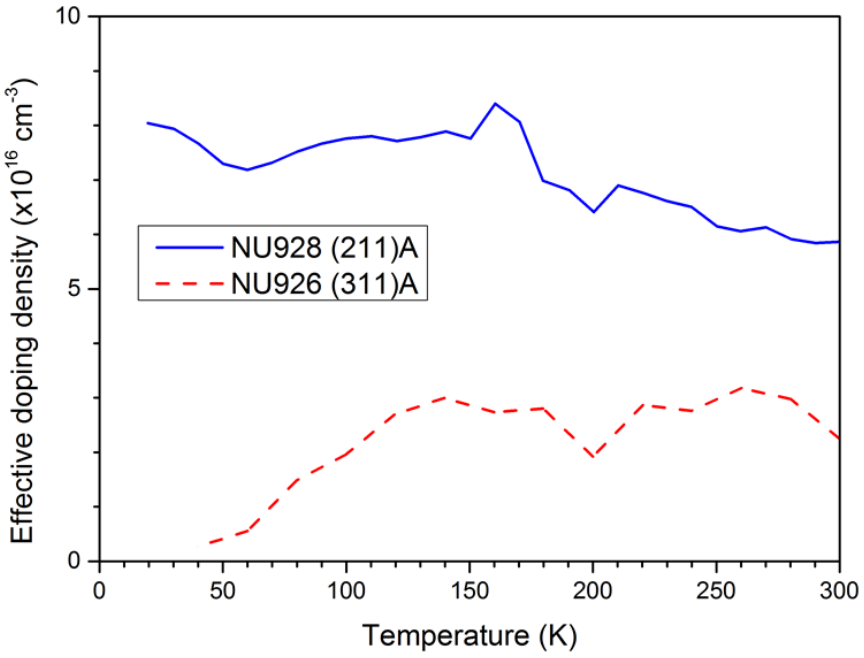


Figure 5.5: The average effective density evaluated from the C–V characteristics of the (211)A and (311)A samples at different temperatures.

At 300 K, the average effective density is $\sim 6 \times 10^{16} cm^{-3}$ and $\sim 2.2 \times 10^{16} cm^{-3}$ for the NU926 and NU928 samples, respectively. The effective density is a bit different from that of Hall measurements especially for the NU928 sample. This is may be due to the non-uniformity of the effective density and defects profile in these samples as will be shown later in the simulation part.

5.2.3. DLTS and Laplace DLTS measurements

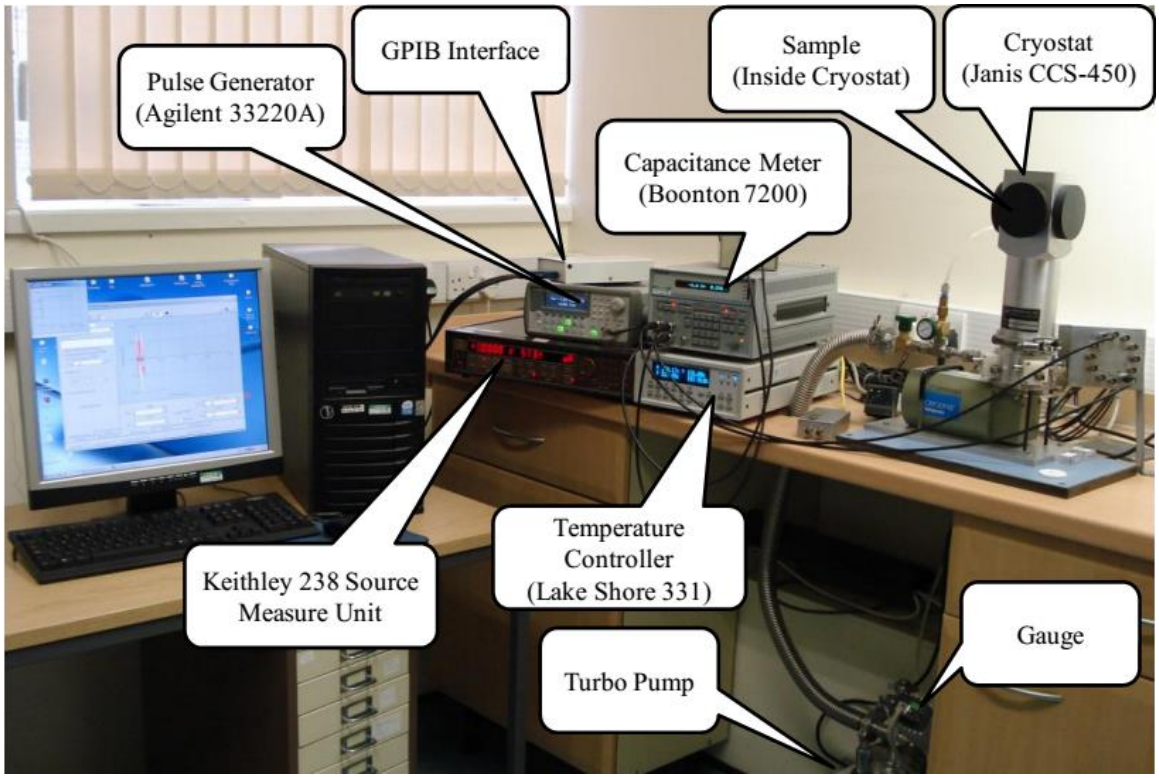


Figure 5.6: A photograph of the DLTS system at Nottingham University [76].

DLTS and Laplace DLTS are used as the main tool for the characterization of deep levels present in semiconductors. The samples packaged in a TO5 header were mounted on a sample holder and downloaded inside a cryostat (type Janis CCS-450) operating in a Closed Cycle Cryodyne. A photograph of the full DLTS system is shown in figure 5.6. The samples were first cooled down to a temperature of 10 K.. DLTS measurements were then started by increasing the temperature at a rate of 2 K/min. A train of electrical pulses, generated by a pulse generator (model Agilent 33220A) was applied to the sample. The filling pulse frequency is 50 Hz. The reverse bias (VR) and filling pulse (VP) is applied in such a way that

VP > VR. The defects are observed in a DLTS spectrum as peaks. Sometime, in particular when many defects are present, the peaks are not well resolved. For the resolution of these broad DLTS peaks, high resolution Laplace DLTS measurements were carried out. Laplace DLTS is an isothermal DLTS process; therefore, the measurements are performed at constant temperature within a temperature range where the conventional DLTS peak appears. The transient measured at a fixed temperature is analysed using a Laplace Transform formalism to separate the different signals due to the different deep levels.

DLTS measurements are performed to reveal the presence of deep levels in the two samples. Typical DLTS spectrums are presented in Figure 5.7 and 5.8 for the NU926 and NU928 samples respectively. The filling pulse has a height of 0.8 V, a reverse bias of 0.5 V and a filling time of 1 ms (corresponding to a frequency of 1 KHz). The rate window varies from 2.5 to 200 Hz by a factor of 2. In the DLTS spectrum and in p-type samples, a negative peak is signature of majority deep levels (hole deep levels in this case) while a positive peak represents a minority deep level (electron deep levels).

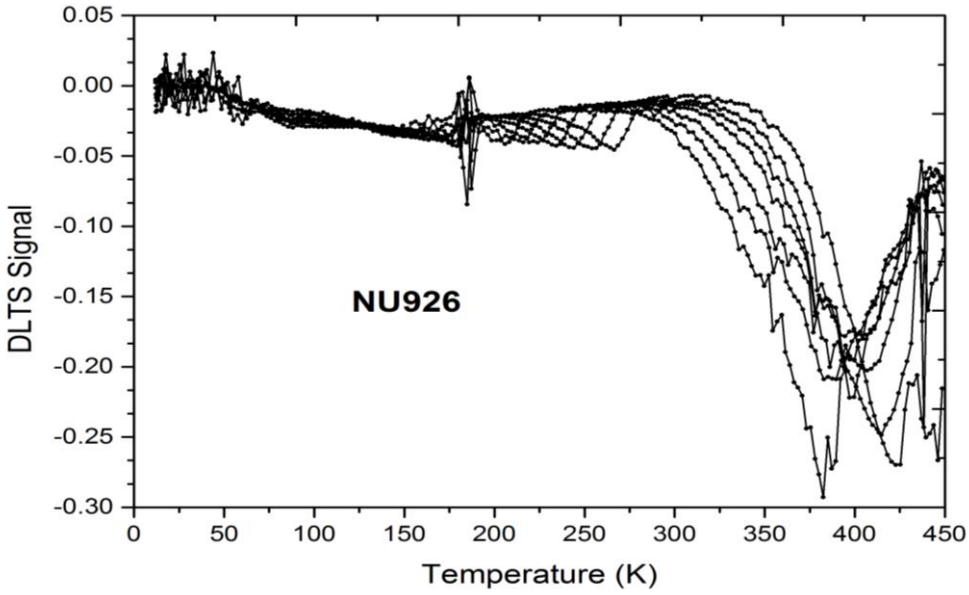


Figure 5.7: DLTS spectra for the sample (311)A (NU926).

In the NU926 sample, only majority (hole) deep levels are detected while both hole and electron deep levels are observed in NU928. Notice also the difference in the scales of the DLTS signals of the two samples. The electron deep levels DLTS signal in the NU928 sample is about 40 times larger than that of hole deep levels. This is clarified by the insert in Figure 5.8. The positive DLTS signal (signature of electron deep levels) is divided by a factor of 20 to clearly reveal the negative signal (hole deep levels). This means that the electron deep

levels have a much higher density than hole deep levels. These are the main reasons (different types of deep levels and different densities) of the observed behaviours differences for the C-V characteristics of the two samples.

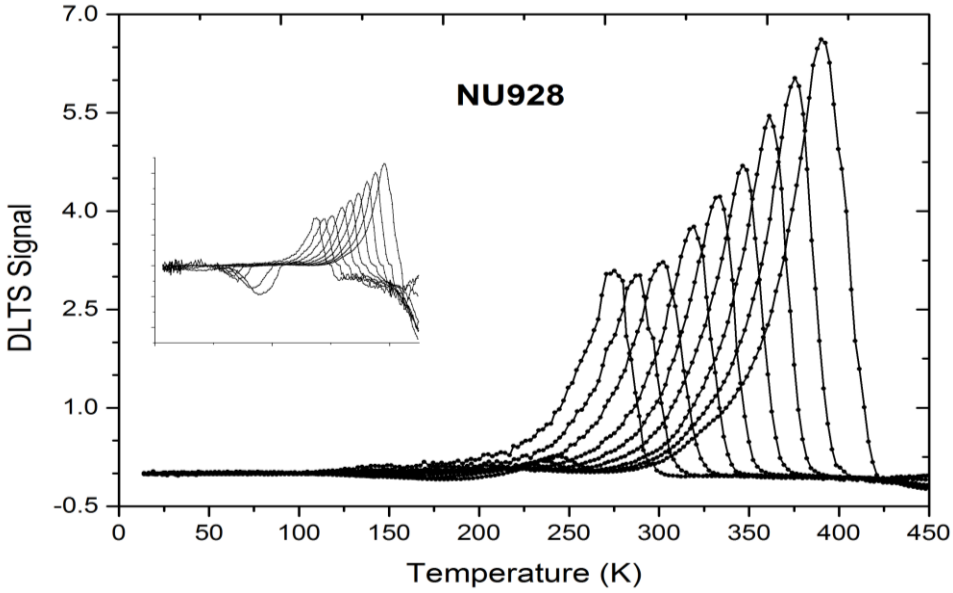


Figure 5.8: DLTS spectra for the sample (211)A (NU928). In the insert in (b), the positive signal (electron deep levels) is divided by 20.

The deep acceptor parameters are measured by Laplace DLTS whereas the electron trap parameters are extracted from the conventional DLTS spectrum for both samples. For the NU926 sample, the evaluated parameters of the deep acceptors are shown in Table 5.1. For the NU928 sample, the parameters of deep acceptors and donors are given in Table 5.2. In both tables the activation energy is above the valence band for the deep acceptors (H) and below the conduction band deep donors (E).

The origin of the observed defects could be due to complexes involving silicon atoms, background impurities, and defects related to the growth conditions. It is also worth pointing out that the samples studied in this work are p-type Si-doped (211)A and (311)A GaAs substrates. Silicon always behaves as n-type dopant in (100) GaAs [76]. Therefore it is expected that Si which primary acts as a dopant may also introduce defects in GaAs grown on non-conventional oriented substrates. Finally, it is worth to mention that not much work is carried out on deep levels in p-type GaAs grown either on conventional (100) or non-conventional (N11, N≠1) GaAs substrates.

Deep level	Activation energy (eV)	Density (cm^{-3})	Capture cross section (cm^2)
H1	0.025 ± 0.003	1.43×10^{15}	1.63×10^{-18}
H2	0.014 ± 0.002	1.47×10^{15}	4.79×10^{-17}
H3	0.247 ± 0.005	1.19×10^{15}	7.35×10^{-18}
H4	0.837 ± 0.007	1.54×10^{15}	6.75×10^{-18}

Table 5.1: The defect parameters determined by Laplace DLTS for the sample (311)A.

Deep level	Activation energy (eV)	Density (cm^{-3})	Capture cross section (cm^2)
H1	0.061 ± 0.003	5.65×10^{15}	5.35×10^{-16}
H2	0.075 ± 0.011	6.64×10^{15}	4.36×10^{-16}
H3	0.153 ± 0.030	2.81×10^{15}	4.36×10^{-16}
H4	0.170 ± 0.020	3.39×10^{15}	4.77×10^{-16}
H5	0.283 ± 0.001	7.83×10^{14}	3.99×10^{-16}
E	0.431 ± 0.019	1.68×10^{16}	3.33×10^{-17}

Table 5.2: The defect parameters determined by Laplace DLTS for the sample (211)A.

5.3. Simulated structures

Numerical simulation starts usually by collecting information about the device to be simulated. These include its structure, geometry, the used materials and their physical properties …etc. The latter information is not always available, so the physical properties can be classified into two classes: known and unknown parameters. These parameters are so important that essentially impose to study the influence of all of them. Thus, this study by simulation will make possible the determination of the critical and significant parameters in the operation of any type of devices and thus the optimization of their performances. To identify the unknown parameters we should scan their value one by one, while fixing that of the others each time. At each scan the simulation is compared to experimental results.

In this work, it has to be mentioned that there are so many different parameters to adjust to fit the simulation to measurements (several defects, each of them is characterized by three parameters: energy level, capture cross section and density, in addition to other parameters of the material such as mobility, lifetime, and doping density). Therefore numerical simulation is usually more difficult than analytical. In the latter, much fewer parameters have to be adjusted and in most cases they do not have a physical meaning. In this work the parameters of deep

levels are fixed (Table 5.1 and 5.2) and the doping density is adjusted so that simulation is as close as possible to measurements. A value of $\sim 1 \times 10^{16} cm^{-3}$ gives the best comparison between simulation and measurements. This value is a bit lower than the effective doping density evaluated from the C-V characteristics and Hall measurements. This may be due to the presence of other shallow levels in both structures and hence may contribute to the effective doping density in the simulation. This is perhaps a first indication that the shallow levels, detected by Laplace DLTS, may be related to the doping element (Si).

To simulate the operation of a given structure, it is essential to apply a grid adapted to this one. Thus it is necessary to find a compromise between computing time and calculation precision. To satisfy this compromise, a fine grid is applied in the regions where the variations of the physical parameters are significant and a wider grid in the zones where these variations are insignificant. Thus, the grid is refined in the critical zones which are the zone around Schottky contact (depletion region) and the buffer layer interfaces. While in the rest of the active region (P-type doped GaAs) the grid varies from fine to wide. Finally for the substrate, the applied grid is wide because the physical parameters variations are very small. Figure 5.9 represents the grid used to simulate the devices.

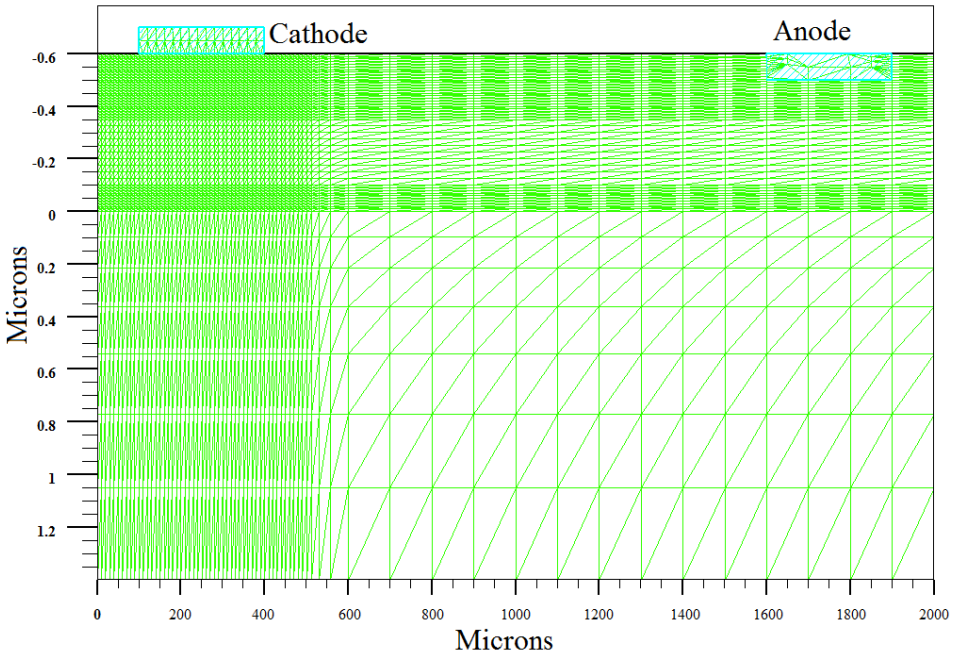


Figure 5.9: The mesh grid used in the structure simulation.

The structure of the device simulated in this work is shown in Figure 5.10. It consists of GaAs substrate of thickness 1.4 µm and 0.1 µm undoped GaAs buffer layer, and finally 0.5 µm of

GaAs p-type doped with density of $1 \times 10^{16} cm^{-3}$ (see the evolution of the effective doping density is shown in Figure 5.5). The device has an anode length 300 µm of and thickness of 0.1 µm. The anode was deposited on the top of the active p-type GaAs layer after the preparation of the structure by etching it using ATHENA, and defined as an Ohmic contact. On other hand, the cathode has the same dimension as the anode except that it was deposited on the top of the structure without etching, and defined as a Schottky contact by adopting the Au/Ti work-function which is 4.75 eV [93]. An example of defining the distribution of deep levels is shown in Figure 5.12. The values of the deep levels are those given in Table 5.1.

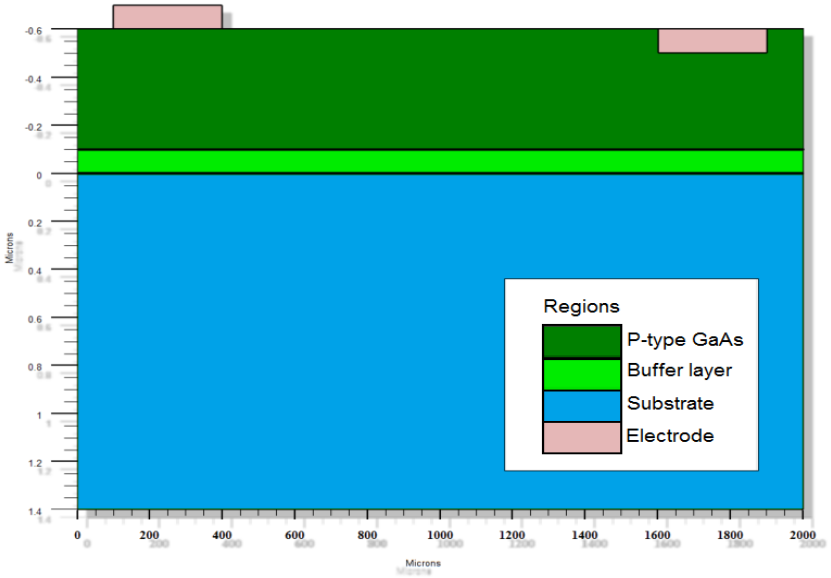


Figure 5.10: The different regions of the simulated structure.

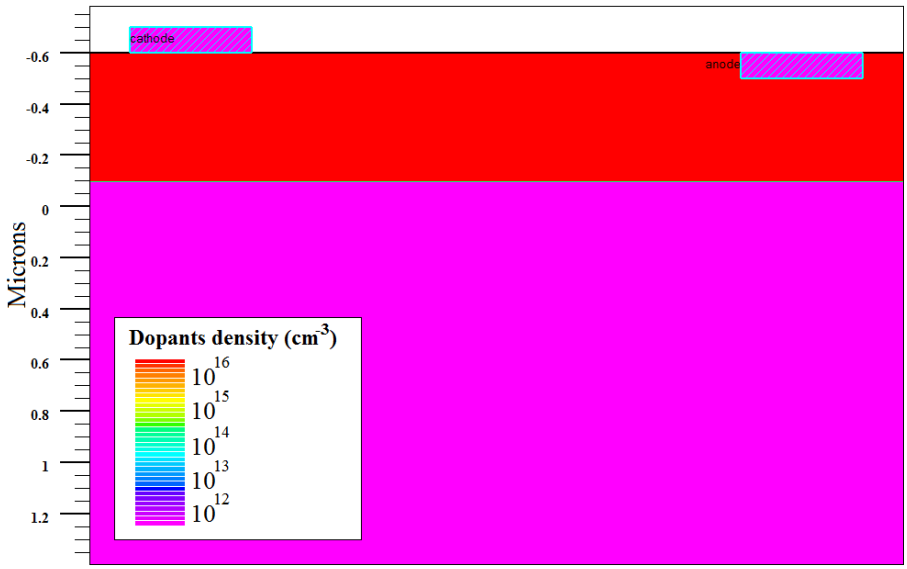


Figure 5.11: The acceptors dopant density profile of the simulated device.

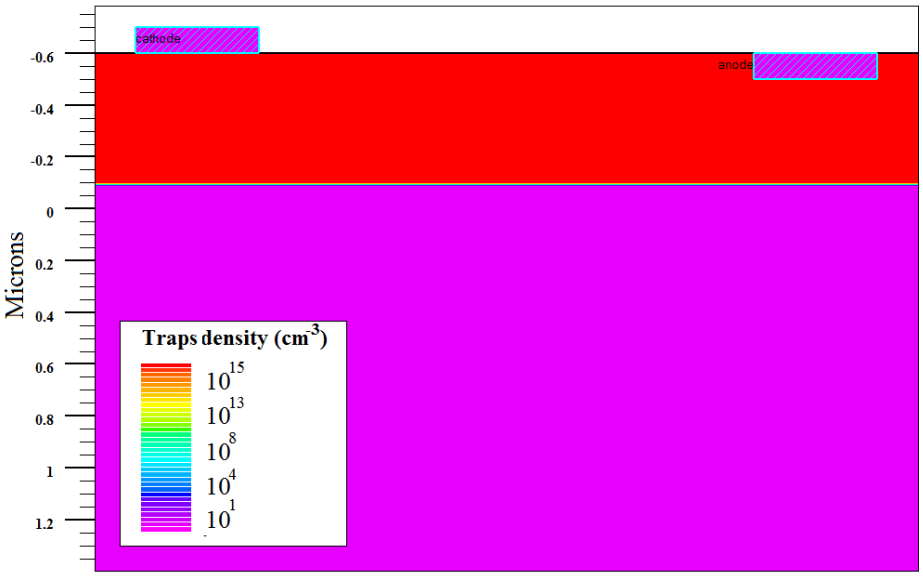


Figure 5.12: The deep levels density profile of the simulated device.

5.4. Capacitance-Temperature characteristics

In order to relate the observed dependence of the capacitance on temperature to the defects present in the samples, a simulation of three structures using SILVACO-TCAD is carried out. The three structures are similar (p-type, same regions, dimensions and characteristics); they differ only in the defects introduced. The parameters, other than the defects, are those described in section 5.2.1. The first structure is ideal, i.e. no defects are present, which will be the reference sample. The second is when only deep acceptors are present (the case of NU926). The third is when both deep donors and acceptors are present in the structure (the case of NU928). The deep levels are situated in the p-region as it is shown in Figure 5.12. Before presenting the full simulation results on these devices some preliminary simulation is carried out on the NU926 sample since it has the more complicated C-T and C-V shapes.

5.4.1. Models

After the construction of the device's structure, the next important step is to define the appropriate models for the simulation. For that purpose, the simulation will be started using the basic models "`fldmob evsatmod=1 hvsatmod=1 srh klaaug`" (see chapter 4). After that, the appropriate models which have an effect on the capacitance-temperature characteristic will be added successively. This will make the simulation more difficult but closer reality. At this level the most important criteria to satisfy is the capacitance curve shape

not its value. Figure 5.13 shows the capacitance versus temperature of the (311)A sample when different models are considered.

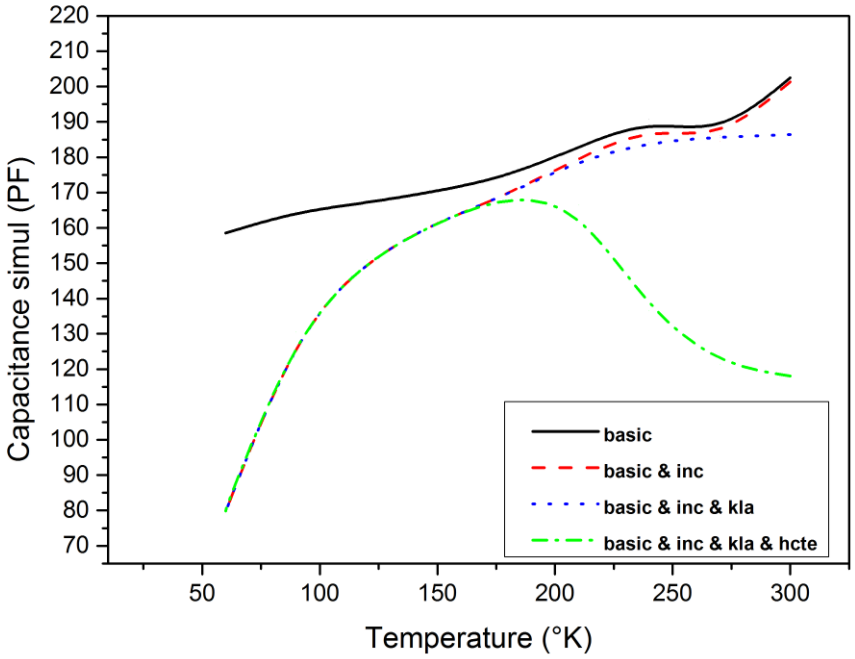


Figure 5.13: The simulated capacitance-temperature characteristic using different models.

The basic models don't account the ionization of the dopant with temperature. Instead, it considers the ambient temperature dopant's density as a constant for all temperatures. In this case the temperature has no effect on the capacitance. On the other hand incomplete model is temperature dependent since the effective doping density is related to the temperature as it explained previous in chapter 4.

The final model combination of bipolar, incomplete, Klassen and the heat model gives the closest shape of the capacitance temperature curve to the real characteristics of the NU928 sample. This model will be adapted for the remaining of the work.

5.4.2. Traps parameters

As it was seen in chapter 4 (section 4.5.1.2), there are some parameters that define deep traps in ATLAS. For the sake of clarity they are mentioned again here: they are the activation energy, the density, electrons and holes capture cross section and finally degeneracy. The experimental data which are extracted from DLTS (Table 5.1 and Table 5.2) do not offer all

these information. In fact, the electrons capture cross section and the degeneracy factors are unknown. These two parameters are related to the nature of the defects. As mentioned in the experimental results section it is difficult to ascertain the origin of the observed defects, which could be due to complexes involving silicon atoms, background impurities, and defects related to the growth conditions. So, further experimental studies are required in order to shed some light on the nature of these defects. This is one of the inconveniences of experimental work.

Simulation is of great value in this respect. In simulation, the degeneracy factor and the electrons capture cross will be taken as unknowns, and will be scanned to define their best values to give comparable simulation to experimental measurements.

5.4.2.1. Electrons capture cross section

In DLTS characterisation and for deep levels only the capture cross section for majority carriers can be evaluated. However, in SILVACO capture cross sections for both types of carriers (minority and majority) are required. Therefore it is important to study the influence of the non-evaluated capture cross section for minority carries on the simulated results. Due to the acceptor nature of the defects, their capture cross section for holes (σ_p) have values smaller than that of electrons (σ_n). in the particular case of gallium arsenide none of the characterized traps appears to act as a recombination centre, that is to say, a centre having large capture cross-sections for both electrons and f holes [94]. Therefore, the ratio (σ_p/σ_n) is scanned, keeping the capture cross section for holes constant at the value evaluated by DLTS, from 1 to 10^4 to reveal its effect on the simulated results. This effect is shown in Figure 5.14. It can be observed that the capture cross section for electrons does not affect the simulated capacitance. This may be due to the semiconductor P-type nature where the electrons density is much smaller and therefore negligible compared to that of holes.

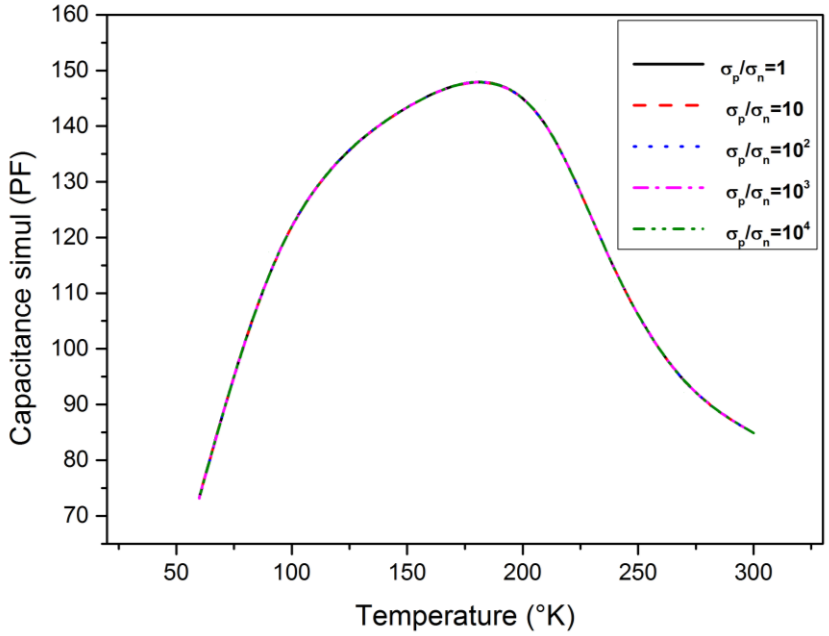


Figure 5.14: The simulated capacitance temperature characteristic in presence of deep acceptor traps with different electrons capture cross section values.

5.4.2.2. Degeneracy factor

Another factor which cannot be evaluated by DLTS measurement is the degeneracy factor (*g*). The degeneracy factor represents the number of carriers which can be captured by one trap. Its importance lies in the fact it may play a role comparable to that of the trap's density to some extent. Again in SILVACO it is a required value. Therefore it is very important to evaluate its effect on the simulated results. The degeneracy factor is swept from 2 to 8 and is shown in Figure 5.15. It is clear that the slope of the capacitance decrease (after the peak) increases with increasing degeneracy factor (). On the other hand, the degeneracy factor does not affect the capacitance at low temperatures (the first part of the graph where the capacitance increases). This behaviour can be considered as a first proof of the responsibility of the defects on the capacitance-temperature strange behaviour. Figure 5.15 shows also that the best value of the degeneracy factor which gives the best comparison to measurements is 2. This is clarified by the insert in the figure where the capacitance scale is extended to show the nonphysical basis of the degeneracy factor being larger than 2.

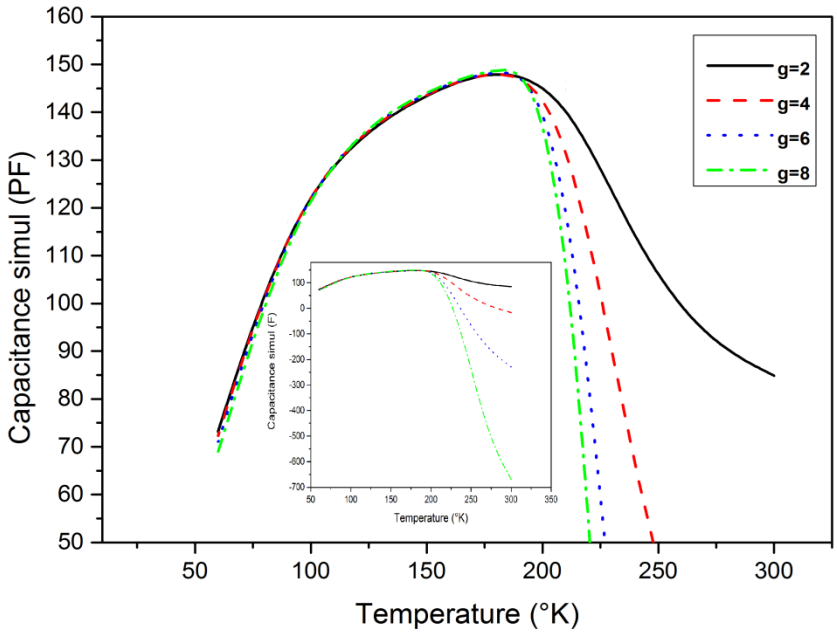


Figure 5.15: The capacitance temperature characteristic in presence of deep acceptor traps with different degeneracy factor values. The insert is an extended capacitance scale.

5.4.3. Contacts dimensions effect

After getting the desired shape of the capacitance, the values of the capacitance compared to measurements must be taken into consideration. For that purpose, the simulation was carried out for different contacts dimensions.

Since the cathode contact is deposited on the top surface of the semiconductor, in this work, we neglect the cathode's depth; therefore we only investigate its width effect. Figure 5.16 shows the capacitance temperature characteristic for different cathode widths. Here the width is changed from 25 to 400 µm. The extension of the surface between the metal and the semiconductor creates new ionized charges therefore increases the capacitance values, as we can see in the Figure 5.16. It is clear that the best width to be adopted is 300µm.

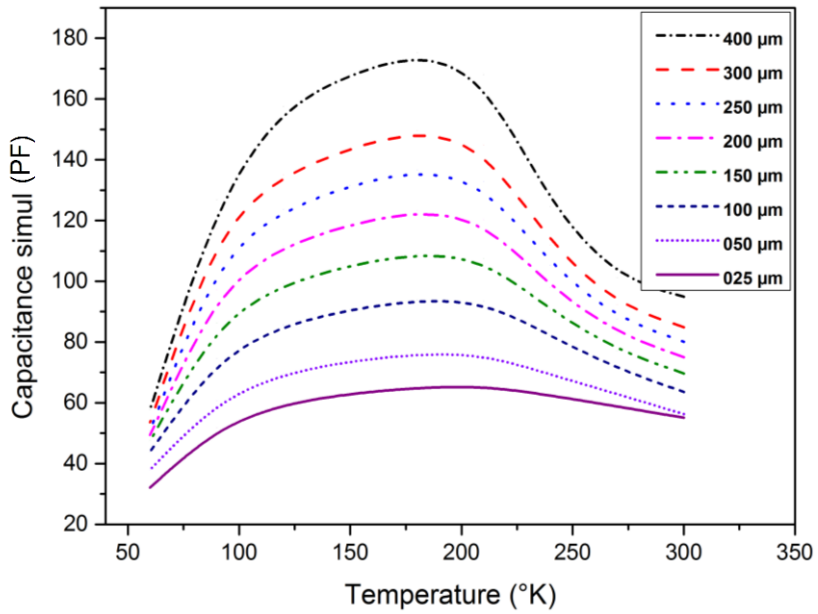


Figure 5.16: The simulated capacitance-temperature characteristic for different cathode widths.

5.4.4. Summary

The simulated dependence of the capacitance on temperature, compared to measurements, at a reverse bias of 0 V is shown in Figure 5.17 (a), (b) and (c) for the reference, (311)A and (211)A samples, respectively.

When no defects are present (reference sample) the capacitance increases monotonically as expected and predicted by the standard model of a simple diode eqt.(5.1). The increasing rate is faster at low temperatures where the shallow doping level is still ionizing. At high temperatures, the increase slows down since most of the shallow level is fully ionized.

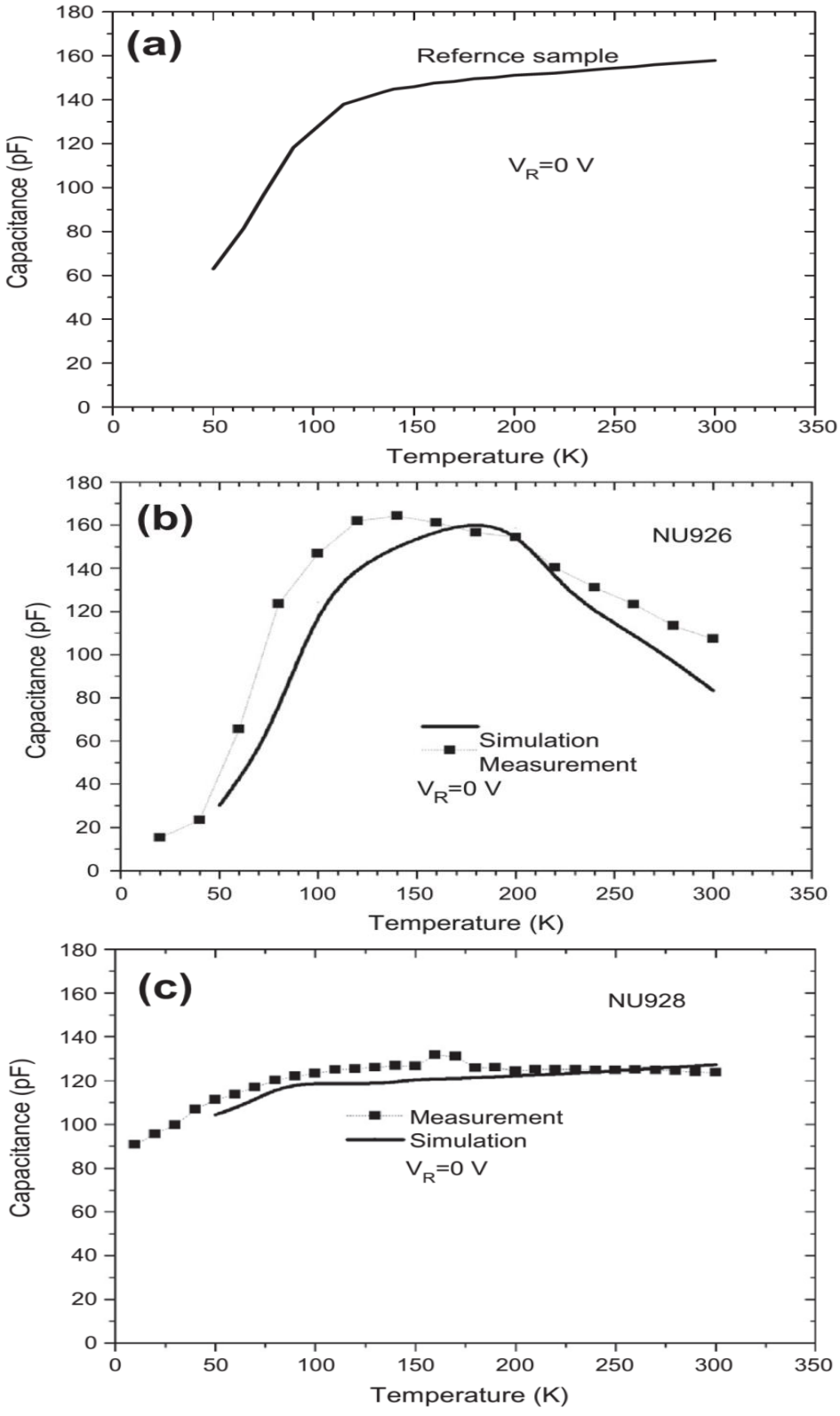


Figure 5.17: The simulated capacitance–temperature characteristics for three samples: in the absence of deep levels [(a), reference sample], in the presence of deep acceptors [(b) (311)A sample (NU926)] and in the presence of deep acceptors and donors [(c), (211)A sample (NU928)].

When only deep acceptors are present the capacitance initially increases with increasing temperature. This is because the shallow level ionizes faster than the deep acceptors and hence the Fermi level moves down. At a certain temperature the deep acceptors ionization becomes so important that the Fermi level moves up and the ionized shallow level is reduced. The overall effective density of charges is reduced and the capacitance decreases. This is the point where the capacitance reaches its maximum. From this point the deep acceptor continues to ionize and the Fermi level moves upwards leading to a decrease in the ionization of the shallow level and an increase in the deep level ionization. This is the case of NU926 [(311)A sample] where only hole deep levels (deep acceptors) are present.

For the third sample both deep donor and acceptors are present. It is worth mentioning that the deep donor has a much higher density than deep acceptors as shown by DLTS measurements. The shallow and deep acceptors are therefore compensated by the deep donors. Hence the effective doping density is reduced. The increase in temperature ionizes almost equally the deep donor and acceptors. Hence the effective doping density does not change much with temperature. Therefore the capacitance also does not change much with temperature. This is similar to the effect observed in the case of (NU928) [(211)A sample]. Therefore, the simulation results confirm the results observed experimentally.

5.4.5. Frequency effect on the capacitance–temperature characteristics

The effect of frequency on the capacitance–temperature characteristics is also simulated. This is to enhance our explanation of the relation between the C–T characteristics and the presence of different type of deep levels. It is well known that the deep levels response depends on the frequency of the alternating signal used to measure the change in the capacitance. This is because a deep level is characterized by an emission rate, i.e. a frequency. If the signal frequency is much higher than the deep level emission rate, the deep level cannot follow the signal variations which mean that the deep level does not respond to the signal variation with time. An example of the frequency effect on the capacitance–temperature relation is shown in Figure 5.18 for the case of sample NU926 where both only deep acceptors are present.

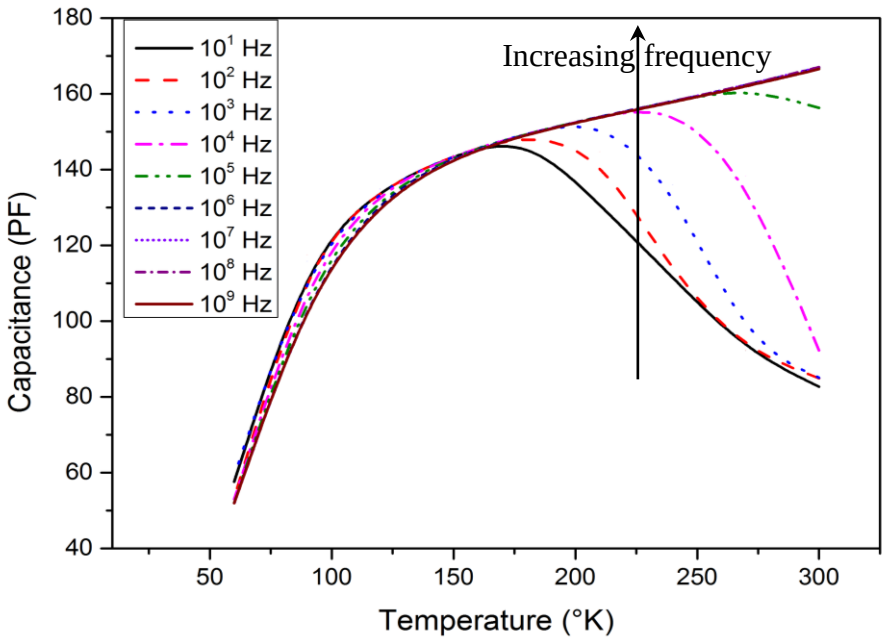


Figure 5.18: The simulated capacitance–temperature characteristics for different frequencies in the presence of deep acceptors only (311)A sample (NU926).

As demonstrated in Figure 5.18 the capacitance–temperature relationship is sensitive to the frequency. When the frequency is low the capacitance–temperature dependence has a similar behaviour as the solid line (without symbols) in Figure 5.17.b. That is deep levels are able to follow the slow changing signal with time. As the frequency increases the capacitance–temperature dependence on frequency decreases. This is because the deep acceptor cannot follow the fast changing signal with time (high frequency). The high frequency curves tend to be similar to Figure 5.17.a (that is when no deep levels are present in the sample). This also confirms that the experimentally observed capacitance dependence on temperature is due to the presence of deep traps.

The frequency effect on capacitance can be clarified by plotting the capacitance-frequency graph (Figure 5.19). Taking as example the black bold line (T=300 K) where the presence of traps effect on capacitance progressively disappears with increasing frequency, therefore the capacitance increases (first part of the graph: $f = 10 - 10^6\ hz$). In the second part of the graph ($f = 10^6 - 10^9\ Hz$) the capacitance does not change with frequency, as though the frequency has annealed the deep levels traps effect and hence behave as non-existents or negligible compared to the shallow levels. Finally, the capacitance will decrease due to high frequency, where the carriers can not follow the signal change.

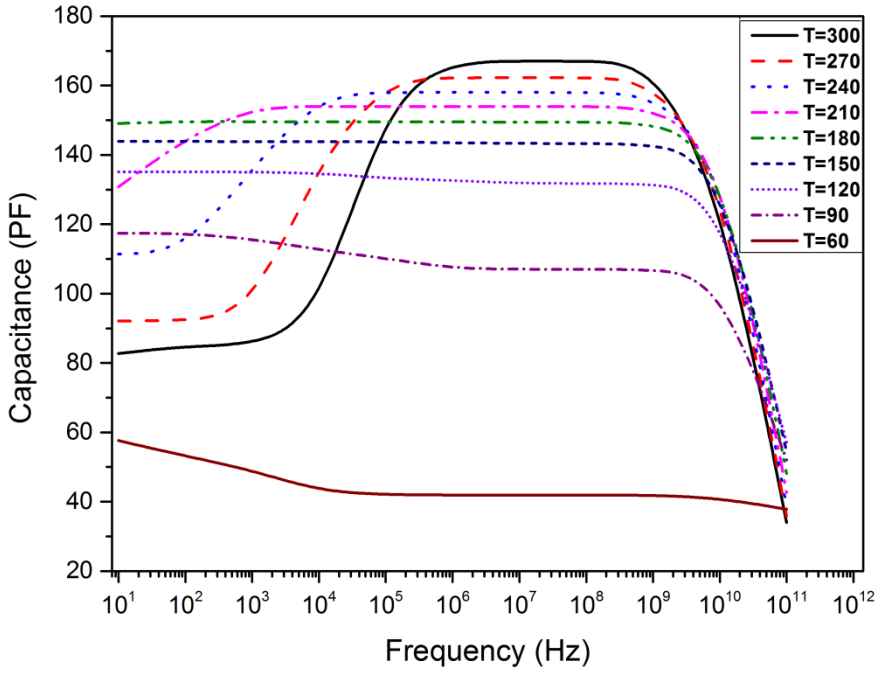


Figure 5.19: The simulated capacitance–frequency characteristics for different temperatures in the presence of deep acceptors only, (311)A sample (NU926)

5.5. Capacitance-Voltage characteristics

By confirming that the presence of different types of defects in the two samples is the main reason of the strange behaviour of the capacitance-temperature characteristics, it is logical to assume that it is also the reason of the different shapes observed in the capacitance-voltage characteristics of the two samples (Figure 5.2 and Figure 5.3).

As it can be clearly seen, the C-V characteristics are entirely different for the two devices. In NU928, the C-V characteristics have almost the usual shape for all temperatures and increase monolithically. In NU926, however, the C-V characteristics begin with the usual shape at low temperatures. As the temperature increases the C-V characteristics deviate from the usual shape and a negative differential capacitance (NDC) manifests clearly. NDC is the phenomenon where the capacitance increases for a certain interval then decreases once passed this interval. IT will be shown that the difference in the shape of the C-V characteristics of the two samples is related to the difference in the type of deep levels observed in the two samples.

The negative capacitance (NC) is not new and is frequently observed in the capacitance-voltage characteristics in structures where deep traps are present. In fact not only NDC is observed but also an apparent negative capacitance (NC). For example, Jones et al [95] reported a forward bias NC. Saadoune at al [96] used numerical simulation to relate the NC to

defects in the semiconductor diodes subjected to high dose of energetic particles such as protons and electrons. Yahia et al [97] and Korucu et al [32] related this effect to interface states and series resistance. The so-called negative differential capacitance (NDC) is another effect due to the presence of deep levels. Stuchlíková et al [34] observed that NDC increases with increasing temperature and is a characteristic of quantum well heterostructures. Kumar et al [36] also argued that NDC is the result of free electron emission from quantum states. Simulation of a three layered GaAs structure showed that the presence of deep levels produces a NDC effect [98]. Silicon implantation of GaN P-I-N photodetectors also showed a NDC behaviour, which increases with increasing temperature [33]. It is argued that this is due to defects introduced by implantation. A study of the effect of temperature on the electrical characteristics of GaAsN Schottky diodes revealed an apparent high density of traps [99] and are signalled as the cause of NDC.

5.5.1. Sample NU926

For this sample, DLTS reveals four majority deep levels (see Table 5.1) and the C-V characteristics show an NDC behaviour (Figure 5.2). In the following sections simulation will be used to find out which of the deep level(s) is (are) responsible for the NDC behaviour.

5.5.1.1. Effect of deep levels with uniform distribution on capacitance voltage characteristics

In this case it is supposed that all the deep levels as well as the shallow doping have uniform distribution within the whole volume of the p-type GaAs layer. A separate series of capacitance-voltage simulations were performed at different temperatures to show the effect of the presence of defects (**Figure 5.20**). At this point the used parameters in simulation are the same that gave the best results for the capacitance-temperature simulation.

The simulated curves show that the presence of defects not only affects the capacitance-voltage values, but also affects its shape at small reverse bias (0 – 0.5 V), where the C-V characteristics change their shape with variable temperature. While at high reverse bias (0.5 – 4 V), the presence of defects has more regular (same) effect, which is not the case for the experimental measurements.

As in the case of the C-T characteristics and in order to investigate the defects effect on the C-V measurements, different structures have been simulated using a different traps parameters such as the traps density, degeneracy factor and traps activation energy level.

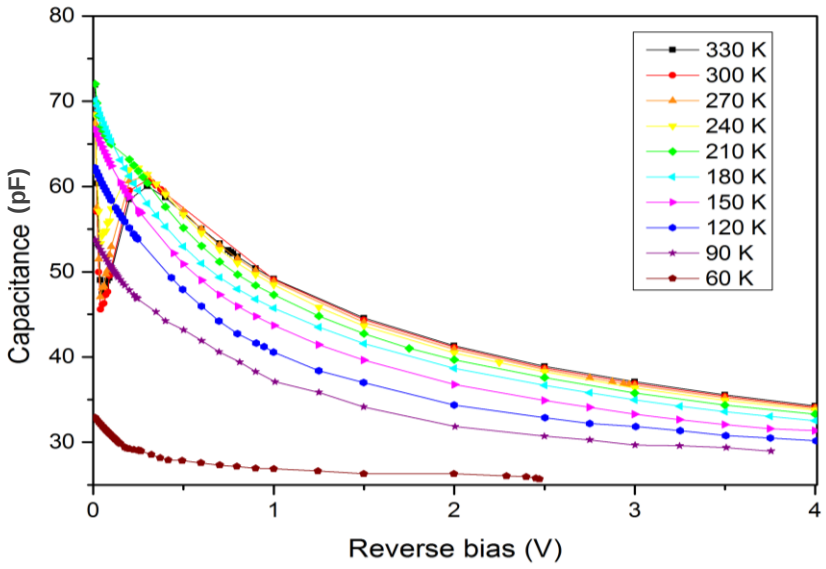


Figure 5.20: The simulated capacitance-voltage characteristics for the NU926 sample.

a. DEGENERACY FACTOR EFFECT

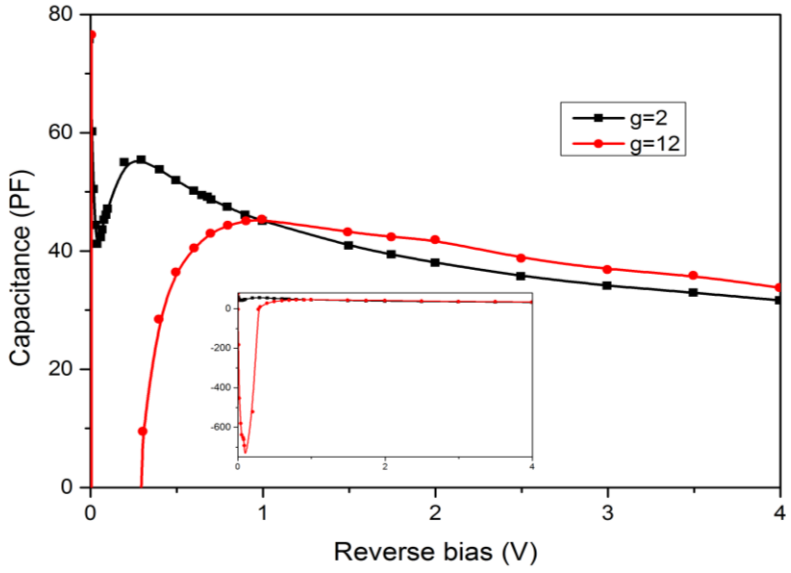


Figure 5.21: The simulated capacitance-voltage characteristics of NU926 sample for different degeneracy factor.

As we saw in the capacitance-temperature, the variation of the degeneracy factor can amplify the traps effect. This makes the degeneracy factor one of the most important parameters that may cause a huge change to the capacitance-voltage characteristic. In this case two values of degeneracy factor are simulated. This is shown in Figure 5.21.

b. TRAPS DENSITY EFFECT

For better understanding of the effect of the traps present in NU926 sample, different simulations have been done using different traps densities. Each time a high density is used for one level ($10^{17}\ cm^{-3}$), and fixed densities for the others (the real values shown in Table 5.1).

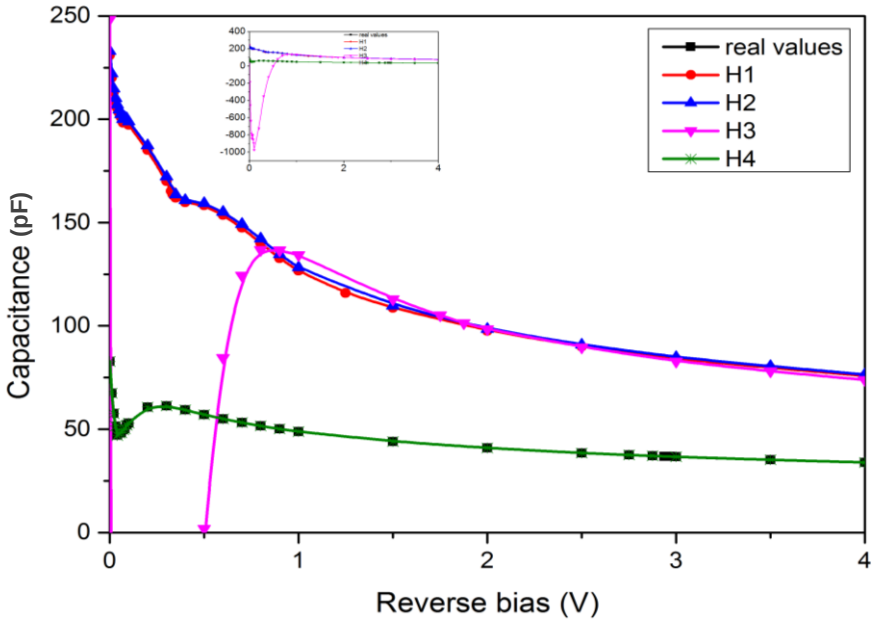


Figure 5.22: The simulated capacitance-voltage characteristics of NU926 sample: real density values of all levels (squares), high density of: H1 (circles), H2 (up triangles), H3 (down triangles) and H4 (stars).

The results show that the first and the second levels (shallowest: H1 and H2) have almost the same effect as the shallow levels (dopants: see 5.5.1.2), where their presence increases the capacitance without affecting its shape. That if we consider that the irregularities appeared at V=0.4 V are due to the presence of the other defects with relatively small densities. On the other hand, by increasing the third level density (H3) which is deeper than the precedents, the

capacitance shows a strange behaviour at small reverse biases, while it shows the same behaviour (as H1 and H2) for high reverse bias values. Finally, the deepest level (H4) does not affect the capacitance, and this is due to its large activation energy (see **Figure 5.22**).

c. TRAPS ENERGY LEVEL EFFECT

The different response of the capacitance to each level of the samples NU926 showed in Figure 5.22 leads to one question: what are the other responses to other levels? Or in other words, what is the effect of the traps energy level on the capacitance. In order to answer this question a simulation of structure has the same parameter as the NU926 sample (except traps) has been done. In this structure only one trap was introduced, by changing its energy level through the gap, its effect on capacitance is shown in Figure 5.23.

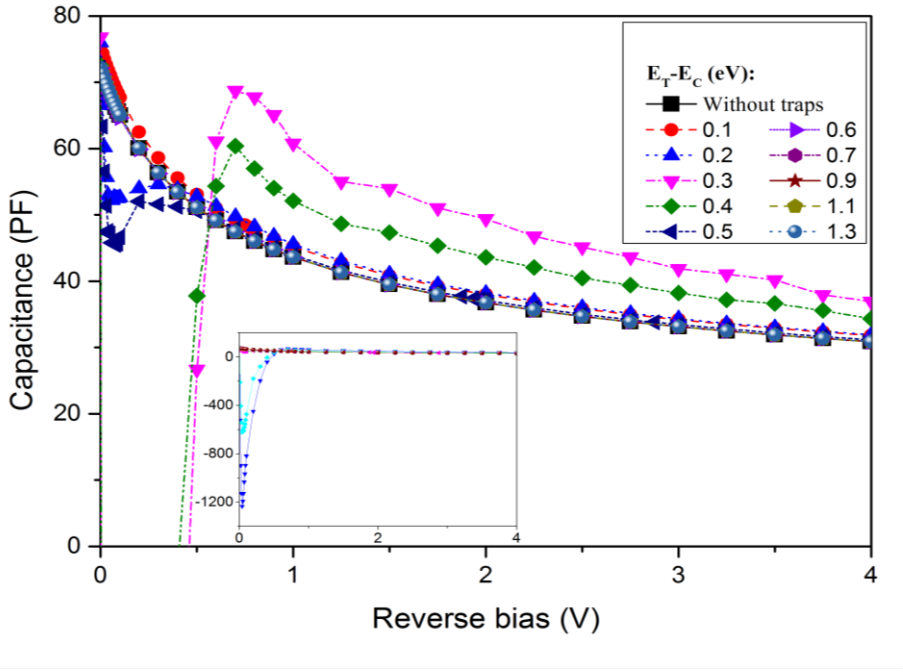


Figure 5.23: The simulated capacitance-voltage characteristics in present of one acceptor trap at different energy positions.

The curves can be divided into three groups according to the trap effect. In the first group the trap increases the capacitance in a regular manner along the reverse bias, in this case the capacitance has an ideal shape (see equation 2-42).

The second group starts from $E_T - E_C = 0.2\ eV$ to $E_T - E_C = 0.6\ eV$, in this interval the capacitance takes a strange shape where it starts with normal values compared to the ideal

capacitance then it decreases sharply in all cases. In fact it even takes a negative values in some cases ($E_T - E_C = 0.4\ eV$ and $E_T - E_C = 0.5\ eV$). After that (~0.8 V) it returns to the usual shape compared to the ideal capacitance with a huge increase.

Finally, the third group ($E_T - E_C = 0.6\ eV$ to $E_T - E_C = 1.3\ eV$). The levels belong to this group have a high activation energy, so the release and capture processes are not easy to occur. Thus, their effect can be neglected. Therefore it can be concluded that the uniform presence of one trap cannot cause an NDC no matter where its energy position.

5.5.1.2. Effect of shallow levels with uniform distribution on capacitance-voltage characteristics

After confirming that the presence of defects with uniform distribution is not the main reason of the convexity observed in the experimental results, the next suspects are the dopants. To study the effect of dopants on capacitance voltage characteristics in presence of traps, the idea is to simulate the NU926 sample with different dopants densities. Figure 5.24 presents the simulated capacitance-voltage characteristics with different dopants densities from 10^{15} to $10^{17}\ cm^{-3}$.

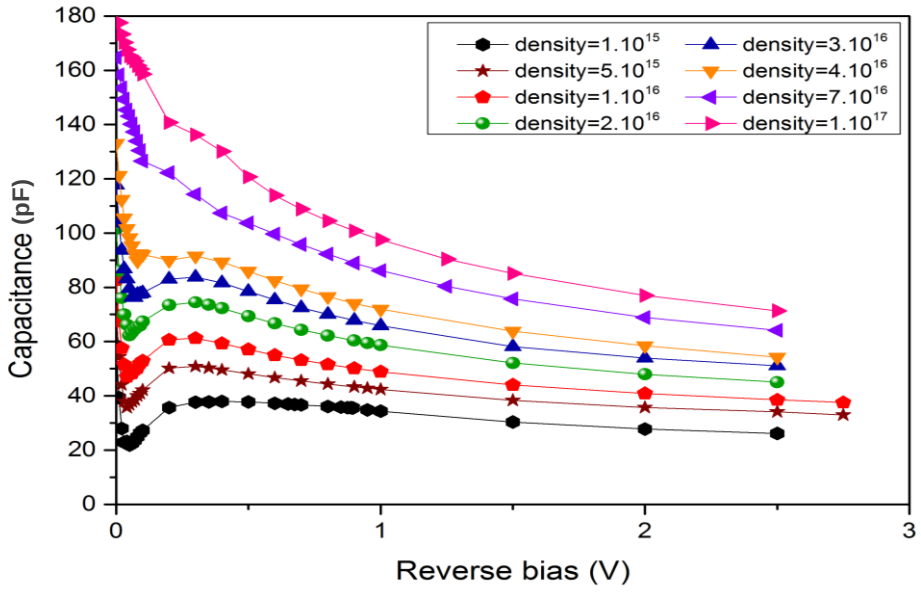


Figure 5.24: The simulated capacitance-voltage characteristics with different dopants densities.

The first observation is the increase of the capacitance with increasing dopants density, which is due the decrease of the depletion region which is due to high density of ionized atoms (see

equation 2-41, 2-43). The second is the irregularity observed at small reverse biases; this is due to the presence of defects. We can see that this irregularity is considerable for small dopants densities (black circles), but it slowly disappears with the increase of dopants density (pink triangle). Therefore it can be concluded that the density of the shallow dopants is not responsible for the NDC behaviour.

5.5.1.3. Non-uniformity hypothesis

The simulation shows that neither shallow levels (dopants) nor deep levels (traps) which are uniformly distributed in the structure can be the main reason of the observed convexity.

As we can see in the capacitance-voltage plot of this sample (**Figure 5.2**), the convexity appears after few volts of reverse bias (~1 to 2.5 V). In addition to the direct relation between the capacitance and the fixed charges in the structure, the depletion region extends with the reverse bias, which leads to the hypothesis of spatial irregularity (non-uniform distribution).

Before adopting some non-uniform distribution, the depth reached by the depletion region at the convexity voltage must be defined. For this purpose a simulation of the NU926sample was carried out using the old parameters (uniform traps and dopants distribution). The expansion of the depletion region at different reverse voltages is presented in Figure 5.25.The depletion region extends with increasing reverse bias, which agrees with theory. At $V = 2\,V$ the depletion region reaches $\sim 0.4\ \mu m$ from the surface. This depth will be adopted in the next simulations as the depth where the irregularity of the parameters occurs.

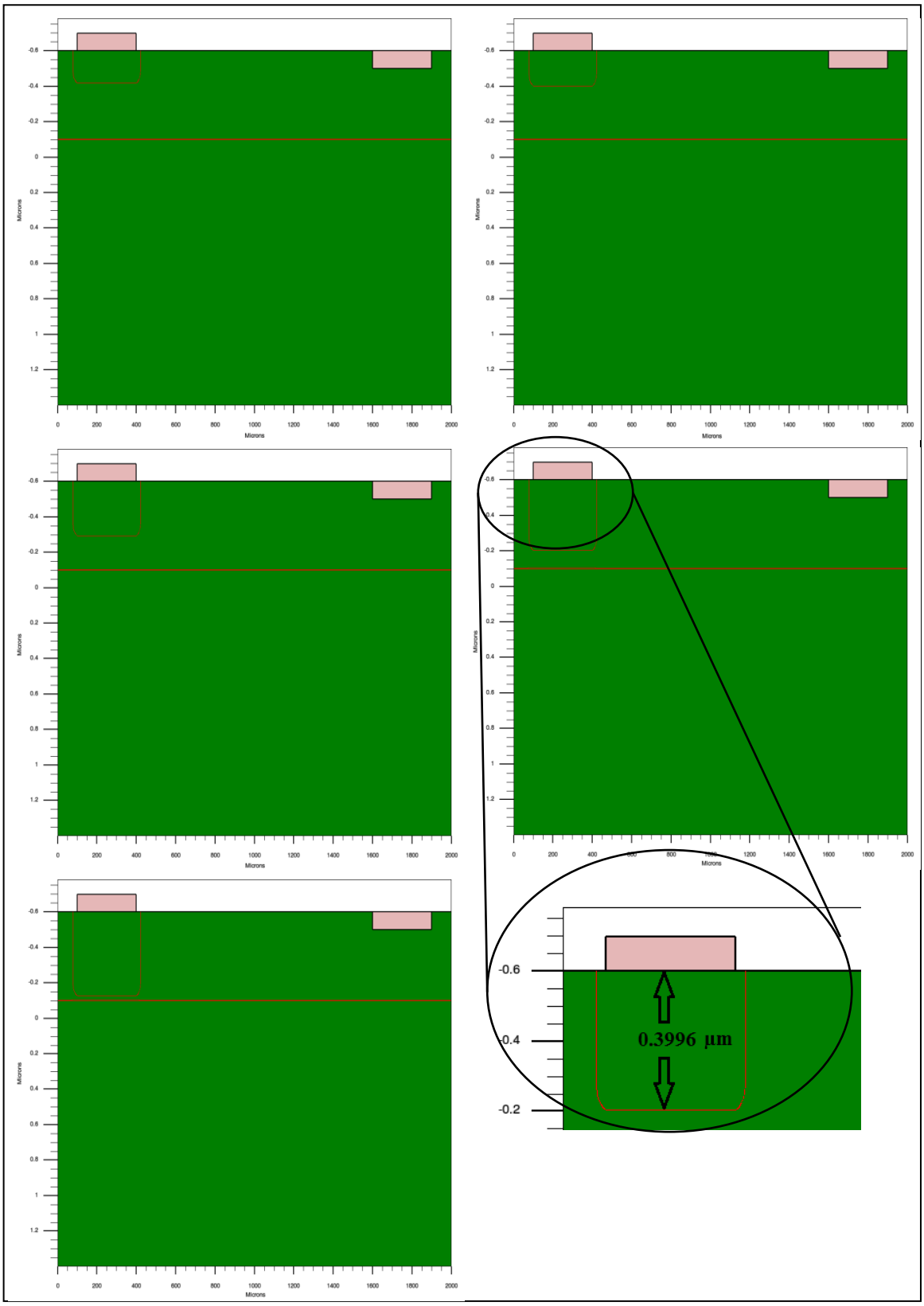


Figure 5.25: The expansion of the depletion region of the sample NU926 for different biases.

There are a lot of possibilities of non-uniform distribution. In this work we will use two types:

- The first one is the simplest distribution; it consists of two regions with different densities. The first one starts from the surface and has a depth of $0.4\ \mu m$. The second is the rest of the active region of the sample.
- The second distribution is smoother compared to the first; it is based on a Gaussian distribution (see equation (5.2)). In this case the maximum concentration is positioned at the surface, so it produces a decreasing gradient from top to the bottom of the sample.

$$N(y) = N.peak * \left[-\left(\frac{y-peak}{char}\right)^2 \right] \qquad (5.2)$$

Where

$N(y)$" is the traps concentration distribution along y direction (depth), $N.peak$" is the peak concentration, $peak$ " is the peak position and $char$ " is the principal characteristic length which equals the square root of two times the standard deviation of the Gaussian function.

- The third one is also based on Gaussian distribution. But in this case, the maximum concentration is positioned in the bulk of the sample, so it produces a peak of high density. In this case, the used distribution is complex; it consists of two different distributions: the old uniform distribution and the Gaussian distribution. So the total is the multiplication of these two density distributions. To get a better visualization about the used structure, a simulated example is illustrated in Figure 5.26. The parameters used in this example are $N.peak = 10^{18}\ cm^{-3},\ peak = -0.2\ \mu m,\ char = 0.03$.

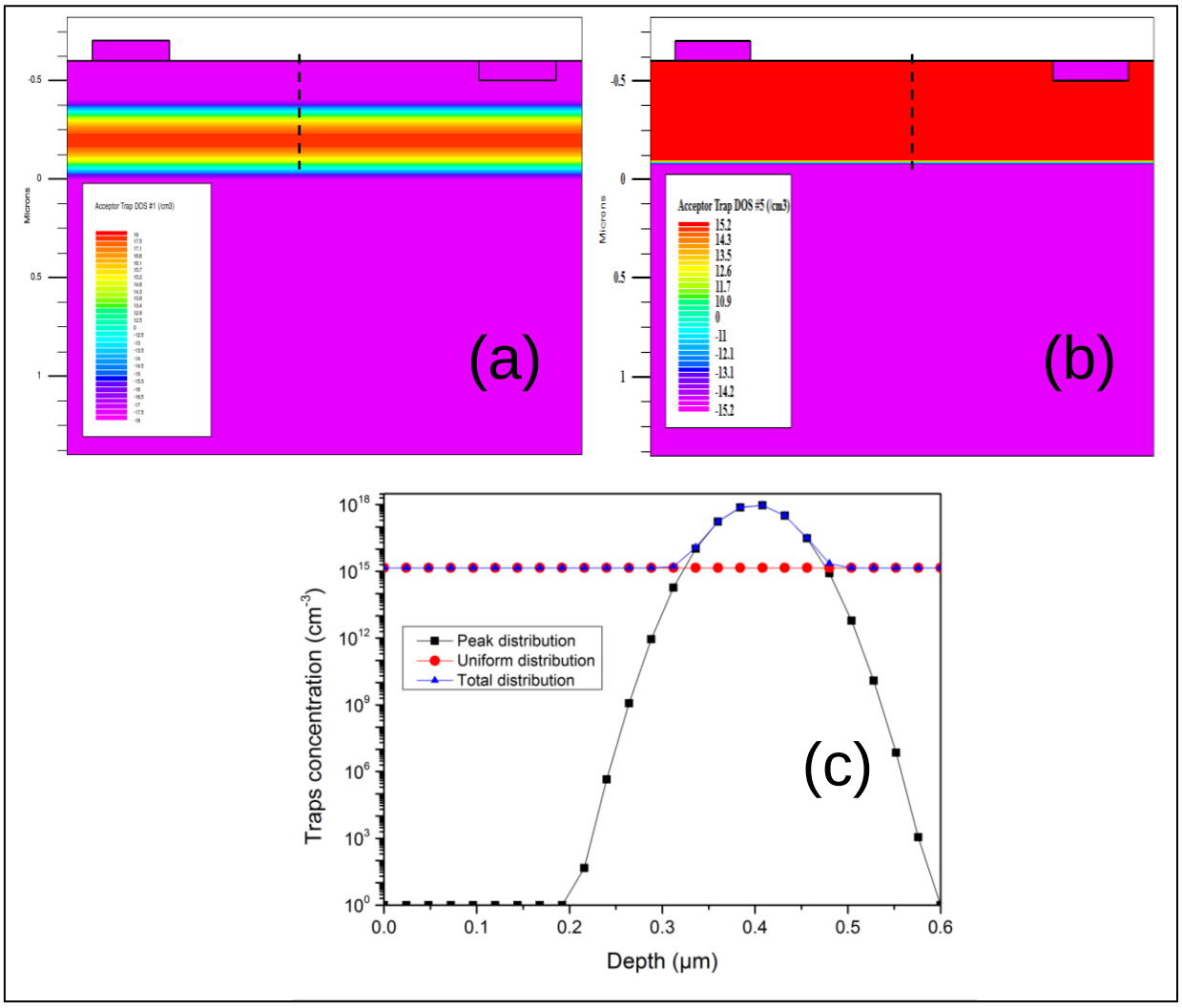


Figure 5.26: An example of non-uniform distribution based on Gaussian function used in simulation: a. Gaussian distribution, b. uniform distribution, c. vertical cut (as shown in a. and b. by dashed) shows the profile of both distributions and the total distribution.

5.5.1.4. Effect of the non-uniformity distribution of shallow levels on the capacitance voltage characteristics

a. Different regions with different densities distribution

To study the effect of non-uniformity of dopants a simple non-uniform distribution consisting of two regions, the first one has a depth of 0.4µm from the surface followed by the second with 0.1 µm is studied (see Figure 5.27).

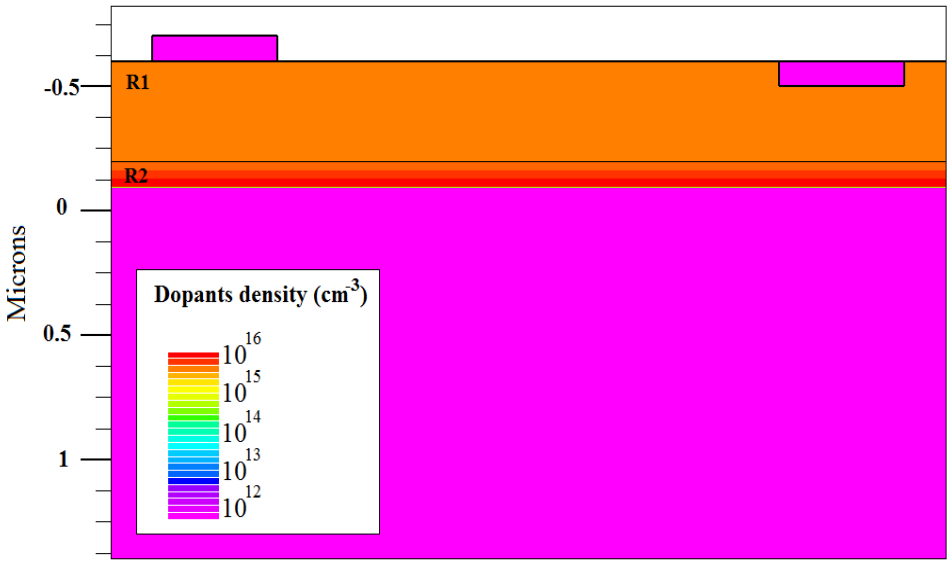


Figure 5.27: The Acceptor dopant concentration distribution in two different regions (R1 and R2).

This distribution makes the depletion region encounter a high density region after few volts of reverse bias, which may affect the capacitance. So there are two possibilities The first is changing the first region with values smaller than the old dopants density ($8 \times 10^{16}\ cm^{-3}$) and fixing the second region at this value (see Figure 5.28). The second is to fix the first region at the old value and changing the second with values bigger than the old dopants density (see Figure 5.29).

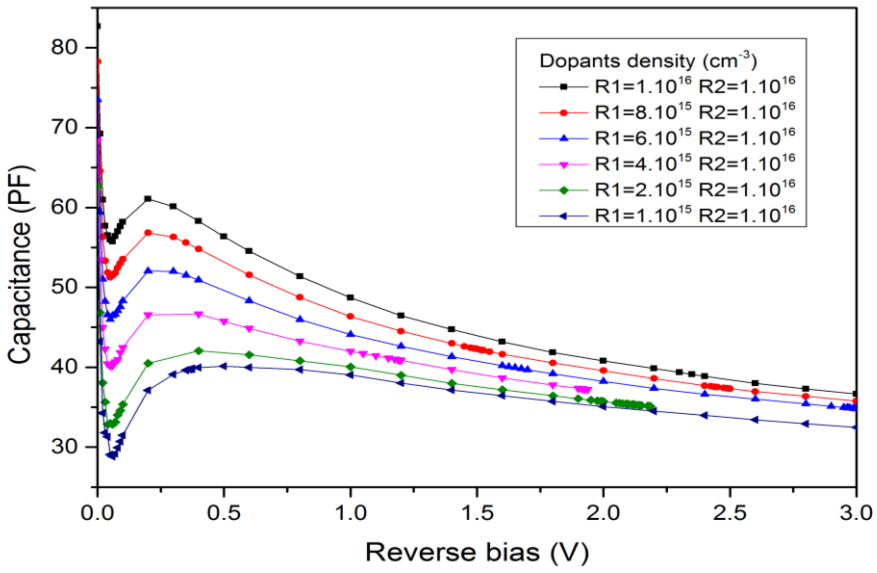


Figure 5.28: The simulated C-V characteristics with different dopants densities in the first region (R1).

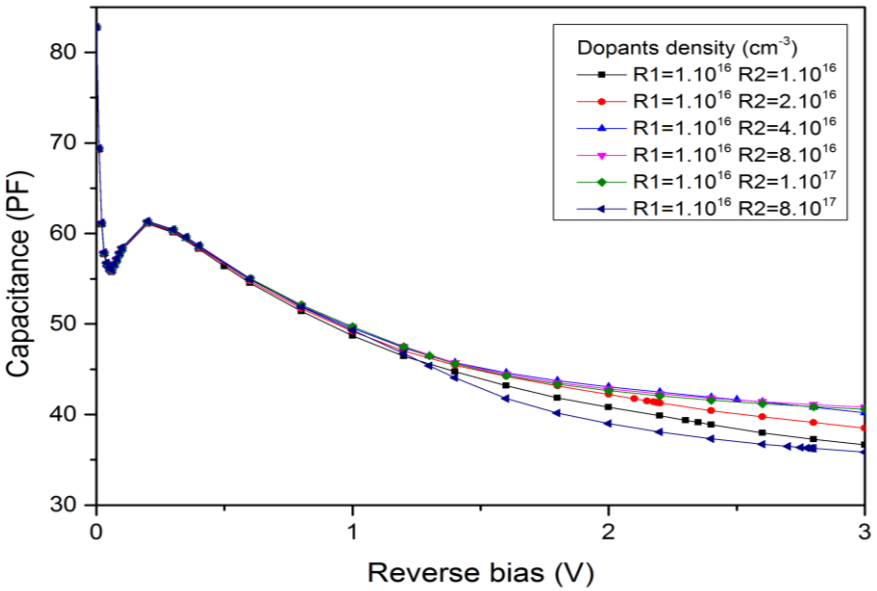


Figure 5.29: The simulated C-V characteristics with different dopants densities in the second region (R2).

For the first possibility (Figure 5.28) the changes around the cathode affect the capacitance in the first part (small reverse biases), where the capacitance decreases clearly by decreasing the first region dopants density. At high biases the capacitance also decreases with decreasing dopants density, but by small values compared to the first part. The second possibility agrees well with hypothesis, as it is shown in Figure 5.29, the capacitance changes its values after few volts of reverse bias. But, this structure does not show a NDC which is observed in the experimental results.

b. PEAK DISTRIBUTION

In this section, the Gaussian function was used to create a peak of high dopants density at a distance of 0.4 μm from the surface for different structures. To get an idea about these structures, an example is shown in Figure 5.30. The peak in this example has a maximum concentration of $4.10^{18}\ cm^{-3}$ and a principal characteristic length of 0.006.

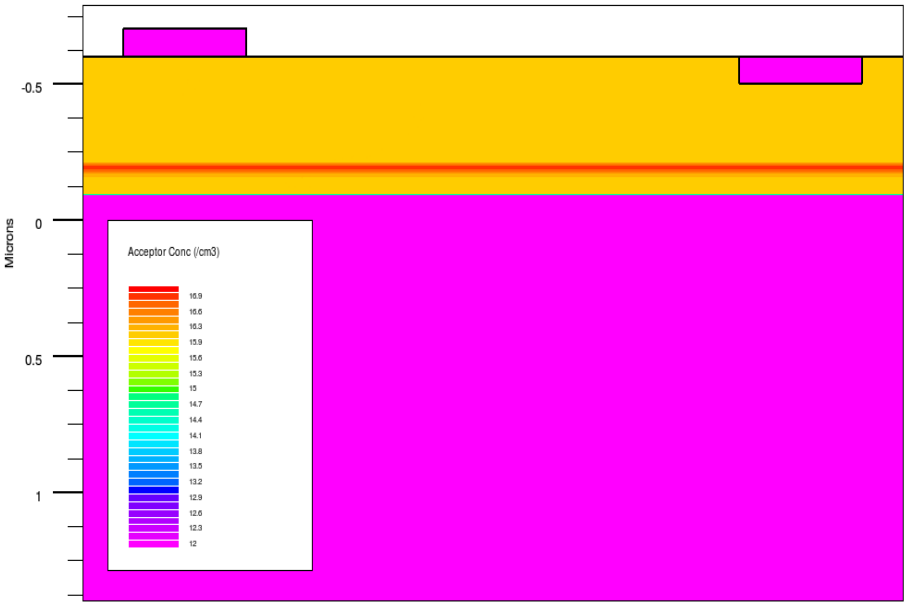


Figure 5.30: The Acceptor concentration distribution with peak density.

In order to study the effect of the presence of a peak with a high dopants density on the capacitance, two different simulations were done: the first one was dedicated to study the effect of the peak's density by varying it and fixing the characteristic length at 0.006, the results are presented on (Figure 5.31). The capacitance is affected by the presence of a the peak after few volts as was expected, where it starts to increase with increasing density till it reaches the highest values at density of $8 \times 10^{17}\ cm^{-3}$, then it decreases again.

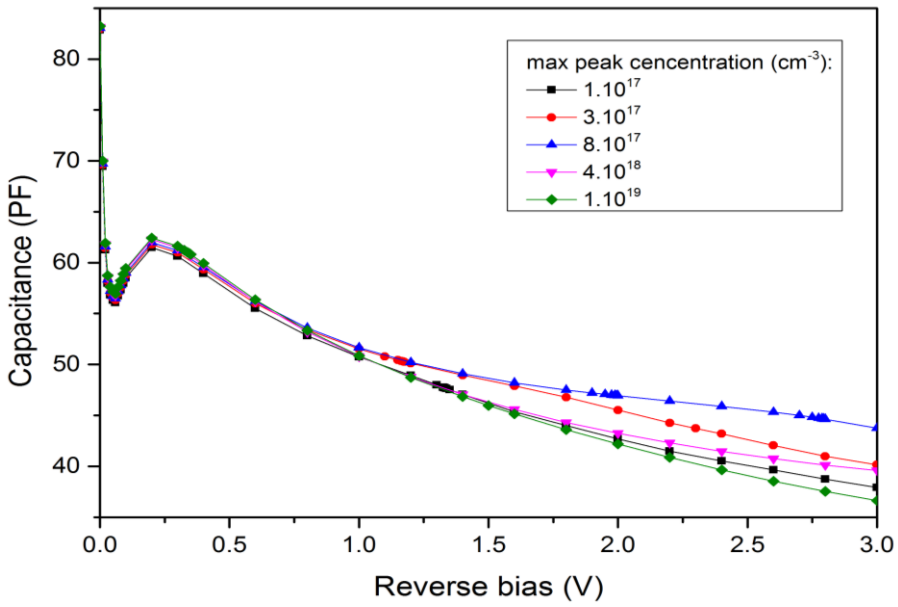


Figure 5.31: The simulated capacitance-voltage characteristics in presence of dopants density peaks with different densities.

The second part is the inverse; where the peak's density was fixed at $3 \times 10^{17}\ cm^{-3}$ and the characteristic length was varied to study its effect on capacitance (Figure 5.32). The results do not show considerable changes; where the capacitance increases by small values with increasing characteristic length. This is due to the increase of dopants density with increasing peak width.

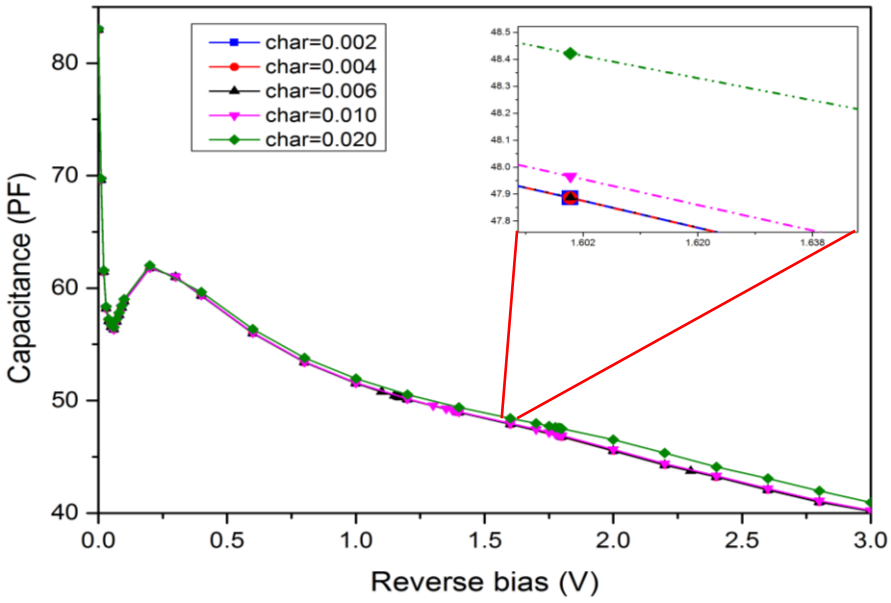


Figure 5.32: The simulated capacitance-voltage characteristics in presence of dopants density peaks with different characteristic length. The insert is a zoomed C-V in order to clarify the differences.

It is clear that the capacitance is affected by the form of dopants density distribution, but no one of the suggested samples has comparable capacitance-voltage characteristics to experimental results. Thus it can be concluded that the dopants are not the main reason of the convexity appeared in the measured C-V.

5.5.1.5. Effect of deep levels with non-uniform distribution on capacitance-voltage characteristics

Traps have a huge effect on capacitance, whether on its values or its shape as demonstrated by precedents simulations, which have been done using a uniform traps density distribution. Basing on these results we can expect that the non-uniformity of traps density will cause a bigger changes to capacitance compared to dopants.

a. GRADIENT DISTRIBUTION (FROM TOP TO BOTTOM)

The first suggested structure has the same parameters, except traps distribution, where the uniform distribution is replaced by a decreasing distribution from the surface to substrate. In this case the peak of the used Gaussian distribution has is positioned at the surface. Using different characteristic lengths we can control the expansion of traps distribution as shown in Figure 5.33.

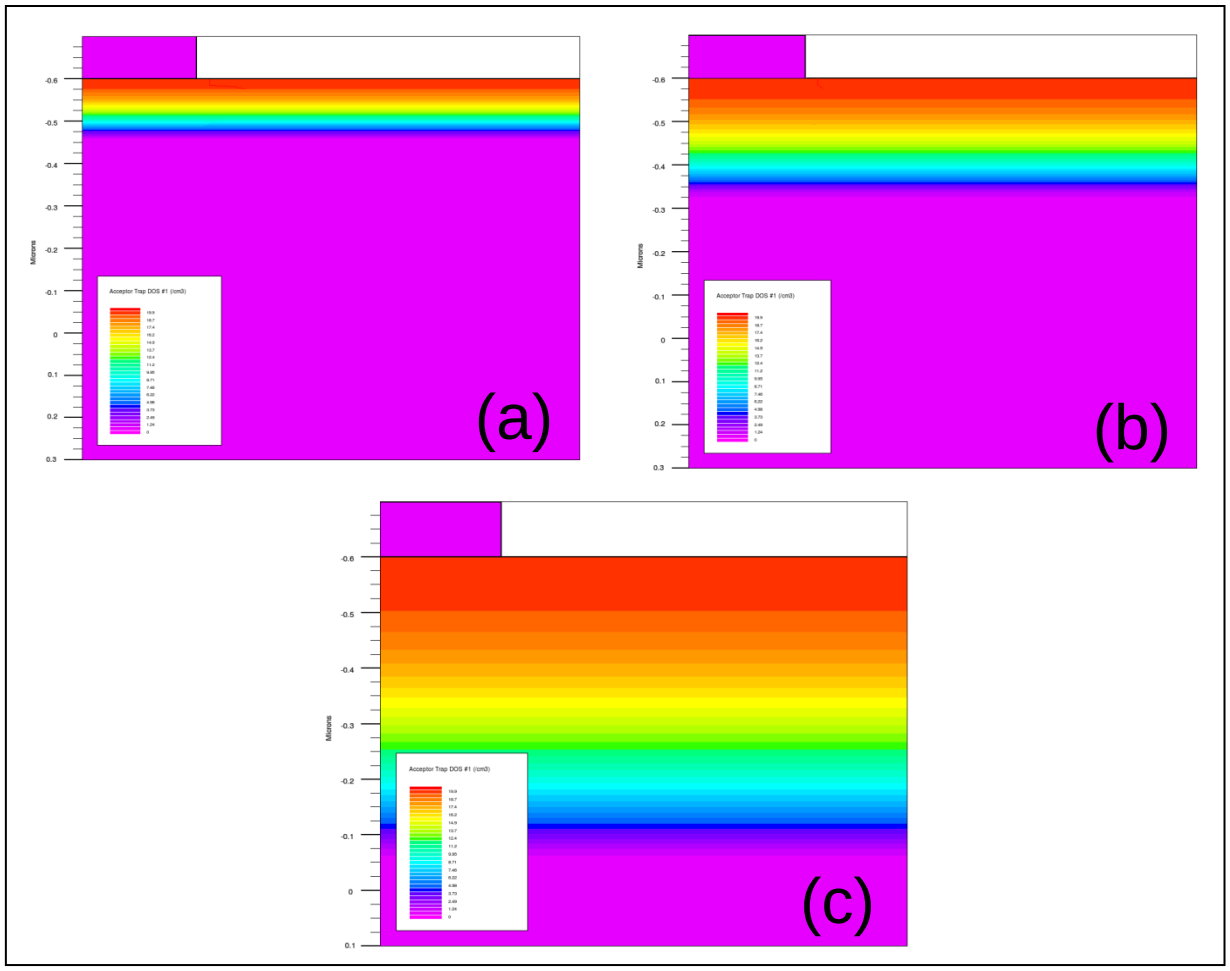


Figure 5.33: Traps density decreasing distributions using Gaussian peak at surface with different characteristic: a. char=0.02 b. char=0.04 c. char=0.08.

The first observation in Figure 5.34 is about the capacitance values at small biases, where it increases with increasing characteristic length; this is due to the expansion of high density region near to surface as it is shown in Figure 5.33.

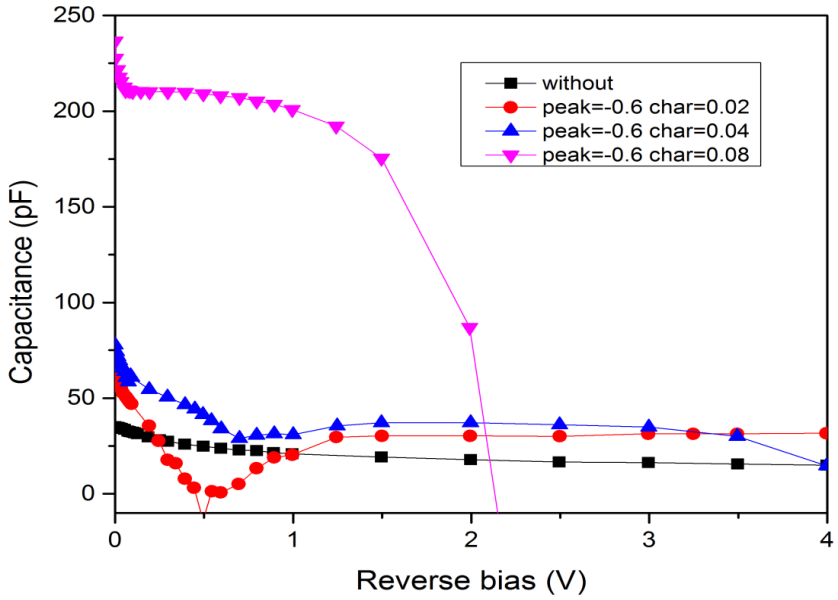


Figure 5.34: The simulated capacitance-voltage characteristics with traps density decreasing distributions using Gaussian peak at the surface.

b. PEAK DISTRIBUTION

The second suggested idea is to add a peak of high traps density at a certain distance from the surface in addition to the uniform distribution. As it is explained in equation (5.2), the Gaussian distribution has three parameters to adjust: peak density, peak position and characteristic length. These three parameters will be scanned in different simulation in order investigate the traps peak density distribution effect on capacitance.

In order to study the characteristic length, different structures were simulated by fixing the peak position at 0.4 μm and their densities at $10^{18}\ cm^{-3}$, and varying the characteristic length from 0.002 to 0.030. The used structures in simulation are illustrated in Figure 5.35.

NB in this figures only the traps peak density (not the total density see Figure 5.26) is presented, in order to get a clear vision of the peak.

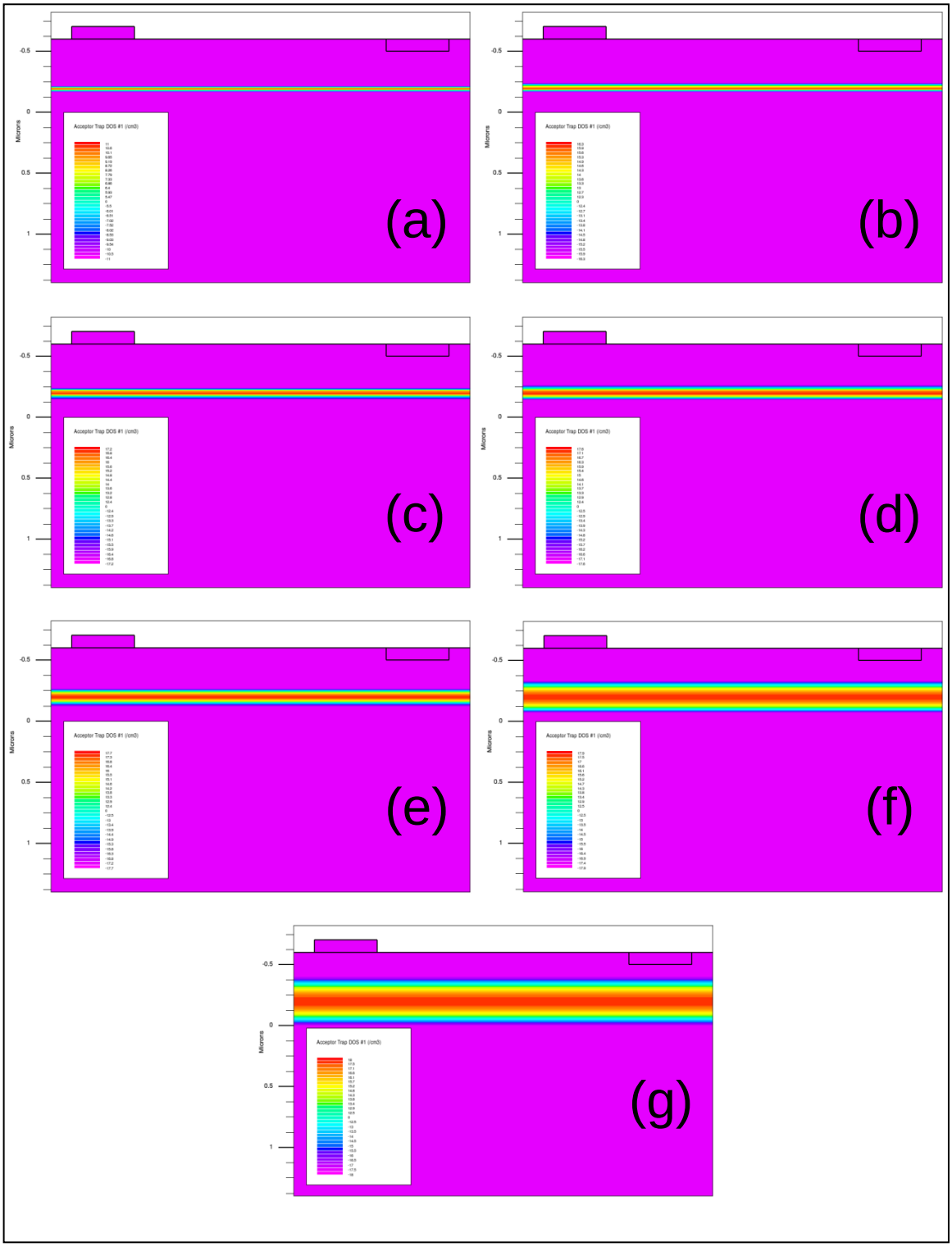


Figure 5.35: Structures in presence of traps peak density with different characteristic length: a. char=0.002 b. char=0.004 c. char=0.006 d. char=0.008 e. char=0.010 f. char=0.02 g. char=0.03.

The results presented in Figure 5.36 shows the effect of characteristic length on capacitance. As it is shown the increase of characteristic length value increases the peak's width, thus the traps density increases, which add some negatively charged ions leading to increase the capacitance. This is happened after few volts of reverse bias, when the depletion region approaches the peak.

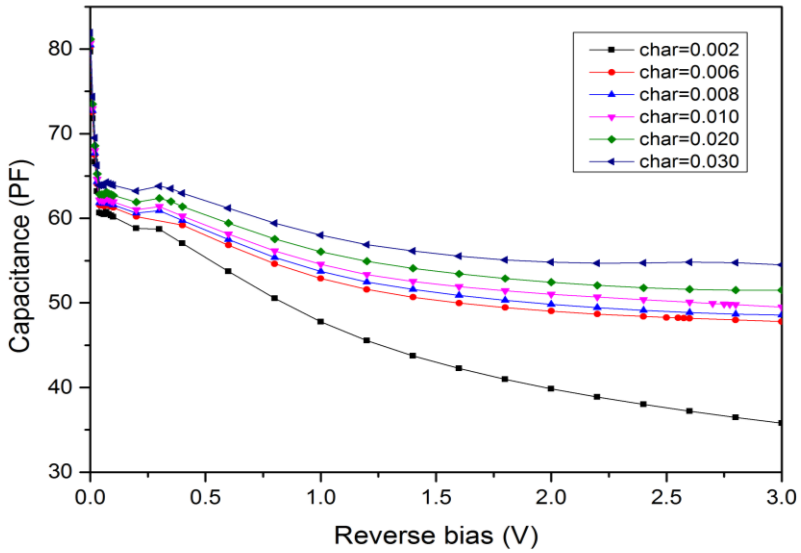


Figure 5.36: The simulated Capacitance voltage in present of traps peak density with different characteristic lengths.

In order to study the second parameter of the Gaussian distribution, which is the peak position; different structures were simulated by fixing the peak characteristic length at 0.006 and its density at $10^{18}\ cm^{-3}$, and varying the peak distance from 0.1 to 0.5 μm from the surface. This is shown in Figure 5.37.

The curves can be divided into 2 groups: the first group contains the distances (0.5, 0.45 and 0.4 μm). For this group the capacitance show a normal behaviour, where it increases with decreasing distance between the peak and the surface. The second group contains the distances (0.3, 0.2 and 0.1 μm). In these cases the capacitance shows different shapes. The closest one to the experimental results is the peak positioned at a distance of 0.3μm from the surface. This peak causes an NDC similar to the observed in measured C-V, but it is not in the same voltage interval. In addition this peak's depth is far from the position of the irregularity defined by the expansion of the depletion region. On the other hand, the peak positioned

around $0.418\ \mu m$) causes a variation of the capacitance shape at (2.5 to $3\ V$) where the capacitance increases again.

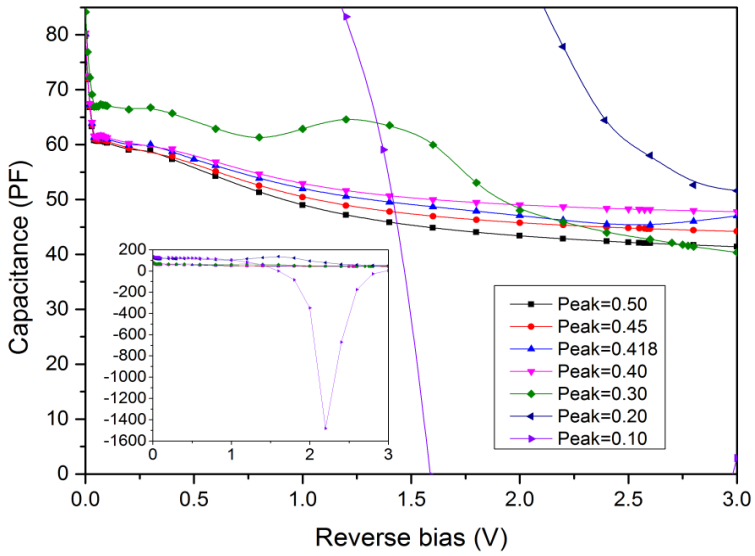


Figure 5.37: The simulated Capacitance voltage in present of traps peak at different distances from the surface.

In order to get a closer C-V to the measured characteristics, another simulation is suggested to study the effect of the peak concentration using the last distance ($0.418\ \mu m$) and the characteristic length (0.006) with different densities, the results are presented in Figure 5.38.

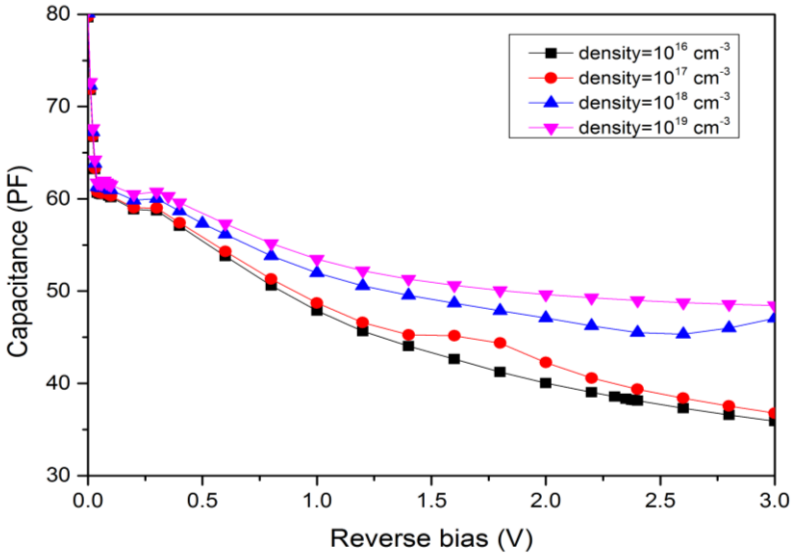


Figure 5.38: The simulated Capacitance voltage in present of traps peak with different concentrations.

It is clear that the capacitance increases with increasing traps peak concentration. But it also changes its shape. Comparing to experimental results, the closest results are obtained using a peak with concentration of ($10^{17} cm^{-3}$). In order to reduce the possibilities, a simulation was carried out using these peak parameters on each trap alone. So the new structures will contain a uniform distribution of dopants and traps in addition to a peak of high density of one trap each time. The results are then compared to the closest graph obtained from the precedent simulations (Figure 5.38).

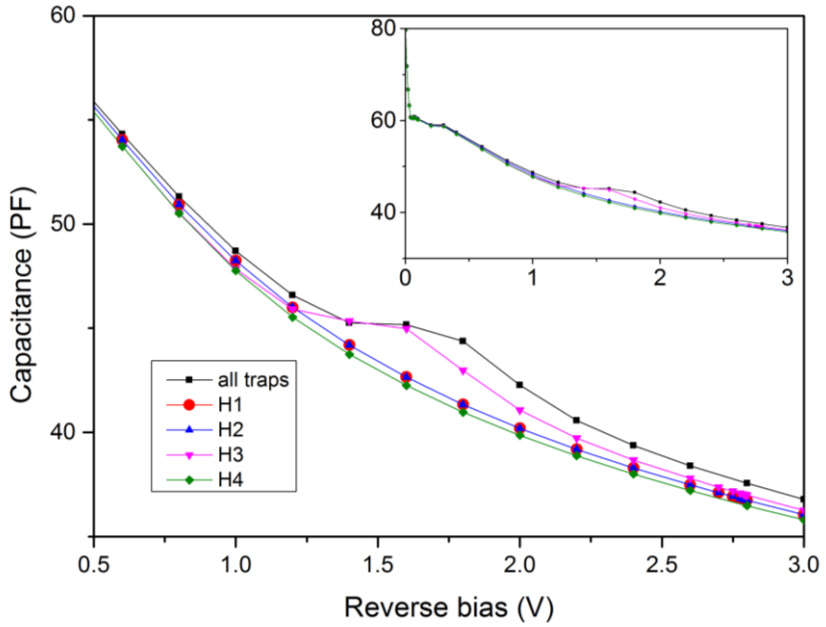


Figure 5.39: The simulated Capacitance voltage in presence of every trap peak alone.

It is apparent that the presence of a peak of the traps (H1, H2 and H4) has a small effect on the C-V characteristic compared to that of H3, which is the main reason of the irregularity observed in the presence of all traps peak. This result imposes the study of the presence of a peak of high concentration of the third trap (H3) alone.

5.5.1.6. Effect of H3 level on the capacitance

The obtained results from studying every trap's effect on the capacitance (whether the uniform distribution or the peak distribution) reveal the most important impact of the presence of the third level (H3) compared to others. This leads to a more detailed study of the effect of non-uniform distribution of H3.

a. GRADIENT DISTRIBUTION (FROM TOP TO BOTTOM)

First we will start by a simple distribution with decreasing concentration from top to bottom. For that purpose a Gaussian distribution has been used with a peak positioned at the surface ($peak = -0.6\ \mu m$) and concentration of $10^{18} cm^{-3}$ and characteristic length of 0.006.

As was expected the presence of gradient concentration of the third level (H3) has a huge effect on the capacitance values and shape (Figure 5.40). But this result is not even close to experiments, which exclude this distribution possibility.

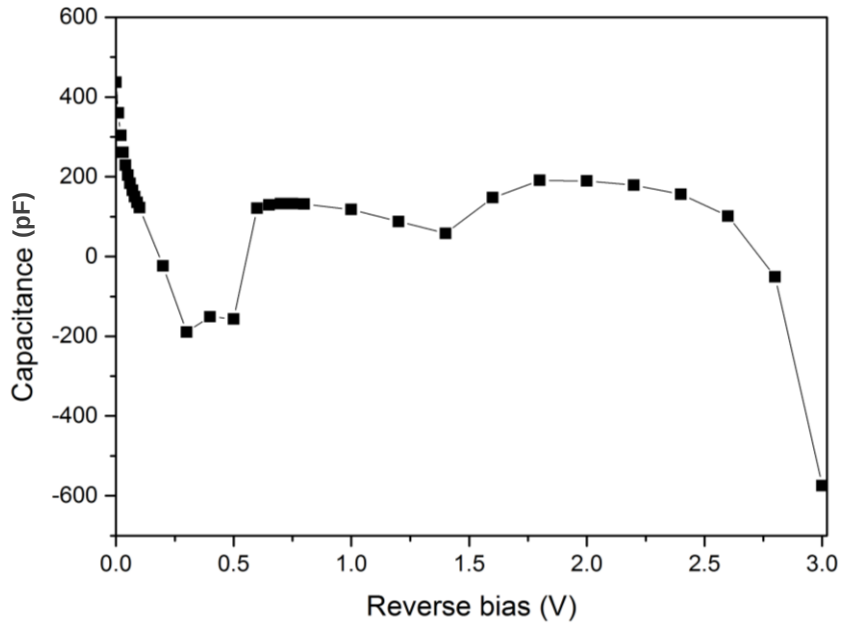


Figure 5.40: The simulated capacitance-voltage characteristics of the NU926 sample for gradient trap (H3) distribution from top to bottom.

b. PEAK DISTRIBUTION

In this section we will study the effect of presence of high peak density of the third level (H3). This will be done using the Gaussian distribution, and again we have three parameters to study: position, characteristic length and density.

We have simulated the effect of the H3 peak's density on the C-V characteristics, which is shown in Figure 5.41. Small values of H3 density (< 10^{17}cm^{-3}) do not show NDC. As this density increases a NDC is observed and increases with the concentration, the best concentration value that gives a clear NDC is $N.Peak = 10^{18} cm^{-3}$. As the density reaches

10^{19} cm^{-3}, NDC disappears. It's clear now that the third level is the main reason of the observed convexity in the measured C-V.

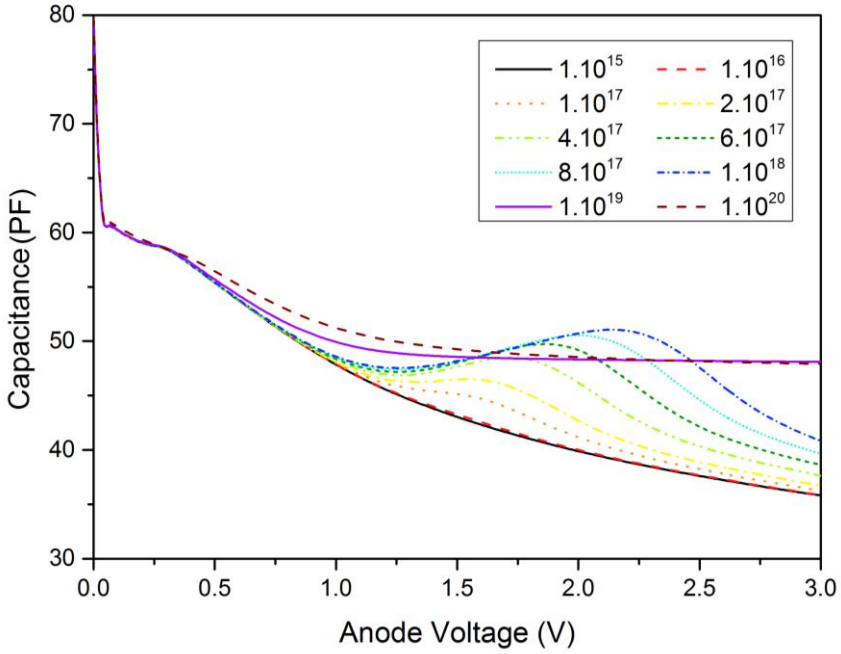


Figure 5.41: The simulated capacitance-voltage characteristics of the NU926 sample for different densities of the non-uniformly distributed H3. Other levels are kept uniform.

Further evidence of the responsibility of H3 for the NDC is provided by the simulation of the effect of the peak's position from the surface (Figure 5.42) on the C-V characteristics, as presented in Figure 5.43. For a distance of 0.3 μm from the surface, a large NDC can be seen but the peak is very narrow and does not resemble experimental observation. For 0.4 μm, although NDC is present but it persists over a wide range of voltage (from 1 to >3 V). For other positions, NDC is not observed at all except for 0.418 μm. In fact even a negative capacitance is observed as shown in the inset of Figure 5.43. This phenomenon was studied previously [96]. The position of 0.418 μm is very similar to that observed experimentally (Figure 5.43).

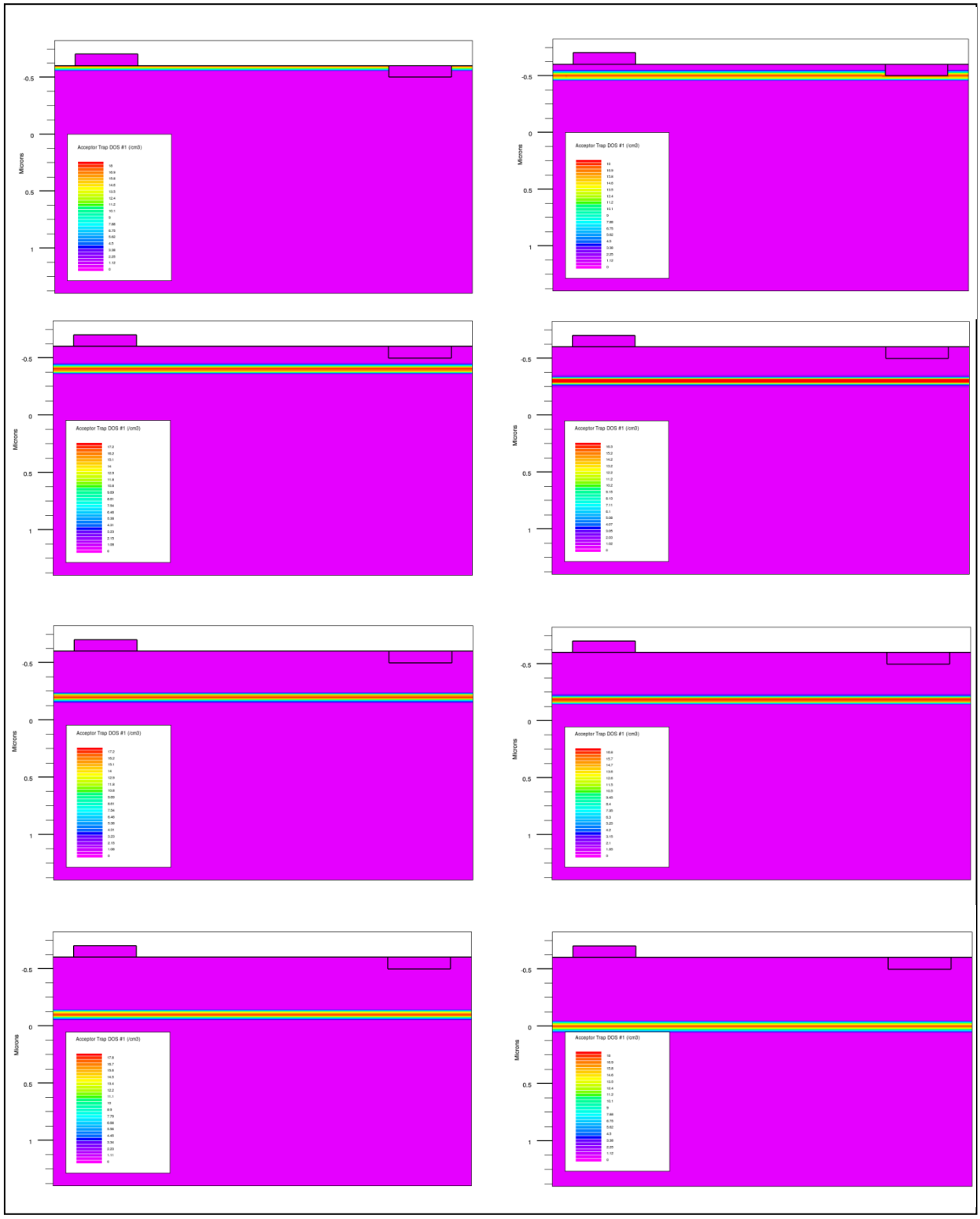


Figure 5.42: structures in presence of traps peak density with different distance from surface.

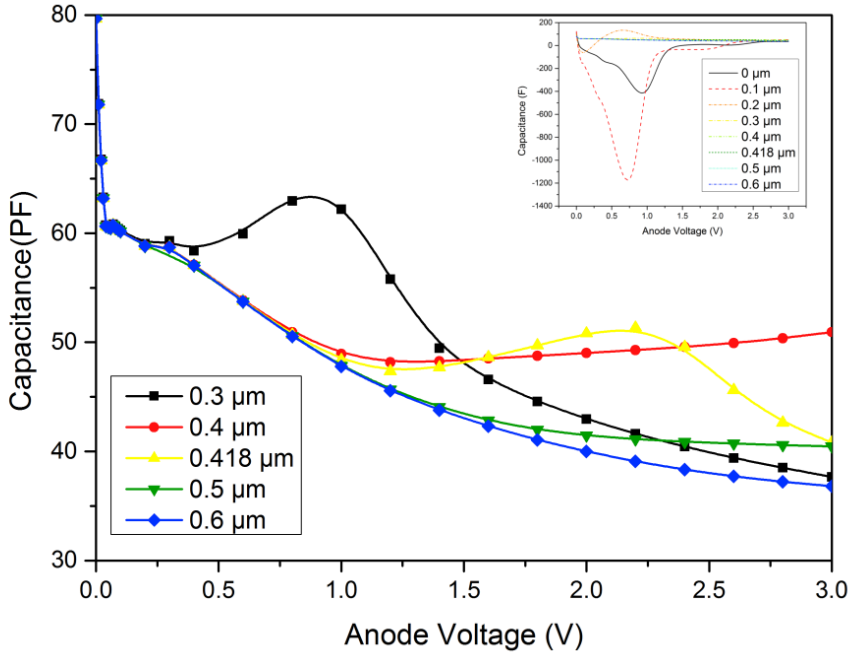


Figure 5.43: The simulated capacitance-voltage characteristics of the NU926 sample for different positions of the non-uniformly distributed H3 from the surface. The insert is for other positions for which a negative capacitance appears.

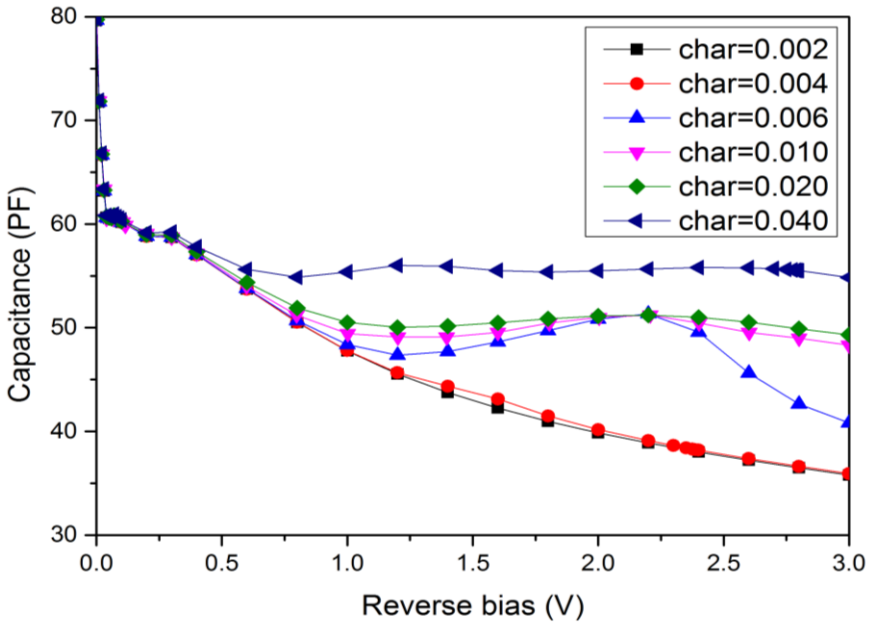


Figure 5.44: The simulated capacitance-voltage characteristics of the NU926 sample for different characteristic length of the non-uniformly distributed H3.

The last Gaussian distribution variable is the characteristic length. Its effect on capacitance is studied by simulating different structures with different characteristic length values using the best values for other variables (maximum concentration $10^{18} cm^{-3}$, distance $0.418\ \mu m$ from the surface), as presented in Figure 5.44. For a characteristic length of $0.3\ \mu m$, a small NDC can be seen but the peak is very wide. By decreasing the characteristic length, the NDC starts to increase and narrow at the same time till it reaches its biggest value at $char = 0.006$. After that it starts to fade at $char = 0.004$. However, its signs can still be seen around the voltage ($V = 1.5\ V$). Finally it disappears at $char = 0.002$ where the peak is very narrow to cause a remarkable effect.

5.5.2. Sample NU928

For this sample, DLTS reveals both majority and minority deep levels. The C-V characteristics show the usual shape but with a slow changing capacitance with reverse bias. In simulation of the C-V characteristics of this sample we will use uniform distribution of all levels (doping and deep) and use the values given in Table 5.2. The results are presented in Figure 5.45.

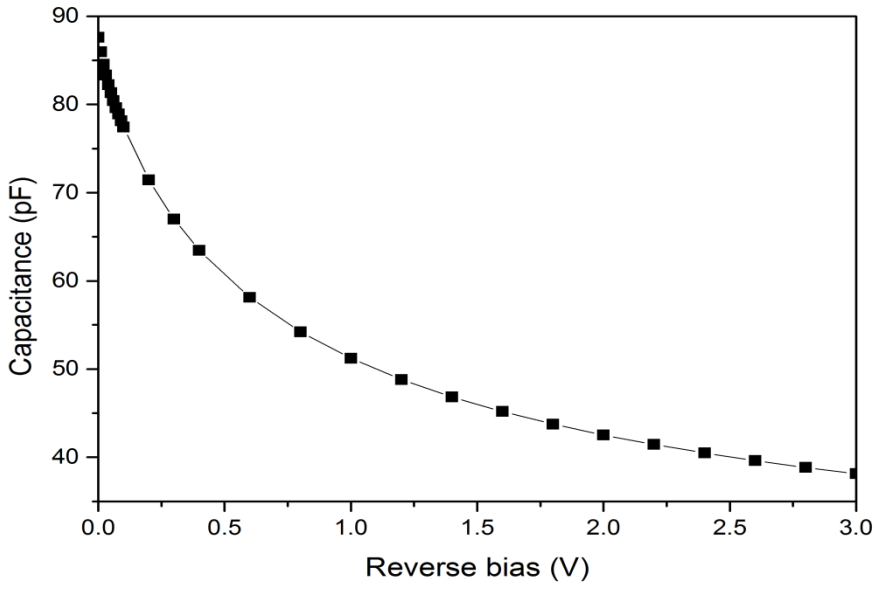


Figure 5.45: The simulated capacitance voltage of NU928 sample.

However, the C-V characteristics did not resemble the measured capacitance. Thus a study of the effect of dopants concentration was done by simulating the sample structure with different

dopants density (see Figure 5.46). The results show that the capacitance simply increases with increasing dopants density maintaining its ideal shape, which is not the case for experimental measurements.

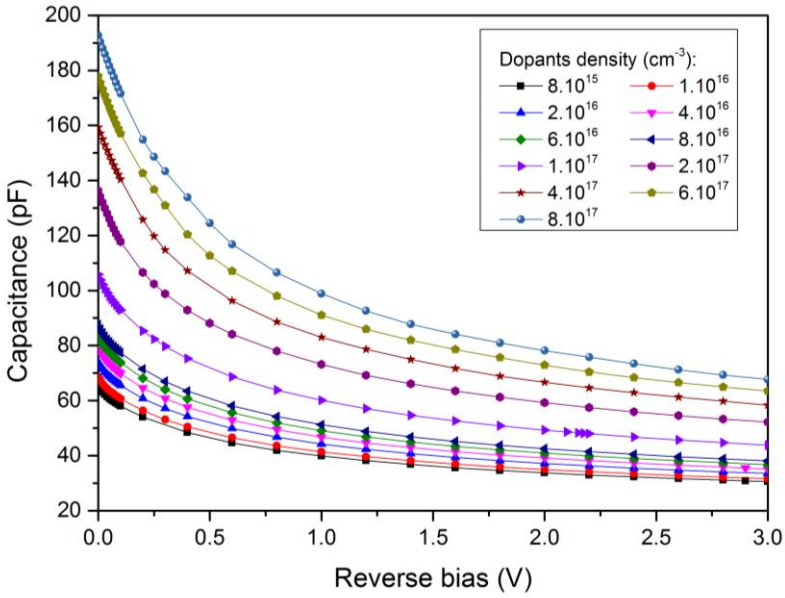


Figure 5.46: The simulated capacitance voltage of NU928 sample with different dopants densities.

Thus, in order to get comparable simulation and measurement results, the C-V characteristics were simulated again, but this time for different deep donor density. The simulation results are shown in Figure 5.47. An interesting phenomenon is observed in this simulation. The capacitance (at any bias) decreases with increasing density of the deep donor level then increases after the latter surpasses a value of ~4 × 10^{16}cm^{-3} as shown in the insert of Figure 5.50 for a bias of 0 V. This is the value of the deep donor density where simulation is comparable to measurement. The decrease and increase of the capacitance with increasing density of deep levels is a well-known phenomenon and is usually attributed to a type inversion of the semiconductor [100]. In the present case the p-type semiconductor has become n-type because of the high density of the deep donor. We can see also that the capacitance changes its ideal shape with donor traps densities equal or bigger than $2.10^{16} cm^{-3}$, where it has small changes with voltage. This is similar to the measured capacitance.

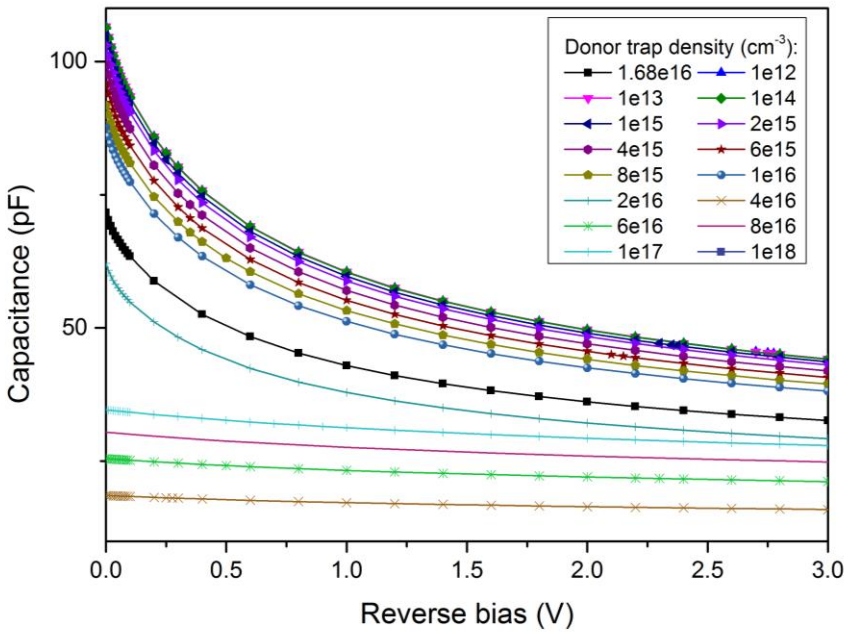


Figure 5.47: The simulated capacitance voltage of NU928 sample with different donor traps densities.

5.5.2.1. Final results

After scanning different parameters in different structures with different distributions, the simulation has successfully reproduced similar responses of the strange C-V characteristics of the samples NU926, and NU928. By comparing the simulated C-Vs to the measured ones, we can choose the best distributions values for both structures:

For the NU 926 sample the best C-V is obtained using a uniform distribution of dopants and traps mentioned in Table 5.1, in addition to a peak of the third level (H3) positioned at distance of $0.418\ \mu m$ from the surface and density of $10^{18} cm^{-3}$ and characteristic length of 0.006.

To confirm the responsibility of the third level (H3) of the NDC, we have simulated the presence of other levels each alone using the best parameters mentioned above that give a clear NDC. The distribution used in simulation is presented in fig, and the results are shown in fig. It is clear that only a non-uniform distribution of the deep level H3 which produces NDC.

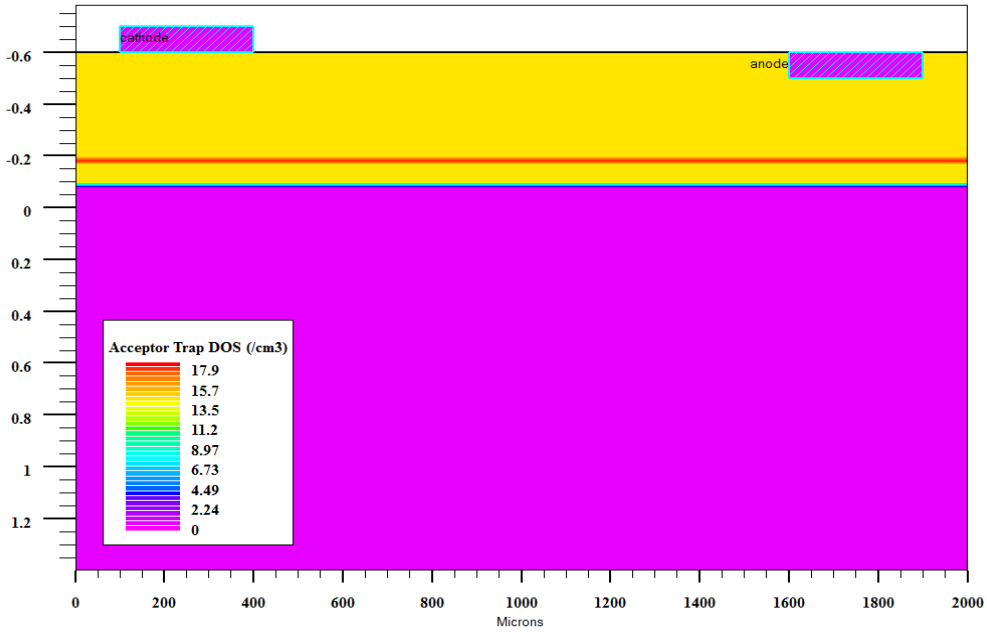


Figure 5.48: Best distribution density used in simulation.

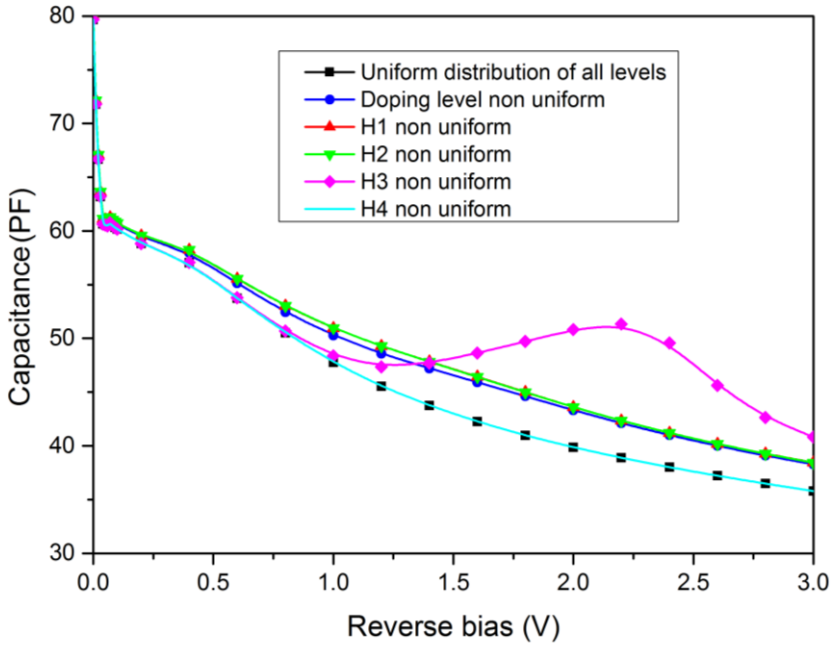


Figure 5.49: The simulated capacitance-voltage characteristics of NU926 sample: uniform distribution of all levels (squares), doping level non-uniform (circles), H1 non-uniform (up triangles), H2 non-uniform (down triangles), H3 non-uniform (diamonds) and H4 non-uniform (simple line).

For the sample NU928. the measured C-V characteristic is reproduced by simulation for a deep donor density of ~4 × 10^{16}cm^{-3} which is a bit higher than that given in Table 5.2. This may be due to the value of the acceptor doping density used in the simulation which may be not correct.

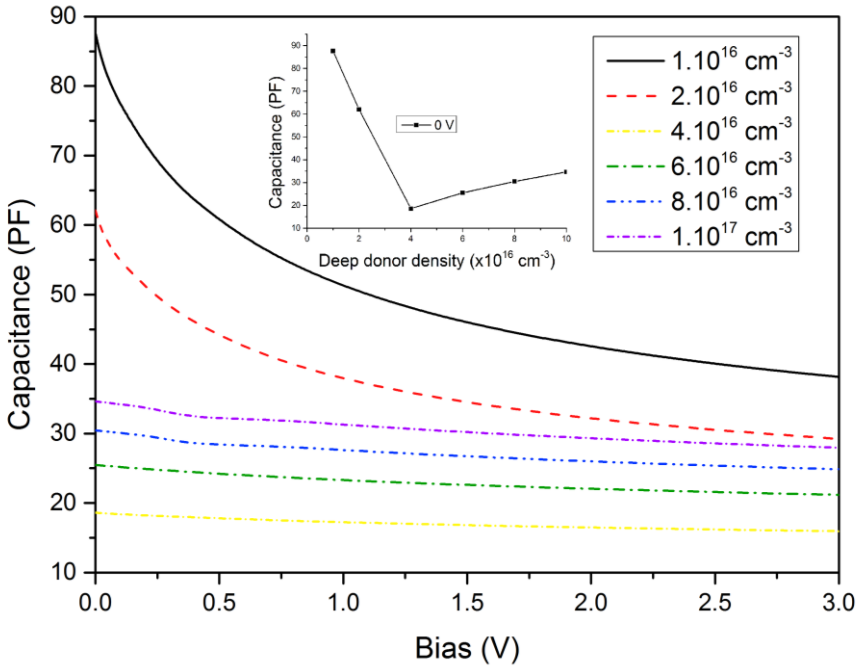


Figure 5.50: The simulated capacitance-voltage characteristics of the NU928 sample for different densities of the deep donor level "E" The insert is the capacitance for a bias of 0V versus the deep donor density showing the type inversion phenomenon.

Further evidence of the samples structure can be found using the effective doping density profile, which has been evaluated from the measured C-V characteristics (Figure 5.51). The doping density profile proves the presence of irregularity with a peak form in the sample NU926. This peak has a width of 0.035 µm, which is almost the same width measured at the same concentration in simulated structures. Also, both peaks (experimental and simulated) are at very close positions: 0.40 µm for real peak and 0.418 µm for simulated peak. Another time the simulation has proven their worth in predicting real phenomena.

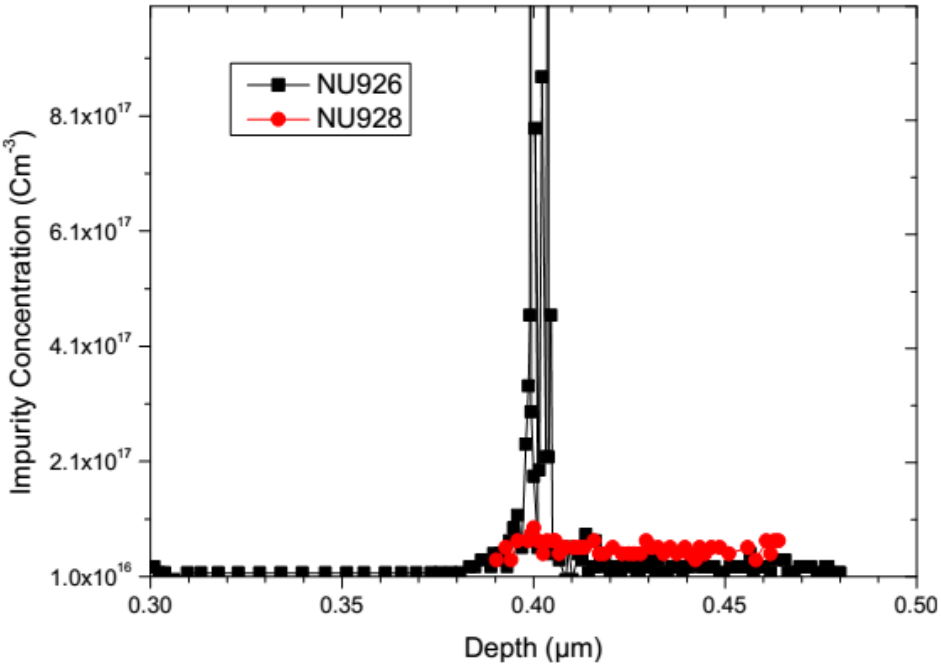


Figure 5.51: The effective doping density profile evaluated from the C-V characteristics.

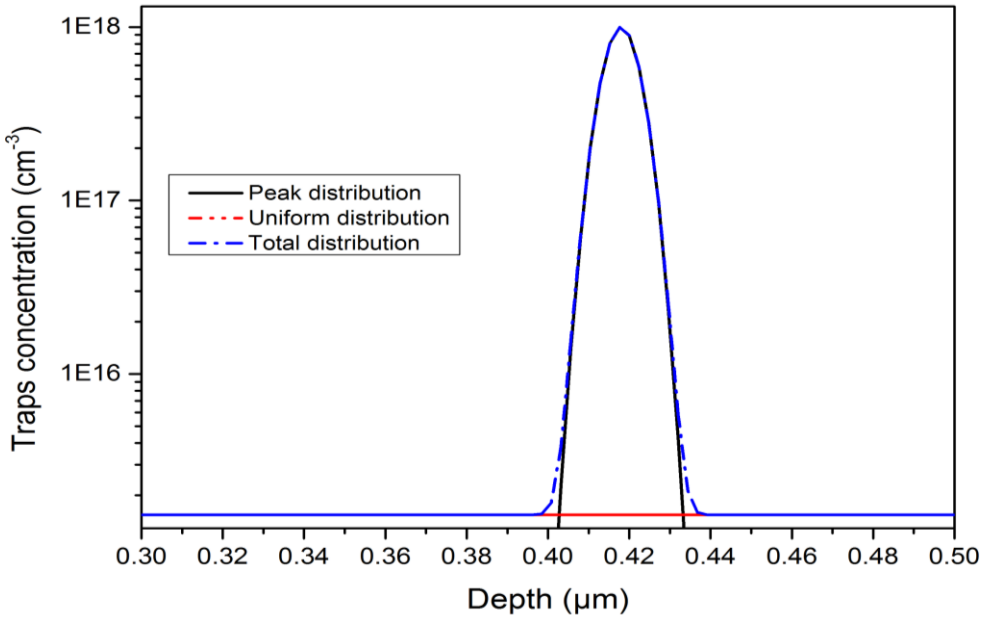


Figure 5.52: The peak's profile of traps high density used in simulation.

5.6. Conclusion

Two p-type GaAs Schottky diodes grown on (311)A and (211)A SI GaAs substrates were characterized by capacitance–voltage, capacitance–temperature and DLTS measurements. The capacitance–voltage characteristics of the (311)A sample were found to depart from the usual capacitance–temperature dependence. DLTS revealed that in the (311)A sample only majority type defects are present, while in the (211)A sample both majority and minority related defects were detected. The departure of the C–T characteristics was related to the presence of deep acceptor defects. A peak was found in these characteristics and this effect was more pronounced for the (311)A sample. The capacitance–voltage was also found to depart from the expected defect free samples. This was related to the presence of a deep acceptor defect which has a non-uniform density.

Numerical simulation by the SILVACO-TCAD software was successfully used to reproduce the experimentally observed effects. The obtained simulation results are in agreement with experimental measurements and confirm that the presence of deep levels is responsible for the strange behaviour observed in capacitance-temperature.

Simulation was also used to study the effect of presence of shallow and deep levels on capacitance voltage characteristics. Where it showed that the shallow levels can affect capacitance voltage values but not its shape. Unlike the shallow levels, simulation has shown that deep levels can affect either the values or the shape of capacitance voltage characteristics.

Capacitance-voltage characteristics were found to be sensitive to distribution profile especially for deep levels. Different capacitance responses were produced using different traps distribution profiles such as the use of different regions with different densities, or the use of gradually decreasing distributions. Finally the use of a peak of high density with the form of Gaussian distribution, showed very different capacitance responses. These results were successfully used to define the best distributions that reproduce the same strange behaviour observed in samples NU926 and NU928. Finally, a comparison showed an agreement between real samples using the effective doping density profile and the used profile in simulation.

Chapter 6

Conclusion

In this thesis, two p-type GaAs Silicon doped Schottky diodes grown on (311)A and (211)A GaAs substrates were characterized by capacitance–voltage, capacitance–temperature and DLTS measurements. DLTS revealed that in the (311)A sample only majority type defects are present, while in the (211)A sample both majority and minority related defects were detected.

The capacitance–temperature characteristics of the samples were found to depart from the usual C–T dependence. A peak was found in these characteristics for the (311)A sample, where the capacitance-temperature characteristics increases with temperature then decreases again, which gives a different shape compared to the ideal C-T characteristics. For the second sample (211)A the capacitance temperature has a closer C-T shape to the ideal C-T, where it only increases with temperature, except that it increases with small changes. Also, it shows a tiny peak compared to the (311)A sample. The strange effect of temperature on capacitance was related to the presence of different types of deep defects in the samples.

The capacitance–voltage characteristics of both samples were also found to depart from the expected defect free samples. The (311)A C-V shows a negative differential capacitance in form of a convexity after a few volts of reverse bias. However, the (211)A sample shows a C-V with small changes with reverse bias. The departure of the capacitance voltage was also related to the presence deep acceptors for (311)A and to both types of defects for (211)A.

In order to confirm these hypotheses a numerical simulation by the SILVACO-TCAD software was successfully used to reproduce the experimentally observed effects of temperature in presence of defects for both cases (samples (211)A and (311)A). Further evidence on the responsibility of the defects on these strange behaviours was revealed by

comparing the C-T of different structures with and without presence of defects. Also, a simulation of the capacitance-temperature was done in different frequencies shows clearly the annealing of the defects effect with increasing frequency.

The simulation proved that the presence of defects with different parameters does not reproduce the same observed behaviour of the capacitance-voltage characteristics. The observed convexity after few volts of reverse bias on the (311)A sample led to the hypothesis of non-uniform distribution of defects. The effect of non-uniformity was studied by simulating the effect of different distributions of deep and shallow defects on capacitance-voltage characteristics. These distributions were suggested basing on the expansion of the depletion region in the reverse bias. The simulation showed that the non-uniformity of shallow levels has different effects on the C-V characteristics, but this does not include the negative differential capacitance.

On the other hand the non-uniformity of deep levels affects the C-V in different manners reproduces NDC. But the most important distribution for this work is the presence of a peak of a high density at 0.4 µm from the surface. This distribution shows the closest behaviour to the real samples. Moreover, a comparison showed an agreement between the real and the simulated samples using the effective doping density profile, which showed a similar peak to the used in simulation. Finally, Simulation did not reveal only the best distribution of defects; it also revealed the main level responsible of this behaviour.

Perspectives

- This work revealed the responsibility of the presence of defects on the strange behaviour of C-T and C-V. In order to more understand this effect, another study is required to investigate the other possibilities of defects parameters that reproduce the same effect without being restricted to experimental results. Furthermore, a model that describes the variation of this behaviour depending on the defects parameters can be suggested.
- Different behaviours were found during the simulation of different distributions. These behaviours still need other precise explanations.
- The strange behaviour of these defects leads to the study of their effect on other characteristics such as the current-voltage characteristics.

Appendix:

Deep level transient spectroscopy

The differences between the theoretical and real semiconductor devices' properties are considerable, and the defects are one of the most important causes for these differences. That is why the identification of such defects gives us a closer look of reality. In that purpose a lot of serious attempts were held, one of them is Deep Level Transient Spectroscopy (DLTS) which is a very popular characterization technique that depends on the change of the junction capacitance of diodes such as pn or Schottky diodes. Since its invention by Lang in 1974 [4], DLTS is considered to be the most powerful technique for the assessment of electrically active defect states present in semiconductors. The technique is capable of displaying the spectrum of traps in a crystal as positive and negative peaks on a flat baseline as a function of temperature. It is sensitive, rapid, and easy to analyse. The sign of the peak indicates whether the trap is near the conduction or valence band, the height of the peak is proportional to the trap concentration, and the position, in temperature, of the peak is uniquely determined by the thermal emission properties of the trap. In addition, it can measures the activation energy, concentration profile, and electron and hole capture cross sections for each trap.

The DLTS signal is obtained from the capacitance transient which originates due to the filling and empting of the defect levels by applying electrical pulses to the sample under observation. it is based on the slow response of the deep levels and its effect on the capacitance. Let suppose that a Schottky diode is reverse biased for a long time, and therefore all the traps are emptying (Fig A.1.a). Then a filling pulse is applied for sufficient time so the traps can capture carriers (Fig A.1.b). After the filling pulse is applied the state of the traps goes again from a filling to an emptying as shown in Figure A.1.c. This is the most important step in DLTS.

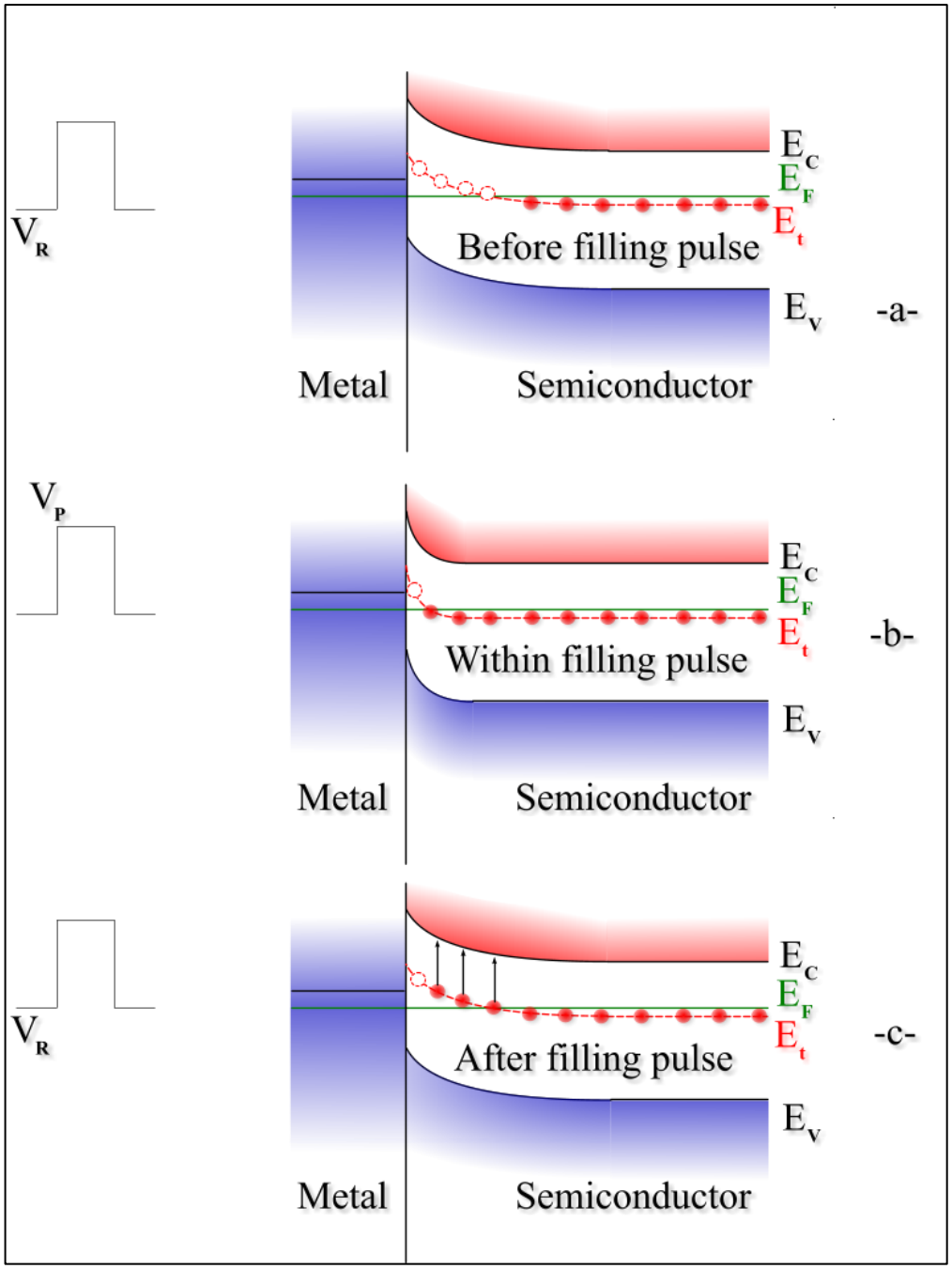


Figure A.1: Illustration of the band diagram of an n-type Schottky diode under different bias conditions: (a) under reverse bias (V = V_R), (b) under filling pulse condition (V =V_P) and (c) under reverse bias (V = V_R).

In this step the bias changes instantly while the measured capacitance take time to return to its initial value due to the slow response of the traps (Fig A.2.a). This delay can be described using the equation (3.45), which can be simplified using a first-order expansion, so:

$$C = C_0\left(1 + \frac{N_t}{2N_D}\left[1 - \exp\left(-\frac{t}{\tau}\right)\right]\right) \qquad \text{(A.1)}$$

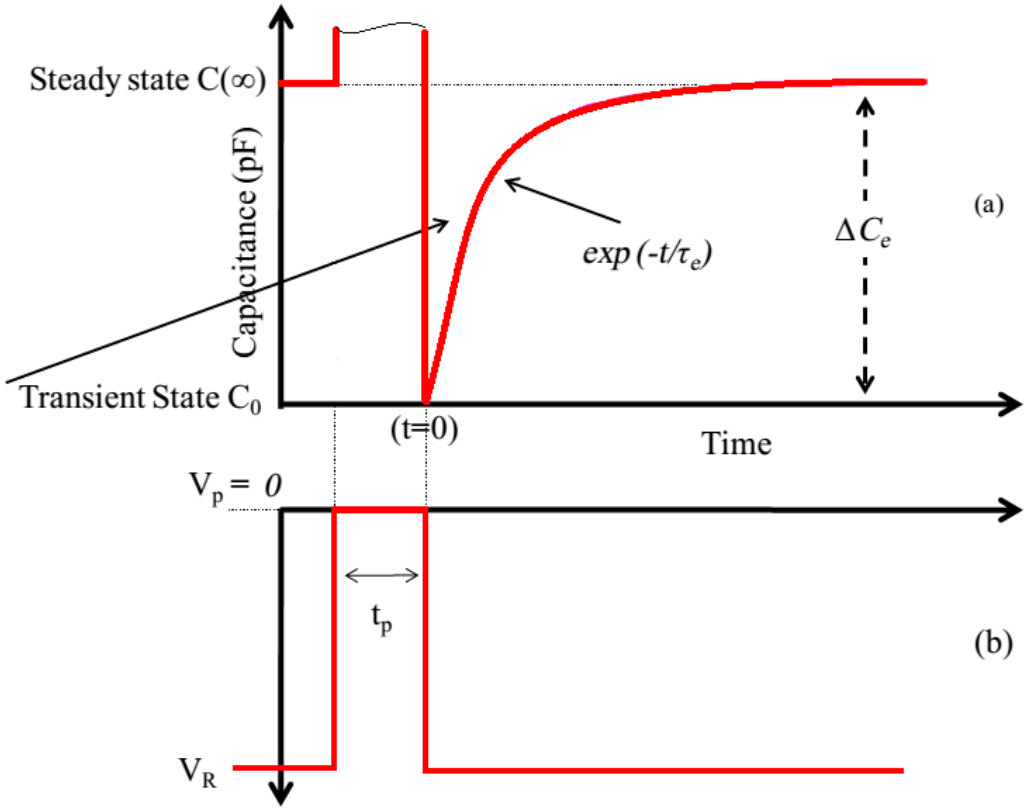


Figure A.2: (a) Capacitance transient response of the Schottky diode for different bias conditions shown in (b).

D.V Lang [28] introduced the conventional DLTS technique in 1974, this technique is based on the rate window concept where the capacitance is measured at two different times t1 and t2 (t2 > t1). The DLTS signal (S) is basically the change in capacitance between t1 and t2 [$S = \Delta C = \big(C(t1) - C(t2)\big)$]. Therefore, the DLTS signal (S) is mathematically written as

$$S(T) = \frac{C_0 N_t}{2N_D}\left[\exp\left(-\frac{t_2}{\tau_e}\right) - \exp\left(-\frac{t_1}{\tau_e}\right)\right] \qquad (A.2)$$

The maximum amplitude of the DLTS signal is obtained when the inverse emission rates (τ_{max}) is equal to the DLTS rate window as described below. The value of $\tau_{e,max}$ can be deduced by taking the first derivative of equation (A.2) and equating it to zero i.e.($\frac{dS(T)}{dt}$). Then:

$$\tau_{e,max} = \frac{t_2 - t_1}{\ln(t_2/t_1)} \text{ for } \tau = \tau_{e,max} \qquad (A.3)$$

Equation (A.3) is known as the rate window. By changing the values of two measurement times one can change the value of the rate window and thus the peak maximum can be obtained at different temperatures.

By changing the temperature the capacitance recovery will be faster, therefor we obtain different DLTS signal values as a function of temperature (The DLTS signal generation process is schematically represented in Figure A.3. It can be seen that the emission rates become faster and faster with increasing the temperature of the sample. The DLTS signal peaks when the inverse of emission rate ($\tau = \tau e,max = 1/en$) matches ($\Delta t = t2-t1$).

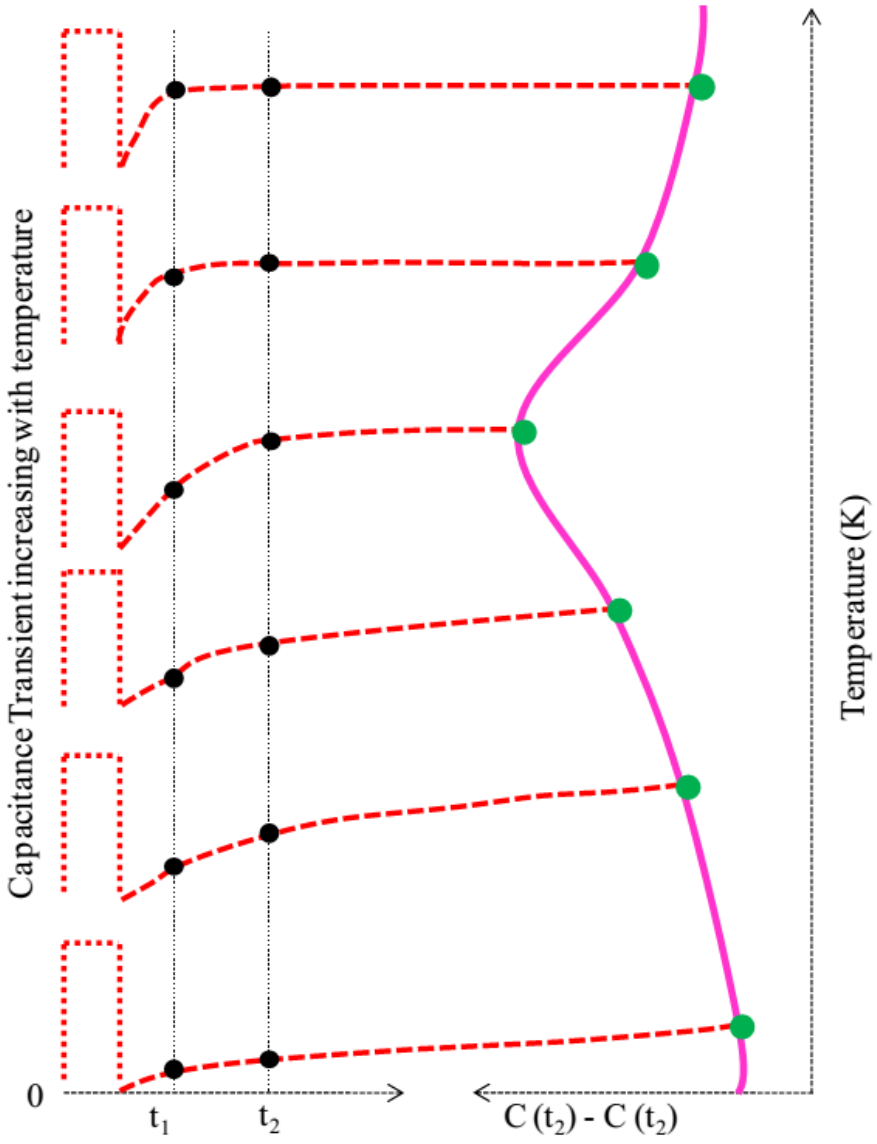


Figure A.3: The generation of DLTS signal from capacitance transient [7].

The DLTS relies on the use of different rate windows to determine the emission rates at different temperatures. For example, by using equation (3.11) the electrons emission rates can be written as:

$$e_n = \gamma_n . \sigma_n . T^2 . \exp\left(-\frac{\Delta E}{KT}\right) \tag{A.4}$$

where $\Delta E = E_C - E_t$ is the trap activation energy with respect to conduction band energy.

$$\ln\left({}^{e_n}/_{T^2}\right) = -\frac{\Delta E}{KT} + \ln(\gamma_n . \sigma_n) \tag{A.5}$$

The plot of $\ln({}^{e_n}/_{T^2})$ versus (1000/T) should be a straight line. The slope of the plot is used to calculate the trap activation energy (eV), whereas the intercept at (1000/T) = 0 is used to deduce the value of the capture cross-section of the trap (Fig A.4).

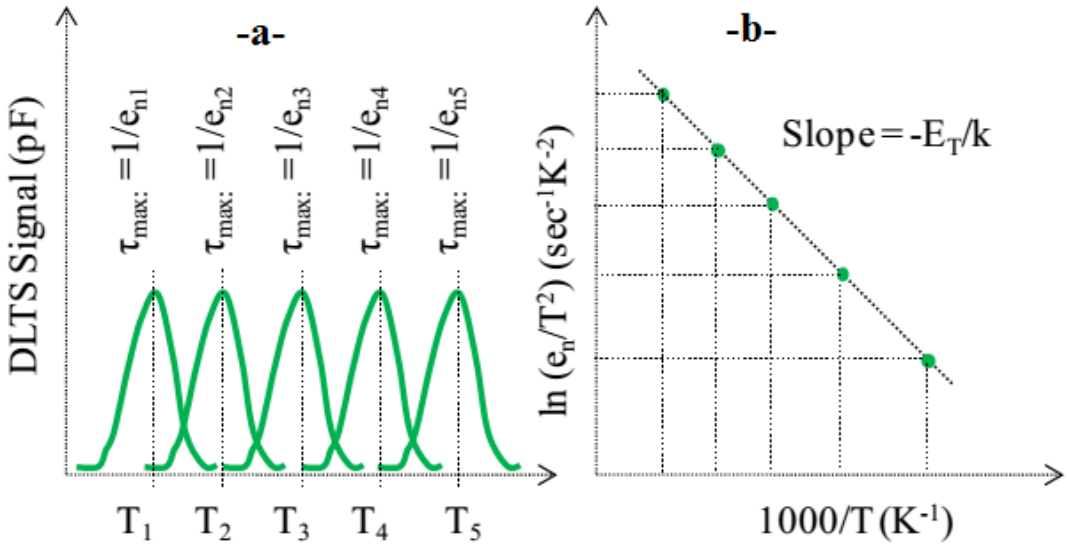


Figure A.4: a. the change in peak position for different rate windows, b. the Arrhenius plot for the calculation of trap activation energy (E_t) [7].

The trap concentration (cm-3) is directly related to the amplitude of the DLTS peak. The mathematical relation to calculate the trap concentration can be derived from equation (A.1). Considering that the filling pulse is applied for sufficient time so that the trap is completely filled (nT(t) = NT), the difference between the initial value ($C(0)$) and the steady state ($C(\infty)$) is written as:

$$\Delta C = C(0) - C(\infty) = C_0\left(\frac{N_t}{2N_D}\right) \tag{A.6}$$

$$\Rightarrow N_t = 2N_D \frac{\Delta C}{C_0} \quad \text{(A.7)}$$

where N_t is the trap concentration,ΔC is the conventional DLTS peak amplitude and C_0 is the capacitance at maximum reverse bias.

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Deep traps and temperature effects on the capacitance of p-type Si-doped GaAs Schottky diodes on (2 1 1) and (3 1 1) oriented GaAs substrates

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ABSTRACT

The SILVACO-TCAD numerical simulator is used to explain the effect of different types of deep levels on the temperature dependence of the capacitance of p-type Si-doped GaAs Schottky diodes grown on high index GaAs substrates, namely (3 1 1)A and (2 1 1)A oriented GaAs substrates. For the (3 1 1)A diodes, the measured capacitance–temperature characteristics at different reverse biases show a large peak while the (2 1 1)A devices display a much smaller one. This peak is related to the presence of different types of deep levels in the two structures. These deep levels are characterized by the Deep Level Transient Spectroscopy (DLTS) technique. In the (3 1 1)A structure only majority deep levels (hole deep levels) were observed while both majority and minority deep levels were present in the (2 1 1)A diodes. The simulation software, which calculates the capacitance–voltage and the capacitance–temperature characteristics in the absence and presence of different types of deep levels, agrees well with the experimentally observed behavior of the capacitance–temperature properties. A further evidence to confirm that deep levels are responsible for the observed phenomenon is provided by a simulation of the capacitance–temperature characteristics as a function of the ac-signal frequency.

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Modeling the effect of deep traps on the capacitance–voltage characteristics of p-type Si-doped GaAs Schottky diodes grown on high index GaAs substrates

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ABSTRACT

Numerical simulation, using SILVACO-TCAD, is carried out to explain experimentally observed effects of different types of deep levels on the capacitance–voltage characteristics of p-type Si-doped GaAs Schottky diodes grown on high index GaAs substrates. Two diodes were grown on (311)A and (211)A oriented GaAs substrates using Molecular Beam Epitaxy (MBE). Although, deep levels were observed in both structures, the measured capacitance–voltage characteristics show a negative differential capacitance (NDC) for the (311)A diodes, while the (211)A devices display a usual behaviour. The NDC is related to the nature and spatial distribution of the deep levels, which are characterized by the Deep Level Transient Spectroscopy (DLTS) technique. In the (311)A structure only majority deep levels (hole traps) were observed while both majority and minority deep levels were present in the (211)A diodes. The simulation, which calculates the capacitance–voltage characteristics in the absence and presence of different types of deep levels, agrees well with the experimentally observed behaviour.

1. Introduction

Silicon (Si) doping of Gallium Arsenide (GaAs) and other III–V semiconductors offers an advantage over Beryllium (Be) because of its amphoteric nature. It can be either a donor (occupies a group V site) or acceptor (occupies a group III site) depending on the substrate orientation [1–5]. Si is mainly a donor when the growth is on the (100) surface. However, silicon incorporates preferentially as a donor in (*N*11)B, and as an acceptor or a donor on (*N*11)A surfaces (*N*=1,2,3) depending on the substrate temperature and the arsenic overpressure used during the MBE growth. A and B denote a Ga- and As-terminated plane, respectively. Thus, the interest in the growth of III–V compound semiconductors on high index planes, other than the conventional (100) orientation, has increased tremendously over the last several years. In fact the MBE growth of p-type GaAs/AlGaAs heterostructures on (311)A results in higher hole mobilities than those based on the conventional Be-doped p-type on (100) GaAs plane [6–11].A wide variety of structures can be grown on high index planes such as quantum wire structures [12], quantum dots [13,14], zero-dimensional quantum dots and one-dimensional quantum wires [15–17].

The growth of semiconductor layers and structures strongly depends on the substrate orientation and hence to surface atomic arrangement [18,19]. This may lead to some defects which could have deleterious effects on the electrical and optical properties of III–V based devices [20].

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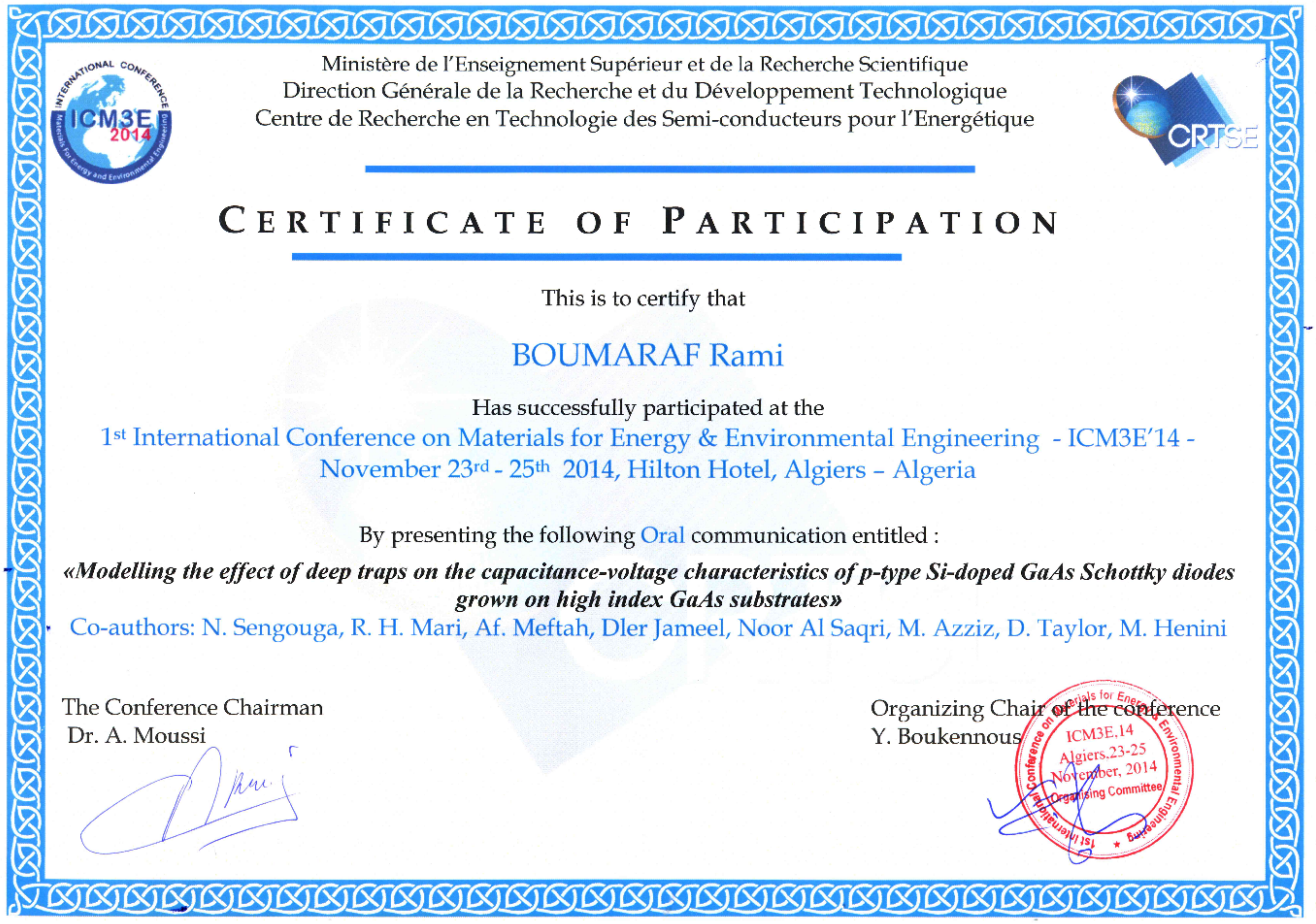

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CERTIFICATE OF PARTICIPATION

This is to certify that

BOUMARAF Rami

Has successfully participated at the
1st International Conference on Materials for Energy & Environmental Engineering - ICM3E'14 -
November 23rd - 25th 2014, Hilton Hotel, Algiers – Algeria

By presenting the following Oral communication entitled :

«Modelling the effect of deep traps on the capacitance-voltage characteristics of p-type Si-doped GaAs Schottky diodes grown on high index GaAs substrates»

Co-authors: N. Sengouga, R. H. Mari, Af. Meftah, Dler Jameel, Noor Al Saqri, M. Azziz, D. Taylor, M. Henini

The Conference Chairman
Dr. A. Moussi

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CONGRATULATION

BOUMARAF Rami

As a result of your participation at the
1st International Conference on Materials for Energy & Environmental Engineering - ICM3E'14 -
November 23rd - 25th 2014, Hilton Hotel, Algiers – Algeria

With **Oral** communication entitled :

Modelling the effect of deep traps on the capacitance-voltage characteristics of p-type Si-doped GaAs Schottky diodes grown on high index GaAs substrates

The organizing committee is pleased to award you first prize

Dr. N. Gabouze, Director CRTSE

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