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Etude des Transistors couches minces (TFTs) à base d'alliages des oxydes amorphes d'In, Sn et Zn.

Study of thin film transistors (TFTs) based on In, Sn and Zn amorphous oxides alloys

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Dedication

To my dear parents

To my brothers and sisters

To all my teachers and
administrative staff

To all those who are dear to me

Acknowledgements

In the Name of Allah, the Beneficent, the Merciful

ملخص

في هذا العمل, تم اقتراح تأثير أنواع مختلفة من عوازل البوابة ذات k- العالي, كما تم أيضا اقتراح تأثير سمك العوازل مزدوجة الطبقات مع تأثير سمك الأكسيد المكافئ لعازل البوابة وكذلك سمك العوازل أحادية الطبقة, بالإضافة إلى ذلك, تم اقتراح تأثير العوازل البينية ذات k- منخفض مثل SiO$_2$ جنبا إلى جنب مع تأثير العوازل البينية ذات k- عالي مثل Al$_2$O$_3$ على أداء وموثوقية a-ITZO TFT. لذلك تم تنفيذ العديد من التحليلات من خلال المحاكاة العددية للجهاز بواسطة برنامج Silvaco Atlas الذي تم استخدامه لإجراء تحليل رقمي مفصل للتحقيق في العلاقة بين هذه التأثيرات المختلفة وأداء وموثوقية الجهاز.

النتائج أظهرت أن استبدال طبقة SiO$_2$ ذات k-المنخفض بطبقة عازلة ذات k-عالي في a-ITZO TFT المرتكز على عازل أحادي الطبقة يؤدي إلى تحسينات مغرية في أداء a-ITZO TFT مماثلة للتحسينات الناجمة عن تناقص السمك المادي لعازل البوابة دون تأثيرات التسرب المرتبطة بها.

أيضا, جهاز a-ITZO TFT المرتكز على عازل مزدوج الطبقة (SiO$_2$/HfO$_2$) مع سماكة مادية أعلى (DDT = 70 nm) يمكنه أن يقدم نفس الخصائص الكهربائية التي يقدمها جهاز a-ITZO TFT المرتكز على الأكسيد المكافئ مع سماكة أقل, سبع مرات تقريبا (EOT = 10 nm) دون تأثيرات التسرب المرتبطة بها, في حين يقدم خصائص كهربائية أحسن بكثير من الخصائص التي يقدمها a-ITZO TFT المرتكز على عازل أحادي الطبقة (SiO$_2$) من أجل نفس السماكة المادية (DDT = 70 nm).

بالإضافة إلى ذلك, جهاز a-ITZO TFT المرتكز على عازل مزدوج الطبقة (Al$_2$O$_3$/HfO$_2$) مع سماكة مادية (PT = 30 nm) يمكنه أن يقدم خصائص كهربائية جيدة أحسن من الخصائص التي يقدمها جهاز a-ITZO TFT المرتكز على عازل مزدوج الطبقة (SiO$_2$/HfO$_2$) من أجل نفس السماكة المادية. مع ذلك, فإنه لا يمكننا إهمال الدور الأساسي لطبقة SiO$_2$ البينية ذات k- المنخفض بين القناة والعازل ذو k-العالي, التي تملك بعض الصفات الجيدة فيما يتعلق بحركية الحاملات في قناة الترانزستور. أيضا, على الرغم من وجود تفاوت في قيمة التسرب بين الجهازين, إلا أن تأثيره ضعيف للغاية على أداء الجهاز وموثوقيته, خاصة من أجل توترات البوابة المنخفضة.

الكلمات المفتاحية: TFT؛ A-ITZO؛ SiO$_2$؛ Al$_2$O$_3$؛ k-منخفض؛ k-عالي؛ EOT؛ Silvaco Atlas.

Abstract

This work is mainly focused on a numerical optimization of a-ITZO TFT based on the gate dielectric materials. Different types of high-k gate dielectrics are proposed. The effect of the thickness of : the double-layered dielectric, the equivalent oxide and the mono-layered dielectric of the gate is also presented. In addition, the effect of the interfacial states that can subsist between the TFT channel and the gate dielectric is also studied, for first low-k dielectrics such as SiO_2 and second for high-k dielectrics such as Al_2O_3. Accurate analyses were implemented through numerical simulation of the device by Silvaco Atlas software that was used to carry out a detailed numerical analysis for investigating the relationship between these different effects and the performance and reliability of the device.

The results showed that replacing the low-k SiO_2 layer by a high-k dielectric layer in TFT based on the mono-layered dielectric leads to attractive improvements in the performance of a-ITZO TFT similar to the improvements resulting from the decrease in the physical thickness of the gate dielectric without the associated leakage effects.

Also, the TFT device based on the double-layered dielectric (SiO_2/HfO_2) with a higher thickness (DDT = 70 nm) it can provide the same electrical properties that are offered by TFT device based on the equivalent oxide with a less thickness, almost seven times (EOT = 10 nm), without the associated leakage effects, while provides electrical properties better than properties that are offered by TFT based on the mono-layered dielectric (SiO_2), for the same thickness (MDT = 70 nm).

In addition, the TFT device based on the double-layered dielectric (Al_2O_3/HfO_2) with a physical thickness (PT = 30 nm) it can provide good electrical properties better than the properties provided by TFT based on the double-layered dielectric (SiO_2/HfO_2) for the same physical thickness. However, it we cannot neglect the fundamental role of the interfacial low-k SiO_2 layer between the channel and the high-k dielectric, which has some beneficial qualities with regard to the carrier mobility in the transistor channel. Also, although there is a difference in the value of leakage between the two devices, its effect is very poor on the performance of the device and its reliability, especially for low gate tensions.

Keywords: TFT; A-ITZO; SiO_2; Al_2O_3; Low-k; High-k; EOT; Silvaco Atlas.

Résumé

Dans ce travail, l'effets des différents types de diélectriques de la grille haute k, l'épaisseur diélectriques à double couche, et l'épaisseur d'oxyde équivalente du diélectrique de grille ainsi que de l'épaisseur diélectrique monocouche de la grille ont été suggérés. En plus, l'effet des diélectriques interfaciaux à faible k tels que SiO_2 a été suggéré, ainsi que l'effet des diélectriques interfaciaux à haute k tels que l'Al_2O_3 sur les performances et la fiabilité de a-ITZO TCM. Par conséquent, plusieurs analyses ont été réalisées grâce à la simulation numérique du dispositif par le logiciel Silvaco Atlas, qui a été utilisé pour effectuer une analyse numérique détaillée afin d'étudier la relation entre ces différents effets et les performances et la fiabilité du dispositif.

Les résultats ont montré que le remplacement de la couche de SiO_2 à faible k par une couche diélectrique à haute k dans l'a-ITZO TCM basé sur la diélectrique monocouche conduit à des améliorations intéressantes dans les performances de l'a-ITZO TCM qui sont similaires aux améliorations résultant de la diminution de l'épaisseur du diélectrique de grille sans les effets de fuite associés.

De même, le dispositif l'a-ITZO TCM basé sur le diélectrique à double couche (SiO_2 / HfO_2) avec une épaisseur plus élevée (DDT = 70 nm) peut fournir les mêmes propriétés électriques offertes par le dispositif a-ITZO TCM basé sur l'oxyde équivalent avec un épaisseur inférieure, presque sept fois (EOE = 10 nm), sans les effets de fuite associés, tout en offrant des propriétés électriques de bien meilleures que celles offertes par un a-ITZO TCM basé sur le diélectrique monocouche (SiO_2), pour la même épaisseur (MDT = 70 nm).

En outre, le dispositif a-ITZO TCM basé sur le diélectrique à double couche (Al_2O_3 / HfO_2) avec une épaisseur physique (PT = 30 nm) peut offrir de meilleures propriétés électriques que les propriétés fournies par a-ITZO TCM basé sur diélectrique à double couche (SiO_2 / HfO_2) pour la même épaisseur physique. Cependant, nous ne pouvons pas ignorer le rôle fondamental de la couche interfaciaux à faible k SiO_2 entre le canal et le diélectrique à haute k, qui présente des avantages en ce qui concerne la mobilité de la porteuse dans le canal du transistor. En outre bien qu'il y ait une différence de valeur de fuite entre les deux appareils, sauf que son effet est très faible sur les performances de l'appareil et sa fiabilité, en particulier pour les faibles tensions de la grille.

Mots clés: TCM; A-ITZO; SiO_2; Al_2O_3; faible k; haute k; EOE; Silvaco Atlas.

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LIST OF ABBREVIATIONS

AOS: Amorphous Oxide Semiconductors

TFT: Thin-Film Transistor

a-Si: amorphous Silicon

pc-Si: polycrystalline Silicon

OS: Organic Semiconductors

a-ITZO: amorphous Indium-Tin-Zinc-Oxide

EOT: Equivalent Oxide Thickness

SS: Subthreshold Swing

DDT: Double-layered Dielectric Thickness

MDT: Mono-layered Dielectric Thickness

T: Tail

G: Gaussian

A: Acceptor

D: Donor

DOS: Density Of States

2D: two-Dimensional

3D: three-Dimensional

TCO: Transparent Conducting Oxide

a-IGZO: amorphous Indium-Gallium-Zinc-Oxide

In_2O_3: Indium Oxide

SnO_2: Tin Oxide

ZnO: Zinc Oxide

CC: Constant-Current

MP: Match-Point

SD: Second-Derivative

TD: Third-Derivative

CTSRTR: Current-To-Square-Root-Transconductance Ratio

LE: Linear Extrapolation

CBT: Conduction Band Tail

VBT: Valence Band Tail

CMOS: Complementary Metal Oxide Semiconductor

nm: nanometer

a-IGZO: amorphous Indium-Gallium-Zinc-Oxide

GDT: Gate Dielectric Thickness

F: Fluorine

C: Carbon

DLC : Diamond Like Carbon

PT: Physical Thickness

ALE: Associated Leakage Effects

FETs: Field Effect Transistors

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

ICs : Integrated Circuits

TAOS: Transparent Amorphous Oxide Semiconductor

GENERAL INTRODUCTION

Amorphous oxide semiconductors (AOS) have attracted considerable attention for various electronic device applications [1] such as solar cells, transparent electrodes, touch screen panels, optoelectronic devices, in flat panel displays, and often used as a channel in the thin-film transistors (TFTs) [2]. Although several materials such as amorphous silicon (a-Si), polycrystalline silicon (pc-Si), organic semiconductors (OS), and ZnO which is formed as a polycrystalline structure can be used as active layers for thin film transistor (TFT), there is growing interest in AOS based on zinc oxide because considered as promising materials for the channel of thin film transistor (TFT) in the next generation display backplanes because they can accomplish high mobility and large-area uniformity at low-temperature process as well as the use of plastic substrate [3]. Most prominent of these materials is amorphous indium-gallium-zinc-oxide (a-IGZO) [4] who has several attractive advantages which include high transparency to visible light [5], uniform deposition at low temperature [6], good controllability of carrier concentration [7]. Recently, amorphous indium-tin-zinc-oxide (a-ITZO) has attracted considerable attention as a new AOS material because it also requires low process temperature [8], it has a wide band gap (>3.02 eV) [9], shows good performance with high mobility (μ_{FE} ~30 $cm^2V^{-1}s^{-1}$) [10], high work function (4.9-6.1 eV) [11], and a high transparency (>85 $\%$) in the visible range [12]. Amorphous-ITZO with a mobility higher than a-IGZO and lower cost has become one of the most promising materials which have been developed for future advanced to the backplanes in ultra-high-definition and high-frame-rate displays for replacing the a-IGZO [13].

Historically, the dielectric most often used in TFT technology was SiO_2, has been used as a gate oxide material for decades [14, 15]. In order raise the performance of TFT devices, researchers sought to reduce the thickness of the SiO_2 gate dielectric for increase the gate capacitance per unit area, which will lead to lifting current and then raising transistor performance [15].

But the problem is that the SiO_2 gate dielectric thickness has steadily decreased until it arrived a level where the SiO_2 will not be able to provide adequate reliability due to the increased of the direct tunneling gate leakage current, leading to higher power consumption and then to lower transistor reliability [16].

Therefore, there has been a continuous search for dielectric materials that will offer a high capacitance per unit area and at the same time with a relatively large thickness, which can prevent or reduces the current leakage through the gate dielectric.

It appears that, after investigating a multitude of materials, found that this is possible by increasing the k of the material and that by replacing a high-k dielectric in place a low-k dielectric such as SiO_2 ($k = 3.9$). Because higher-k material by the relative approximation of old/new k can be physically thicker without being electrically thicker. This leading to increased or maintain the gate capacitance per unit area without the associated leakage effects.

For example, a high-k dielectric material with dielectric constant ($k=39$) compared to 3.9 for SiO_2 can be made ten times thicker than SiO_2 which helps to reduce the leakage of electrons across the dielectric pad of gate with achieving the same capacitance per unit area, and at the same time retaining the fast response of the transistor (retaining the switching speed of the device).

The other problem here is that most of the high-k dielectric materials have much poorer properties than the conventional SiO_2 [17], such as low interface quality, a poor morphological properties, and low thermal stability, in addition, the interface and oxide trap densities larger than those in SiO_2 as well as the energy band gap is less than SiO_2. It is known that the energy band gap can control the leakage of the gate current by a mechanism different from the thickness mechanism. Because the dielectric materials that have a higher band gap energy can prevent or reduce the current leakage through the gate dielectric with less thickness than the dielectrics that have a lower band gap energy [18].

The ideal solution would be to using a double-layered dielectric consisting of a very thin dielectric layer possesses good morphological properties such as SiO₂ ($k = 3.9$) in order to raise the quality of the interface and then obtaining a low interface traps density. Also, another dielectric layer is more thickness (compared to very thin SiO₂ layer) with a high-k such as HfO₂ ($k = 35$) in order obtaining a lower electrical dielectric thickness (a lower effective gate dielectric thickness) that is referred to as the equivalent oxide thickness (*EOT*). Thus obtaining a higher capacitance per unit area and at the same time with a great physical thickness, which can prevent or reduces the direct tunneling current leakage through gate dielectric.

This work consists of three main chapters; the content of each part is briefly described below:

Chapter I: *a-ITZO TFT overview*

The main purpose of this chapter is to conduct a comprehensive theoretical study. For this purpose we have carried out a bibliographic study provides general information about the a-ITZO, low-k dielectrics, high-k dielectrics, double-layered dielectrics, TFT and the method of extracting some output parameters of TFT such as the gate capacitance per unit area (C_i), threshold voltage (V_T), subthreshold swing (*SS*), field-effect mobility (μ_{FE}), on-current (I_{on}), on-off current ratio (I_{on}/I_{off}) and turn-on voltage (V_{on}) of a-ITZO TFT as well as the resistivity (ρ) of the a-ITZO active channel layer. As this part also contains the definitions and equations as well as materials that will be used in our researches.

Chapter II: *Silvaco Atlas for TFT simulation*

The main purpose of this chapter is focused on Silvaco Atlas software and its uses in the numerical simulations of TFT. For this purpose we have carried out a bibliographic study provides general information about the TFT simulators by Silvaco TCAD Atlas software [19].

Chapter 3: *Results and discussions*

The main purpose of this chapter is to:

- Elucidate the relation between the dielectric constant (k) effect of a range of the dielectric materials such as SiO_2, Si_3N_4, Al_2O_3, Y_2O_3, Gd_2O_5, $Zr_xSi_{1-x}O_y$, ZrO_2,CeO_2 La_2O_3, Ta_2O_5, HfO_2, TiO_2, Nb_2O_5, $SrZrO_3$, $BaSrTiO_3$ and $SrTiO_3$, and the change in the electrical characteristics and then the electrical properties of a-ITZO TFT.

- Elucidate the relation between the effect of the different types of the gate dielectric thicknesses and the change in the electrical properties of a-ITZO TFT.

- Conduct a comparative study in order to highlight the impact of the interfacial high-k dielectrics such as Al_2O_3 compared to the interfacial low-k dielectrics such as SiO_2, the existing between the a-ITZO active layer and high-k HfO_2 layer in a-ITZO TFT based on the double-layered dielectric.

For this purpose, several different effects on the electrical properties of the a-ITZO TFT were suggested.

In this part, depending on these different effects, we will study and discuss the electrical characteristics as the transfer ($I_{DS} - V_{GS}$) and output ($I_{DS} - V_{DS}$) characteristics, in addition to the electrical properties such as parameters : the C_i, V_T, SS, μ_{FE}, I_{on}, I_{on}/I_{off} and V_{on} of a-ITZO TFT as well as the ρ of the a-ITZO active channel layer.

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Chapter

1

a-ITZO TFT overview

I.1 Introduction

Although several materials can be used as active layers for thin film transistors (TFTs), there is growing interest in amorphous indium-tin-zinc-oxide (a-ITZO) because it has many good properties [1-3] such as a low process temperature [4], it has a wide band gap ($\geq 3.02\ eV$) [5], shows a good performance with a high mobility ($\mu_{FE} \sim 30\ cm^2V^{-1}s^{-1}$) [6], a high work function (4.9-6.1 eV) [7] and a high transparency (> 85 %) in the visible range [7].

Researchers sought to reduce the thickness of the SiO$_2$ gate dielectric for raising TFT performance. But the SiO$_2$ thickness has decreased until it arrived to a level where the SiO$_2$ will not be able to provide adequate reliability.

The solution to this problem will be by replacing SiO$_2$ with one of the high-k dielectrics. These materials can be physically thicker without being electrically thicker, leading to increased or maintain the good performance of the device, with improving its reliability.

The main purpose of this chapter is to conduct a comprehensive theoretical study. For this purpose we have carried out a bibliographic study on TFT, a-ITZO, and dielectrics, in addition to the method of extraction of some parameters such as threshold voltage (V_T), subthreshold swing (SS), field-effect mobility (μ_{FE}), on-current (I_{on}), on-off current ratio (I_{on}/I_{off}), turn-on voltage (V_{on}) of a-ITZO TFT and the resistivity (ρ) of the a-ITZO active channel layer.

I.2 The density of states (DOSs) for amorphous semiconductors

The total density of states (DOS) for as-deposited amorphous semiconductor materials (before annealing) is presented in Figure I.1.a. DOS is composed of :

- states of two tail bands (a donor-like valence band and an acceptor-like conduction band).

- States of two deep level bands (one acceptor-like and the other donor-like), localized trap states, trap states in H-poor disordered materials (passivated by H), which are modeled using a Gaussian distribution.

- Other dee levels which may be either uniform or modeled using Gaussian distribution in addition to doping levels and isolated states.

Figure I.1.b shows that the subgap density of states (DOS) after annealing ($g(E)$) is composed of four bands : acceptor-like exponentially conduction band tail states ($g_{TA}(E)$), donor-like exponentially valence band tail states ($g_{TD}(E)$), acceptor-like Gaussian deep levels band states ($g_{GA}(E)$) and donor-like Gaussian deep levels band states ($g_{GD}(E)$) [8]. These DOS can be modeled as [9]:

$$g(E) = g_{TA}(E) + g_{TD}(E) + g_{GA}(E) + g_{GD}(E) \tag{I.1}$$

Here:

$$g_{TA}(E) = N_{TA} exp\left[\frac{E-E_c}{W_{TA}}\right] \tag{I.2}$$

$$g_{TD}(E) = N_{TD} exp\left[\frac{E_v-E}{W_{TD}}\right] \tag{I.3}$$

$$g_{GA}(E) = N_{GA} exp\left[-\left[\frac{E_{GA}-E}{W_{GA}}\right]^2\right] \tag{I.4}$$

$$g_{GD}(E) = N_{GD} exp\left[-\left[\frac{E-E_{GD}}{W_{GD}}\right]^2\right] \tag{I.5}$$

where E is the trap energy, E_c is the conduction band energy, E_v is the valence band energy and the subscripts (T, G, A, D) stand for tail, Gaussian (deep level), acceptor and donor states, respectively, while as shown in Figures I.1.a and I.1.b that N_{TA} and N_{TD} are the densities of acceptor and donor-like states in the tail distribution, respectively at the conduction and valence band edges, respectively. N_{GA} and N_{GD} are the maximum densities of acceptor and donor-like states in Gaussian distribution, respectively. W_{TA} and W_{TD} are the characteristic decay energies for the tail distribution of acceptor and donor like states, respectively. W_{GA} and

W_{GD} are the characteristic decay energies for Gaussian distribution of acceptor and donor like states, respectively. E_{GA} and E_{GD} are the energies that correspond to the Gaussian distribution peak for acceptor and donor like states, respectively, these energies are measured from the conduction and valence band edges, respectively.

(a)

(b)
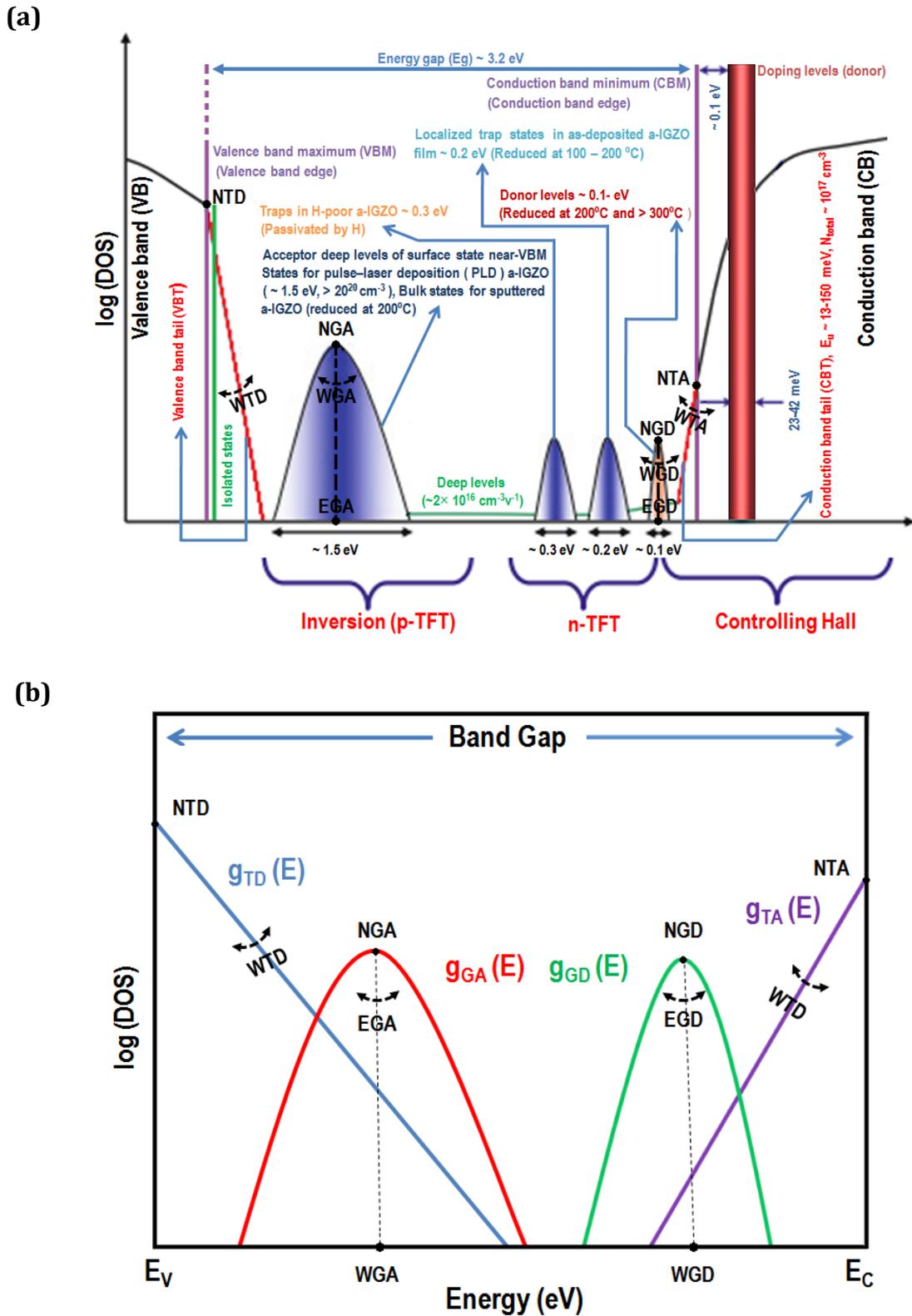
Figure I.1 Schematic electronic structure of a-IGZO where (a) shows the total density of states (DOS) within the band gap of as-deposited a-IGZO [10-13], while (b) shows the density of states (DOS) within the subgap of disordered materials after annealing ($g(E)$)[14].

I.3 The a-ITZO in the In_2O_3-SnO_2-ZnO System

The a-ITZO is a potential replacement for the currently used a-IGZO as a transparent conducting oxide (TCO) for the channel of thin film transistor (TFT). At the present time, a-IGZO is the material of choice for the channel layer, but the increasing cost of gallium metal and the advent of new technologies will require alternative TCOs.

Although several materials can be used as active layers for thin film transistors (TFTs), there is growing interest in amorphous indium-tin-zinc-oxide (a-ITZO) (Figure I.2.a) because considered as promising new AOS materials for the channel of TFT in the next generation display backplanes because it has high properties [1-3]: it requires a low process temperature, it has a wide band gap, shows a good performance with a high mobility, a high work function and a high transparency in the visible range [4-7].

Over the past years, thin film studies have been amassed that report the electrical and optical properties of various ITZO compositions [15]. To better understand the equilibrium phases that form in the ITZO multi-component system, we first briefly review the following end-points:

Amorphous indium-tin-zinc-oxide (a-ITZO), a compound of indium oxide (In_2O_3), tin oxide (SnO_2) and zinc oxide (ZnO) [16]. They are all n-type semiconductors. In_2O_3 has a bixbyite-type cubic crystal structure, which is also known as the C-type modification of the rare-earth sesquioxides [17]. Bixbyite is described as a fluorite-type structure with one-quarter of the anions "missing" in an ordered fashion. The cations reside at the body-center of a cube with anions occupying the corners. The two "missing" anions are located either across the body-diagonal of the cube (b site) or the face-center of the cube (d site) as shown in (Figure I.2.b) [15], and SnO_2 has a rutile crystal structure, where tin is coordinated by six oxygen atoms and oxygen is coordinated by three tin atoms [18]. Rutile is described by a hexagonal close packing of the anions with half of the octahedral holes filled by the cations (Figure I.2.c) [15],

while ZnO has a wurtzite crystal structure, which is a tetrahedral structure where zinc is coordinated by four oxygen atoms and oxygen is coordinated by four zinc atoms [19]. The structure consists of a hexagonal close packing of oxygen anions with zinc cations filling half of the tetrahedral holes, all of which exhibit the same orientation (Figure I.2.d) [15].
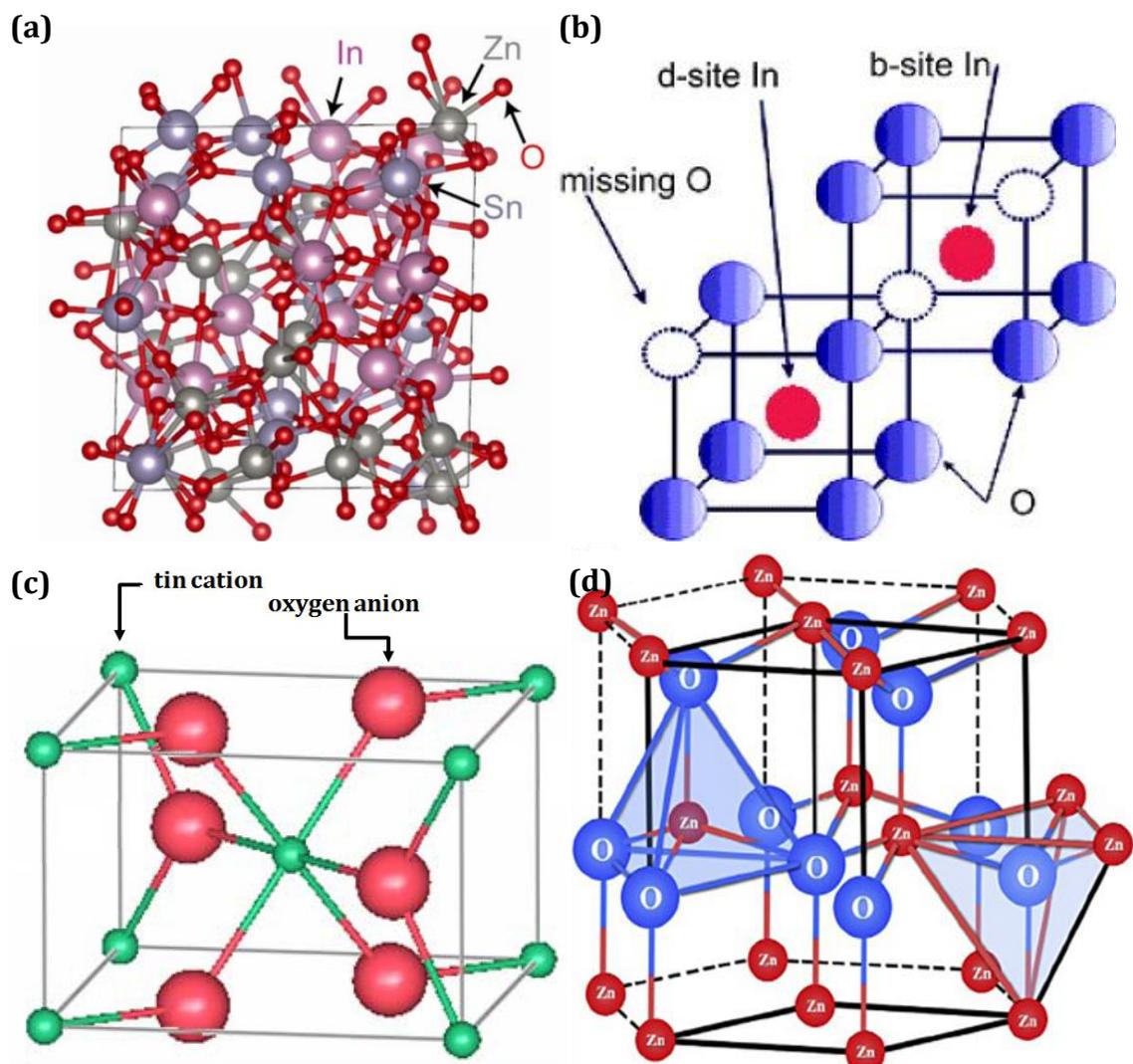
Figure I.2 Structures for each of a-ITZO, In_2O_3, SnO_2, and ZnO, respectively, where (a) shows the amorphous structure of ITZO [20], (b) shows bixbyite-type cubic crystal structure of In_2O_3[21], (c) shows a rutile crystal structure of SnO_2[22], and (d) shows a wurtzite crystal structure of ZnO [23].

Figure I.3 summarizes the widely recognized n-type TCOs encompassing the In_2O_3–SnO_2–ZnO system for practical applications [24]. Binary compounds such as In_2O_3, SnO_2 and

ZnO, ternary compounds such as ITO, and IZO, quaternary compounds such as ITZO and multi-component oxides including $(ZnO)_{1-x}(In_2O_3)_x$, $(In_2O_3)_x(SnO_2)_{1-x}$ and $(ZnO)_{1-x}(SnO_2)_x$ are also the subject of investigation [15, 25]. Among all the compounds for ZnO-based TCOs, a-ITZO is thought to be the best candidates so far.

(a)
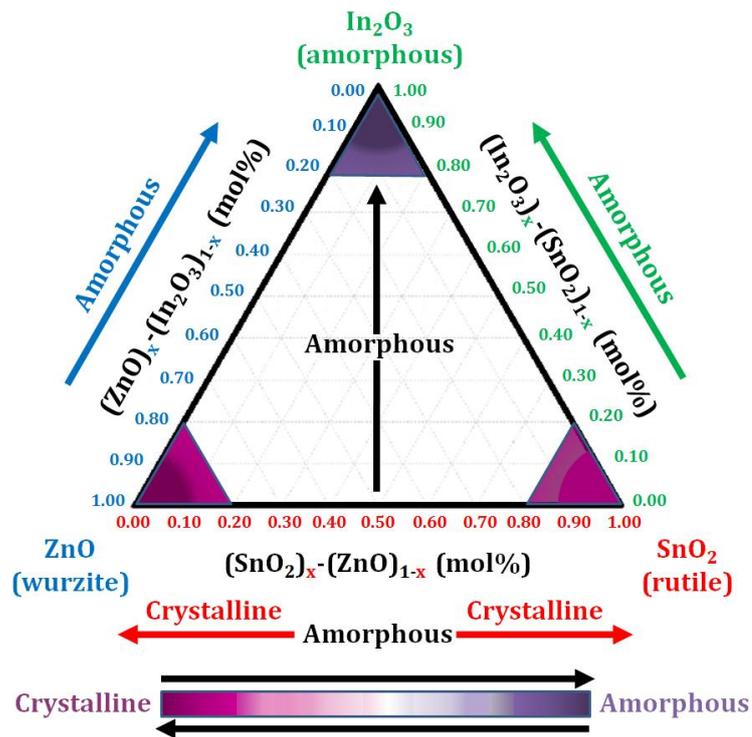
(b)
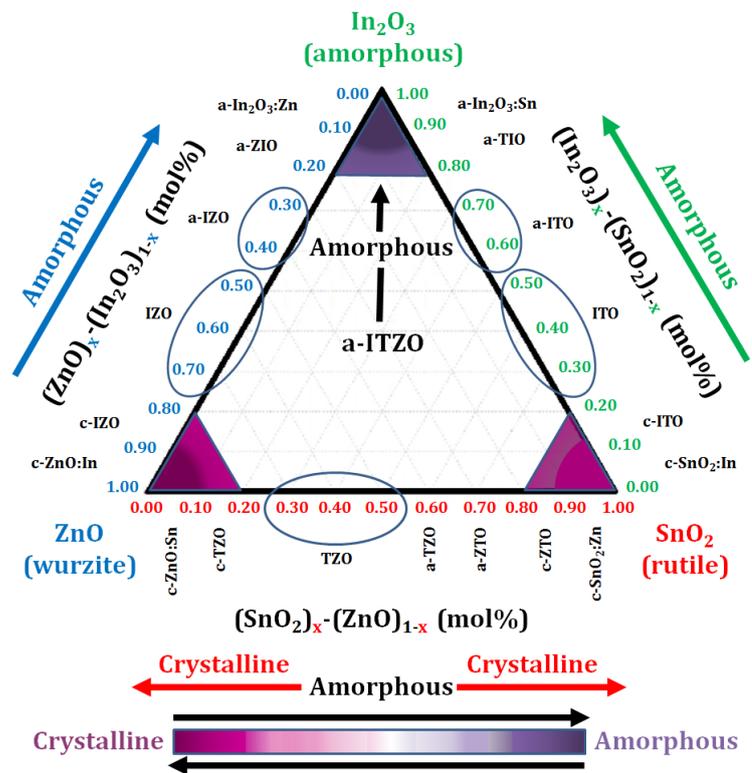
Figure I.3 The ternary diagram of TCOs in In$_2$O$_3$-SnO$_2$-ZnO system where (a) shows crystalline phase diagram of TCOs in In$_2$O$_3$-SnO$_2$-ZnO system and (b) shows some TCO semiconductors of this material family [15, 25].

I.4 Thin film transistors (TFTs)

TFTs are a class of field effect transistors (FETs), which the current through the device is modulated on the same basic principle as the metal oxide semiconductor field effect transistor (MOSFET) [26]. Because its structure and operation principles are similar to those of MOSFETs, which is the most critical device component in modern integrated circuits (ICs) [27].

TFTs are three terminal devices based on field effect with insulated gate built on an insulating substrate or surface. The current flowing between drain and source electrodes of a TFT is modulated by the capacitive injection of carriers close to the dielectric/semiconductor interface, known as field effect [26, 28]. The operation principle of TFTs is the same as that for MOSFETs. MOSFETs are normally fabricated on a mono-crystalline Si substrate, while TFTs are often fabricated on insulating glass substrates with a thin polycrystalline or amorphous film as the active layer. The fabrication of TFTs is more flexible than MOSFETs because of the additional freedom in the choice of a semiconductor other than Si. For example, large band gap semiconductors such as CdSe and CdS may be used. With the large band gap semiconductors as the active layer, the density of thermally generated carriers can be very small compared to the density of majority carriers [26, 29].

I.4.1 History of TFTs

Just years ago, it would have been hard to predict that TFTs would become so widespread in society and necessary in our daily life [30]. The time taken from the start of the research and development of TFTs to their expansion has been unexpectedly short [30].

Therefore, we cannot easily predict the future prospects of the development of TFT technologies; however, it will be beneficial for constructing future strategies to review the

history of the development of TFT technologies and study how they have developed [30]. The

development histories of TFTs and MOSFETs are similar, as shown in Figure I.4 [26, 27].

1925 MISFET concept
1935 MISFET patent

Ge Bipolar 1947
W. Shockley 1948

Si Bipolar 1950
pn JFET 1951
Si Bipolar production 1952

IC, planar FETs 1958

MOSFET 1960
MOSFET 1961
Commercial digital IC 1961

1962 CdS TFT

CMOS IC 1963

1964 Poly-SnO$_2$ TFT

RAM, ZnO FET 1968

Microprocessor 1971

1973 CdSe TFT LCD

1975 a-Si:H TFT

1979 a-Si:H TFT commercialization

1989 10.4 commercial TFT LCD

2003 Poly-ZnO TFT
2004 a-IGZO TFT

LCD panel (Casio) 2005
AMOLED panel (ETRI) 2006
AMOLED panel (LG)
Color E-paper
AMOLED panel (Samsung) 2007
Flexible OLED (LG)
AMLCD panel (Samsung) 2008

Figure I.4 History of oxide thin - film transistors (TFTs), IC development and flat panel displays

using a transparent amorphous oxide semiconductor (TAOS) TFT backplane [26, 27].

The metal insulator semiconductor field effect transistor (MISFET) conceptually was born in 1925 [27, 31]. The early popular TFT versions were made of compound semiconductors, such as CdS or CdSe [32, 33]. This kind of TFT has a high field effect mobility, μ_{eff}, e.g., > 40 cm^2/Vs [27].

The first attempt for implementing a TFT device is traced back to the 40's and it was a thin film field effect device used a germanium film (Bardeen and Brattain, 1948) [26].

The history and the structure of the TFTs, as it is known today, began with the work of Weimer (P. K. Weimer, 1962). Polycrystalline cadmium sulfide (CdS) was the material that used for the thin-film and silicon monoxide as the insulator [26]. The analysis of the device characteristics was realized by Borkan and Weimer (Borkan and Weimer, 1963), based on Shockley's JFET analysis [26, 34].

In the 70's, two very important events changed dramatically the prospects for TFTs. The first was the implementation of a thin-film semiconductor instead of crystalline bulk silicon material, like Cadmium Selenide (CdSe). The impact of this implementation was the reduction of the fabrication cost and the decrease of the transistor size. The second landmark was the Active Matrix addressing method proposed by (Lechner et al., 1971) and the fact that the switch device needed in each pixel of the matrix can be materialized with the use of a TFT device [26, 34].

The CdSe TFT LCD was first demonstrated in 1973 [27, 34]. However, mass production of this kind of LCD on large-area substrates has never been realized. Among many possible reasons, complications in controlling the compound semiconductor thin film material properties and device reliability over large areas are often discussed [27].

In 1975, they demonstrated that the p/n channels of an amorphous semiconductor thin film deposited by glow discharge plasma chemical vapor deposition (CVD) can be controlled. This indicated that the electrical characteristics of the a-Si semiconductor can be controlled by doping phosphorus (P) or boron (B) impurities because dangling bonds are terminated by hydrogen in the a-Si:H thin film [30, 35].

In 1981, they showed that a-Si TFTs can be used to drive liquid crystal displays (LCDs) [30, 36]. This finding greatly accelerated the research and development of a-Si TFTs. Since 1982, many prototypes a-Si TFT LCDs have continuously been put out by various panel manufacturers. In 1983, Sharp released a prototype 3-in. full-color LCD panel. With the aim of mass production and practical application, the 3-in. the color TV was developed in 1986, and its production and sale were started in 1987. Furthermore, in 1988, Sharp developed a 14-in. TFT LCD and demonstrated that a-Si TFT LCDs are flat panel displays (FPDs) that will replace cathode ray tube (CRT) displays and become the mainstream of next-generation displays [30].

The production of the first-generation (G1)-size TFT LCD panels was started in 1987. In 2009, Sharp Sakai Factory (Osaka) started producing LCD panels using G10-size glass [30].

I.4.2 TFT structure

TFTs can be seen as a class of FETs where comprising three terminals (gate, source, and drain) and including semiconductive, dielectric, and conductive layers. The semiconductor is placed between source/drain electrodes and the dielectric. This last is located between the gate electrode and the semiconductor. The main idea in this device is to control the current between drain and source (I_{DS}) by varying the potential between gate and source (V_{GS}), inducing free charge accumulation at the dielectric/semiconductor interface [37, 38].

Due to the flexibility in the thin film deposition process, TFTs can be prepared as various structures, e.g., depending on the relative position of the gate and the source/drain electrodes and whether a channel passivation layer is required leading to two basic types of TFT structures [26].

The first major structural distinction in the TFTs is the arrangement of the electrodes [26]:

- Coplanar where the source and drain electrodes are located on the same side as the gate electrode.

- Staggered where the source and the drain electrodes are located at the opposite side to the gate electrode separated with the semiconductor layer.

The second major distinction of the TFT is the level of the gate electrode [26]:

- The top gate where the gate is located above the semiconductor layer.

- The bottom gate where the gate is located below the semiconductor layer.

With these two distinctions, depending on the location of the layers, the basic TFT structures are divided into four sections as shown in Figure I.5 [39]. They can either be staggered or coplanar (whether drain/source and gate are on opposite or on the same side regarding the semiconductor) and, inside them, top or bottom gate (according to the location of the gate) [39].

(a) Top-gate staggered

(b) Top-gate coplanar

(c) Bottom-gate staggered
Semiconductor
Dielectric
S
Gate
D
Substrate

(d) Bottom-gate coplanar
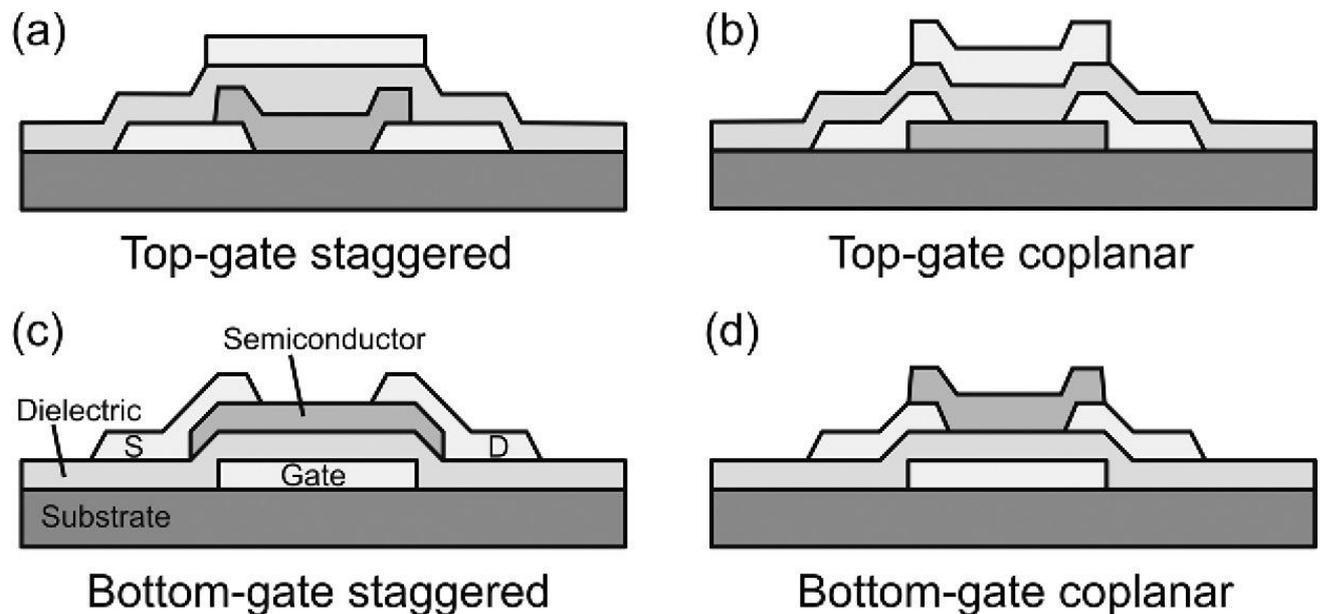
Figure I.5 The most typical TFT structures depending on the positioning of layers: (a) top-gate staggered, (b) top-gate coplanar, (c) bottom-gate staggered, (d) bottom-gate coplanar TFT configurations [39].

The flat panel manufacturers mainly use the bottom gate TFT technology because this structure is made with fewer lithography masks which lowering production costs [26].

In general, the TFT-fabrication process can be classified and described as follows [37, 40]: formation of the gate electrode, gate oxide, active layer, and source-drain electrodes.

I.4.3 Output parameters

The principal electrical characteristics of TFT are the drain current-gate voltage ($I_{DS} - I_{GS}$) at a different drain voltage (V_{DS}), known by transfer characteristic and the drain current-drain voltage ($I_{DS} - V_{DS}$) at a different gate voltage (V_{GS}), known by output characteristic. From the transfer characteristic, a number of output parameters are extracted as shown in Figure I.6 where [41-43]:

- The threshold voltage (V_T) is turn-on voltage in transfer characteristic of the transistor at the semi-logarithmic corresponds to minimum gate voltage required to create a strong inversion and thus achieving the conduction between drain and source. When the $V_{GS} = V_T$, only conduction channel is formed close to the semiconductor/dielectric interface between the source and drain electrodes and conduction takes place where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (gate) of the transistor. It can be positive or negative [44].

It can be extracted in several ways, such as a constant-current (CC) method, a match-point (MP) method, a second-derivative (SD) method, a third-derivative (TD) method, a current-to-square-root-transconductance ratio ($CTSRTR$) method and a linear extrapolation (LE) method [45]. The latter was used to calculate V_T [46]:

For the linear region: it consists of finding the gate voltage axis intercept (i.e., $I_{DS} = 0$) of the $I_{DS} - V_{GS}$ curve linear extrapolation at its maximum first derivative point. Then the value of V_T is often calculated by subtracting $V_{DS}/2$ from the resulting gate voltage axis intercept.

For the saturation region: the LE method, is similar to that in the linear region but it uses the $I_{DS}^{1/2} - V_{GS}$ characteristics instead.

This case (saturation), we can do without them in this study because it is considered filler.

- Subthreshold swing (SS) is the inverse of the maximum slope of the transfer characteristic. typically small values, $SS \ll 1$, result in higher speeds and lower power consumption. It can be written as follows [47, 48]:

$$\boldsymbol{SS = [\gamma']^{-1} = [(tg(\gamma))_{max}]^{-1} = \left[\left(\frac{\partial log(I_{DS})}{\partial V_{GS}}\right)_{max}\right]^{-1} \ll 1 \neq 0} \tag{I.6}$$

- Field-effect mobility (μ_{FE}) at the linear regime and saturation mobility (μ_{Sat}) at the saturation regime when the semiconductor close to the drain region becomes depleted. This mobility for

as-deposited a-ITZO TFT can exhibit poorer values [47, 49-51] while good quality a-ITZO that undergoes an annealing treatment (at 300 $C°$ and over) or an optimized deposition condition exhibits higher saturation mobility [52]. μ_{FE} is calculated in the linear regime (for $V_{DS} = 0.1 \ll V_{GS}$) from the slope of the transfer ($I_{DS} - V_{GS}$) characteristic curve of the transistor at the linear plot as follows [47]:

$$I_{DS} = \alpha^{'}(V_{GS} - V_T) \tag{I.7}$$

Where

$$\alpha^{'} = \frac{\mu_{FE} \cdot W \cdot C_i}{L} \cdot V_{DS} \tag{I.8}$$

Then:

$$\mu_{FE} = \frac{\alpha^{'} \cdot L}{W \cdot C_i \cdot V_{DS}} \tag{I.9}$$

Here, L and W are the length and width of the channel, respectively, while C_i is the capacitance per unit area that is given by [47]:

$$C_i = \frac{\varepsilon_0 \cdot k_{ox}}{T_{ox}} \tag{I.10}$$

where k_{ox} is the relative permittivity of the dielectric oxide, ε_0 is the permittivity of free space (the vacuum permittivity) and T_{ox} is the dielectric oxide thickness.

While μ_{Sat} is calculated in the saturation regime (for $V_{DS} = 10V \gg V_{GS}$) from the slope of the linear $I_{DS}^{1/2}(V_{GS})$ curve as follows [47]:

$$I_{DS}^{1/2} = \beta^{'}(V_{GS} - V_T) \tag{I.11}$$

where

$$\beta^{'} = \sqrt{C_i \cdot \mu_{Sat} \cdot \frac{W}{2L}} \tag{I.11}$$

Then:

$$\mu_{Sat} = \frac{2\beta^{' \, 2} \cdot L}{C_i \cdot W} \tag{I.13}$$

This case (saturation), we can also be dispensed in this study because it is considered filler.

- The on-state current (I_{on}) is the maximum I_{DS} in transfer characteristic at the semi-logarithmic plot [53].

- The off-state current (I_{off}) is the minimum I_{DS} in transfer characteristic at the semi-logarithmic plot [54].

- The on-off current ratio (I_{on}/I_{off}) is the characterizes how much the difference between the on state current (I_{on}) and off-state current (I_{off}) in transfer characteristic at the semi-logarithmic plot [55]. A ratio above 10^6 is typically obtained in TFT and a large value is required for their successful usage as electronic switches [56].

- Turn-on voltage (V_{on}) is a much more precise parameter to quantify the drain current onset than V_T [57]. Additional of Figure I.6 shows there is no compelling justification for selecting V_T as a meaningful indicator of the onset of the drain current.

Figure 1.6 is a brief reminder of the extraction method of these parameters.
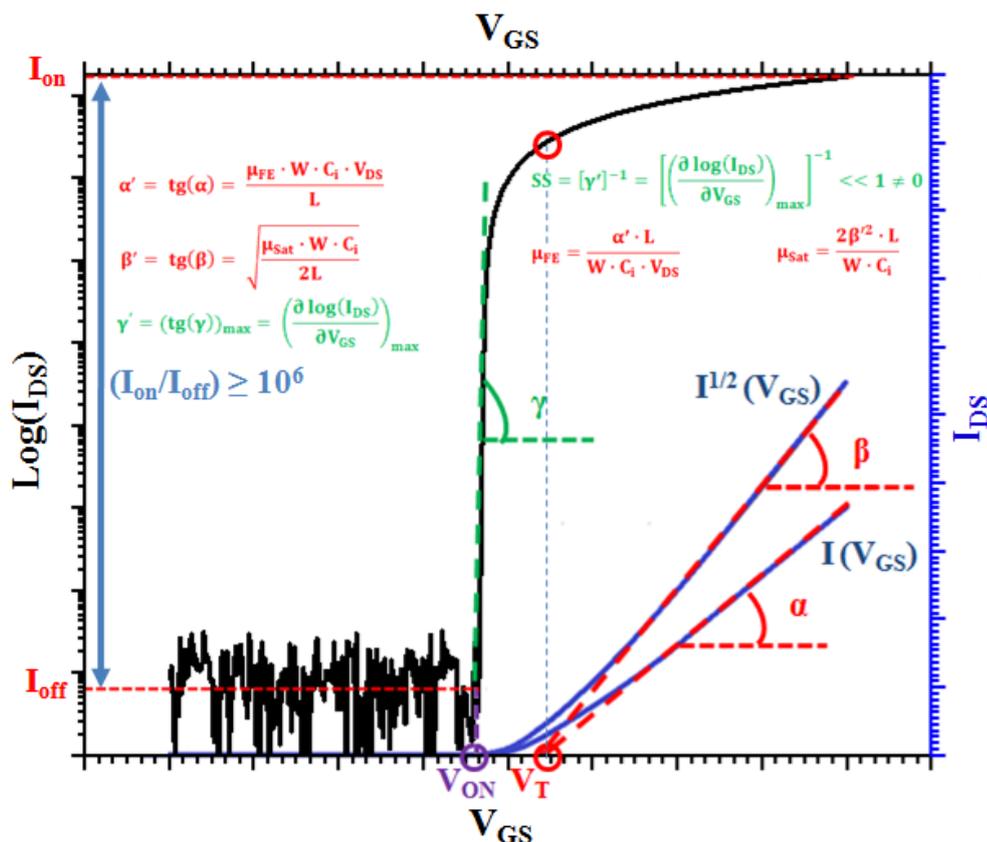
Figure I.6 The extraction methods of the a-ITZO TFT output parameters.

- The resistivity (ρ) of a-ITZO films is evaluated from the current-voltage ($I - V$) measurement plot. In this measurement, weestablished the current-voltage measurement and estimated the resistivity of the single layer of a-ITZO using the following equation [59]:

$$\rho = \frac{V}{I} \cdot \frac{W}{L} \cdot T \tag{I.14}$$

Where V and I are the input voltage and the output current, respectively, W and L are the width and length of the electrode, respectively, while T is the thickness of the a-ITZO layer.

I.5 Low-k dielectric materials

There are two primary approaches to achieve low-k dielectric materials. The first one is to lower the electronic contribution by the addition of fluorine (F) [60] and/or carbon (C) [61], which will provide the material with an inherently lower electronic polarizability. The second one is to lower the contribution due to the orientation and or the ionic contribution. This can

be done by the introduction of a free volume in a material, which will decrease the number of polarizable groups per unit volume and will lower the atomic or dipolar contributions. Generally, the low-k materials fall into three categories, namely inorganic, organic, and hybrid (organo-silicates). Dielectric materials due to their hydrophobic nature and low polarizability, organic dielectric materials show lower k values than inorganic materials. However, inorganic materials retain a SiO_2-like matrix, which helps them to integrate easily into the existing SiO_2-like processes. Hybrid materials, on the other hand, are typically doped with C to take advantages of both organic and inorganic regimes[62].

The variation in the dielectric constant is attributed to the frequency dependence of the polarization mechanisms that contribute to k. The polarizability and the k value of a dielectric material are generally results of the addition of three components (i.e., electronic + atomic + dipolar). One approach to reducing the k value of a dielectric is to introduce C or F atoms to increase the free volume of the matrix which will decrease the number of polarizable groups per unit volume. For example, in SiO_2 ($k = 3.9$), the introduction of C atoms to form SiCOH (k is between 2.7 and 3.3), and F atoms to form fluoro-silicate glass (k is between 3.2 and 4.0), and fluorinated polymides (k is in between 2.5 and 2.9), reduces its k value. On the other hand, hydroxyl and carbonyl groups are polar functional groups which can attract water via hydrogen bonding and thus drastically increase the dielectric constant (k of water ~ 78.5). Thus to formulate a low-k material polar functionality containing elements like oxygen or nitrogen should be avoided. The other approach that has been successfully implemented to reduce the k value is by introducing an air gap (k of air is 1) or pores [62].

The addition of pores in a dielectric material is particularly challenging because the percentage of pores needed for low-k dielectric materials is not an absolute number that can be applied to the film. Thus the overall dielectric constant of a material can be varied from that of

a dense material down to the value of air ($k = 1$) [63-65]. However, the porosity of a foam (static mixture) depends upon many factors, for example, pore diameter, distribution of microstructure, and thickness of the pores (Figure I.7).
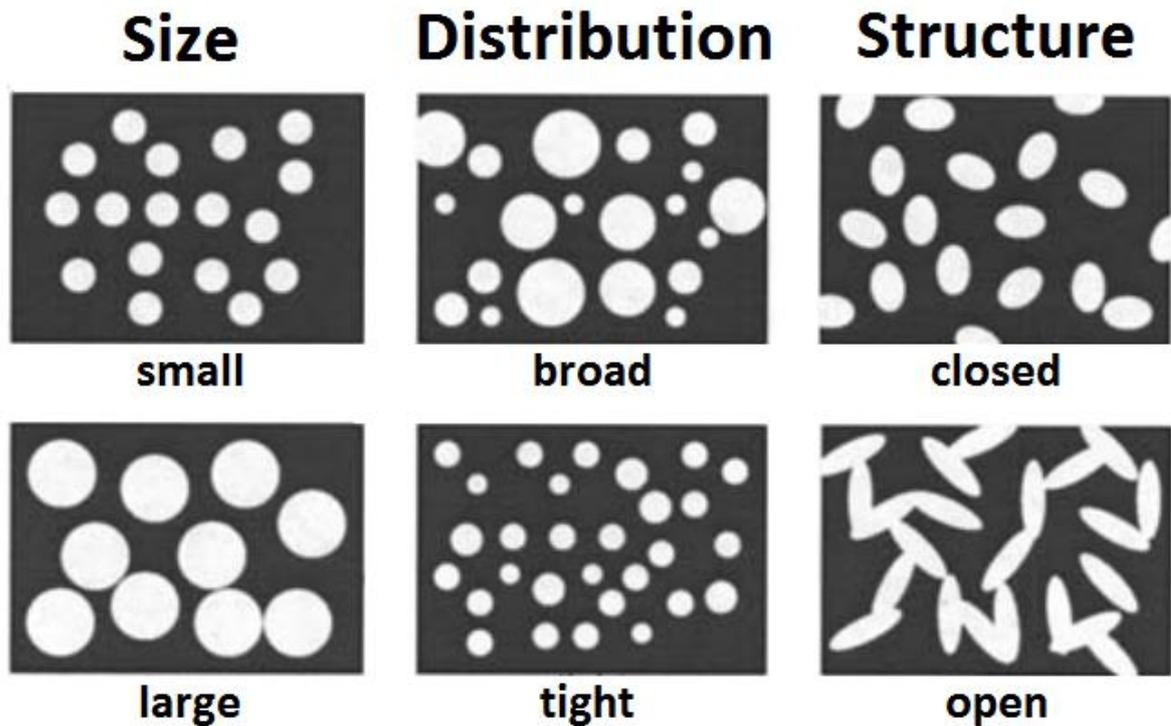
Figure I.7 Different sizes, distribution, and structure of pores inside a low-k porous dielectric material [66].

Table I.1 shows some of the promising low-k dielectric materials and their suitable deposition methods.

Dielectric material	Dielectric constant	Deposition process
Silicon dioxide (SiO_2)	$3.8 - 3.9$	PECVD
Carbon doped SiO_2	$2.2 - 2.7$	PECVD
Bezocyclobutane (BCB)	$2.49 - 2.65$	Spin-on
HSSQ	2.9	Spin-on
MSSQ	2.7	Spin-on
Polyarelene (PAE)	2.8	Spin-on
Parylene-N	2.8	CVD
Parylene-F	$2.3 - 2.5$	CVD
Teflon AF	$1.89 - 1.93$	Spin-on
Diamond like carbon (DLC)	$2.7 - 3.4$	PECVD
Fluorinated DLC	$2.4 - 2.8$	PECVD
Aromatic thermosets (SiLK)	$2.6 - 2.8$	Spin-on

Table I.1 Comparative analysis of deposition processes and dielectric constants of some low-k

dielectric materials [67].

I.6 High-k dielectric materials

The term high-k dielectric refers to a material with a high dielectric constant, as compared to silicon dioxide, used in semiconductor manufacturing processes which replaces the silicon dioxide gate dielectric. the implementation of high-k gate dielectrics is one of the several strategies developed to allow further miniaturization of microelectronic components.

Industry for semiconductors based devices in a combination with dielectrics, such as TFT, mainly depend on the gate dielectric material type, which will provide a very high-k, low leakage current and a low equivalent oxide thickness (EOT) compared to silicon dioxide (SiO_2) [60, 68-70]. The search is spurred by the urgency of minimizing power consumption, particularly in battery-driven high-performance $sub - 100\ nm$ devices [71-73]. As the thickness of SiO_2 approaches $< 1.5\ nm$, the leakage current becomes $> 1\ A/cm^2$ and the tunnel

current is seen to increase significantly. Therefore, it is expected that the future high-k materials for $sub - 100\ nm$ node technology should provide excellent electrical characteristics such as dielectric constant $(k) > 30$, interface density $< 1 \times 10^{11}\ cm^{-2}/eV$, tunneling current $< 1\ mA/cm^2$, and negligible hysteresis [74–76]. An important issue preventing the implementation of high-k gate material is charge trapping in pre-existing traps inside the dielectric material, which affects the threshold voltage [17].

Replacing the silicon dioxide gate dielectric with another material adds complexity to the manufacturing process. Silicon dioxide can be formed by oxidizing the underlying silicon, ensuring a uniform, conformal oxide and high interface quality [77]. As a consequence, development efforts have focused on finding a material with a requisitely high dielectric constant that can be easily integrated into a manufacturing process. Other key considerations include band alignment to silicon (which may alter leakage current), film morphology, thermal stability, Maintain a high mobility of charge carriers in the channel and minimization of electrical defects in the film and interface. Materials which have received considerable attention are $HfSiO_4$, $ZrSiO_4$, HfO_2, and ZrO_2, typically deposited using atomic layer deposition [77].

Table I.2 shows the comparative analysis of band gaps and dielectric constants of different promising high-k materials.

Dielectric material	Band gap(eV)	Dielectric constant	Ref
Si_3N_4	5	7.5	[78, 79]
Al_2O_3	8.7	8.5-10.5	[80]
$ZrSiO_4$	~ 6	10-12	[80]
$Hf_xSi_{1-x}O_y$	6	15-25	[81]
ZrO_2	5.8	25	[82-84]
HfO_2	5.7	35	[82]
$LaAlO_3$	5.7	25	[85]
La_2O_3	4.3	27	[78, 79]
Ta_2O_5	$4 - 4.5$	20-35	[86-89]
CeO_2	5.5	26	[90-92]
Y_2O_3	5.6	12-20	[93,94]
Nb_2O_5	-	50-200	[95-97]
TiO_2	$3 - 3.5$	30-100	[93, 98-101]

Table I.2 Comparative analysis of band gaps and dielectric constants of some high-k dielectric

materials.

I.7 Quantum mechanical tunneling and gate leakage

Gate leakage in a modern transistor occurs through a process called quantum mechanical tunneling [102-105]. Under normal condition, all the electrons are on the upstream side of the gate. Quantum mechanical tunneling occurs when the gate dimension is so thin that the electrons (or holes) have a certain statistical probability of being on the downstream side of the gate without actually sloshing over the gate. In modern transistors, the gate thickness is about five atomic layers. The thinner gate leads to a larger tunneling current and then higher power consumption [106-108].

The tunneling current can be reduced by increasing the physical thickness of the gate dielectric [109-112]. The problem here is that the increase of the physical thickness of the SiO_2

gate dielectric means that the electrical oxide thickness is increased, which reduces the transistor performance [113].

High-k dielectrics are used in the semiconductor-based device to replace SiO_2 gate dielectric or another dielectric layer of the device, as one of the several methods developed to allow further miniaturization of the device, colloquially referred to as extending Moore's Law [114-118].

SiO_2 used conventionally as a gate oxide material has a low k of 3.9. Many high-k (higher than 3.9) materials can be cited, such as oxides of the transition metals such as TaO_2, TiO_2, Al_2O_3, ZrO_2, and HfO_2, ferroelectric materials such as $BaSrTiO_3$, and metal silicates such as $ZrSiO_4$ and $HfSiO_4$.

Different parameters of TFTs such as channel length, channel width, gate oxide thickness, and other dimensions have been scaled down for improving performances. When the sizes approach $sub - 22\ nm$ range, several issues arise to make further scaling difficult. As transistors have decreased in size, the thickness of the SiO_2 gate dielectric has steadily decreased to increase the gate capacitance and thereby the current and performance of the device [118, 119].

However, as mentioned above, with thinner oxide the rate of tunneling gate leakage rises, which contributes to power dissipation and the device reliability is affected.

Besides the gate dielectric thickness, there are many other scaling problems, such as sensitivity to doping fluctuations, interface state and surface charges, different kinds of short-channel effects, quantum confinement in the inversion layer, and source-drain series resistance … etc, which can affect transistor characteristics in the sub-nm range. With planar technology, a channel length of $20\ nm$ is possible, but for practical application, most likely a $10\ nm$ channel length is the scaling limit, even for three-dimensional structures [120-122].

The rapid scaling of TFTs can be obtained by substituting the traditional gate oxide, SiO_2, with high-k dielectrics, which can maintain the same capacitance with much lower leakage current [123, 124].

I.8 Equivalent oxide thickness of the mono-layer dielectrics

By substituting a high-k dielectric material instead of the SiO_2 we can obtain a lower effective thickness (electrical thickness) of the gate dielectric that is referred to as the equivalent oxide thickness (EOT). EOT is a distance, usually given in nanometer (nm), which indicates how thick a SiO_2 film should be to produce the same effect as in use high-k material [125]. The term is often used to describe field effect transistors, which contain a dielectric material between the gate and the active channel region.

The conceptual advantage of a high-k dielectric can be monitored by considering a simple parallel plate capacitor as shown in Figure I.8(a, b).
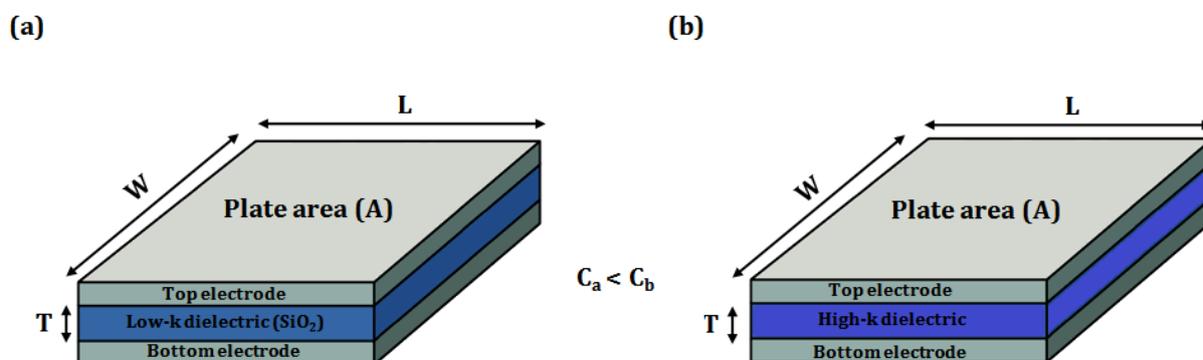
Figure I.8 Simplified representation of the three-dimensional structure of a simple parallel plate capacitor with (a) low-k dielectric and (b) high-k dielectric.

The capacitance of the structure in case (a) can be calculated according to the following equation [126]:

$$C_{ox} = C_{SiO_2} = \frac{\varepsilon_0 \cdot k_{SiO_2} \cdot L \cdot W}{T_{SiO_2}} = \frac{\varepsilon_{SiO_2} \cdot L \cdot W}{T_{SiO_2}} = \frac{\varepsilon_{SiO_2} \cdot A}{T_{SiO_2}} = (C_{ox})_{UA} \cdot A = (C_{SiO_2})_{UA} \cdot A \qquad (I.15)$$

where C_{ox} is the overall capacitance of the dielectric oxide, C_{SiO_2} is the capacitance of SiO2, ε_0 is the permittivity of free space (vacuum permittivity), k_{SiO_2} is the dielectric constant (relative permittivity) of SiO2, ε_{SiO_2} is the permittivity (absolute) of SiO_2, T_{SiO_2} is the thicknesses of SiO2, L and W are, respectively, the length and width of the dielectric oxide (or plates), A is the cross-section area of the dielectric oxide (or plates), $(C_{ox})_{UA}$ is the capacitance per unit area for dielectric oxide and $(C_{SiO_2})_{UA}$ is the capacitance per unit area for SiO2.

In this case, the equivalent oxide capacitance is given by the following expression [126]:

$$\boldsymbol{C_{EOT}} = \boldsymbol{C_{SiO_2}} = \frac{\varepsilon_0 \cdot k_{SiO_2} \cdot L \cdot W}{EOT} = \frac{\varepsilon_{SiO_2} \cdot L \cdot W}{EOT} = \frac{\varepsilon_{SiO_2} \cdot A}{EOT} = (\boldsymbol{C_{ox}})_{UA} \cdot \boldsymbol{A} = (\boldsymbol{C_{SiO_2}})_{UA} \cdot \boldsymbol{A} \qquad (I.16)$$

where C_{EOT} and $(C_{EOT})_{UA}$ are the capacitance and capacitance per unit area for the equivalent oxide thickness (EOT).

For SiO2 dielectric:

$$\boldsymbol{EOT} = \frac{\varepsilon_0 \cdot k_{SiO_2} \cdot L \cdot W}{C_{SiO_2}} = \frac{\varepsilon_{SiO_2} \cdot L \cdot W}{C_{SiO_2}} = \frac{\varepsilon_{SiO_2} \cdot A}{C_{SiO_2}} = \frac{\varepsilon_{SiO_2} \cdot A}{\frac{\varepsilon_{SiO_2} \cdot A}{T_{SiO_2}}} = \boldsymbol{T_{SiO_2}} \qquad (I.17)$$

In the case of the use of a high-k dielectric (Figure I.8.b) EOT decreases while the capacitance increases for the same physical thickness as shown by the following expression:

$$\boldsymbol{C_{ox}} = \boldsymbol{C_{high-k-ox}} = \frac{\varepsilon_0 \cdot high-k \cdot L \cdot W}{T_{high-k-ox}} = \frac{\varepsilon_{high-k-ox} \cdot L \cdot W}{T_{high-k-ox}} = \frac{\varepsilon_{high-k-ox} \cdot A}{T_{high-k-ox}} = (\boldsymbol{C_{high-k-ox}})_{UA} \cdot \boldsymbol{A} \qquad (I.18)$$

Then :

$$\boldsymbol{T_{high-k-ox}} = \frac{\varepsilon_0 \cdot high-k \cdot L \cdot W}{C_{high-k-ox}} = \frac{\varepsilon_{high-k-ox} \cdot L \cdot W}{C_{high-k-ox}} = \frac{\varepsilon_{high-k-ox} \cdot A}{C_{high-k-ox}} \qquad (I.19)$$

Consequently, for the same physical thickness of the high-k dielectric and SiO2 we found:

$$\boldsymbol{C_{high-k-ox}} = \frac{high-k}{k_{SiO_2}} \cdot \boldsymbol{C_{SiO_2}} \qquad (I.20)$$

The $\frac{high-k}{k_{SiO_2}}$ ratio is greater than one, which implies that the capacitance for the high-k dielectric is greater than the capacitance for SiO2 for the same physical thickness.

On the other hand, the most high-k dielectrics have smaller band gap energy than SiO_2, which implies that more current can leak between the plates if the high-k dielectric is not thick enough [126, 127]. Therefore, it is necessary to increase the physical thickness of the high-k dielectric.

(a)   **(b)**
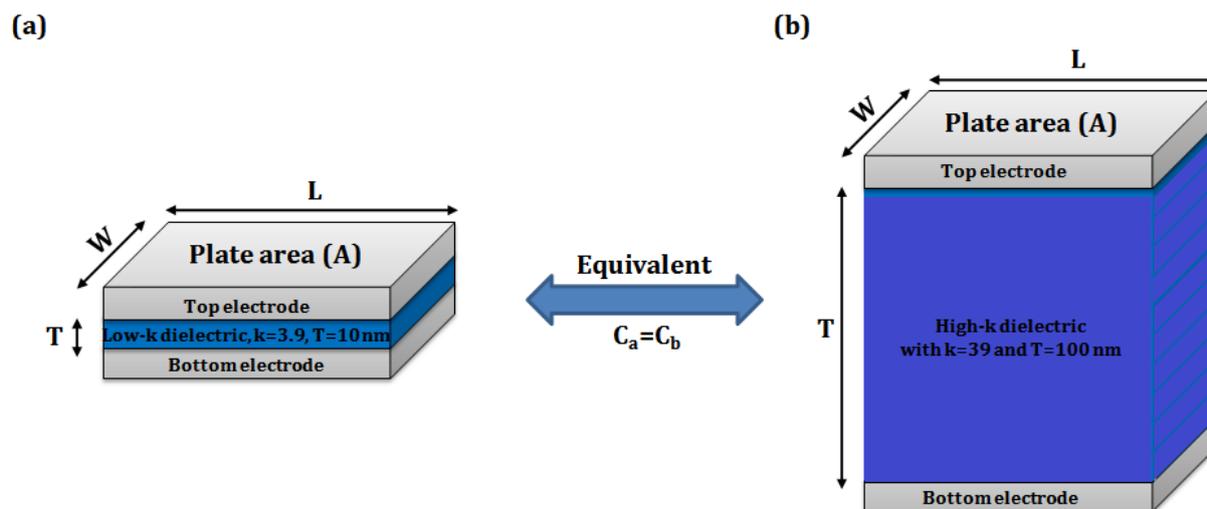
Figure I.9 Simplified representation of the three-dimensional parallel plate capacitor (a) with a low-k dielectric and (b) with a high-k thicker dielectric.

The equivalent oxide thickness EOT of a high-k dielectric can then be written as follows [104]:

$$EOT = \frac{\varepsilon_0 \cdot k_{SiO_2} \cdot A}{\frac{\varepsilon_0 \cdot high-k \cdot A}{T_{high-k-ox}}} = \frac{k_{SiO_2}}{high-k} \cdot T_{high-k-ox} \tag{I.21}$$

For example, a high-k dielectric with a dielectric constant ($k = 39$) can be 10 times more thickness than SiO_2, which helps to reduce the current leakage and at the same time maintain the same capacitance per unit area (Figure I.9). Furthermore, by using a high-k dielectric with a wide band gap such as Al_2O_3 ($E_g = 8.7\ eV, k = 9.5$) it is possible to increase the capacitance per unit area in addition to the current leakage reduction.

I.9 Equivalent oxide thickness of bi-layer gate dielectrics

As is well known, the proper choice of a dielectric material is crucial to define the performance/reliability of any TFT technology. As well, the semiconductor films deposited by lower temperature processes are more prone to have higher densities of defects and reduced compactness, which can be compensated by the larger capacitive injection of high-dielectric-constant (high-k) dielectrics [128].

On the other hand, dielectrics with good capacitance per unit area can still be achieved even if their thickness is increased, compensating the degraded insulating properties of dielectrics fabricated at lower temperatures [128].

Generally, the formation of a bi-layer dielectric structure by adding a high-k dielectric oxide layer to a low-k dielectric oxide layer provides a lower effective thickness (a lower electrical thickness) of the gate dielectrics that is referred to as the equivalent oxide thickness (EOT). At the same time a large physically thickness is obtained with a good semiconductor/dielectric interface quality, which preserves the gate capacitance or even increase it with preventing (or reducing) the gate current leakage then get a better performance of the TFT.

The equivalent capacitance for an oxide consists of two different dielectric layers in series is given by [129]:

$$\frac{1}{C_{ox}} = \frac{1}{C_{low-k-ox}} + \frac{1}{C_{high-k-ox}} \tag{I.22}$$

Then:

$$C_{ox} = \frac{1}{\frac{1}{C_{low-k-ox}} + \frac{1}{C_{high-k-ox}}} \tag{I.23}$$

Here:

$$C_{ox} = C_{EOT} = \frac{\varepsilon_0 \cdot low-k \cdot L \cdot W}{EOT} = \frac{\varepsilon_{low-k-ox} \cdot L \cdot W}{EOT} = \frac{\varepsilon_{low-k-ox} \cdot A}{EOT} = (C_{ox})_{UA} \cdot A = (C_{EOT})_{UA} \cdot A \tag{I.24}$$

$$C_{low-k-ox} = \frac{\varepsilon_0 \cdot low-k \cdot L \cdot W}{T_{low-k-ox}} = \frac{\varepsilon_{low-k-ox} \cdot L \cdot W}{T_{low-k-ox}} = \frac{\varepsilon_{low-k-ox} \cdot A}{T_{low-k-ox}} = (C_{low-k-ox})_{UA} \cdot A \tag{I.25}$$

$$C_{high-k-ox} = \frac{\varepsilon_0 \cdot high-k \cdot L \cdot W}{T_{high-k-ox}} = \frac{\varepsilon_{high-k-ox} \cdot L \cdot W}{T_{high-k-ox}} = \frac{\varepsilon_{high-k-ox} \cdot A}{T_{high-k-ox}} = (C_{high-k-ox})_{UA} \cdot A \qquad (I.26)$$

where k is the dielectric constant of the material, ε_0 is the permittivity of free space (vacuum), ε is the permittivity of the dielectric material, C_{ox} is the equivalent capacitance of the bi-layer dielectric oxide, C_{EOT} is the capacitance of the equivalent oxide of the gate dielectrics, $(C_{ox})_{UA}$ and $(C_{EOT})_{UA}$ are the capacitances per unit area for each of the dielectric oxide layers and the equivalent oxide of the bi-layer dielectric, respectively, $C_{low-k-ox}$ and $C_{high-k-ox}$ are the capacitances for each of the low-k dielectric oxide and high-k dielectric oxide, respectively, $\varepsilon_{low-k-ox}$ and $\varepsilon_{high-k-ox}$ are the low-k dielectric oxide and high-k dielectric oxide permittivity's, respectively, L and W are, respectively, the length and width of the dielectric oxide and A is the cross-section area of the dielectric oxide while $T_{low-k-ox}$ and $T_{high-k-ox}$ are the low-k dielectric oxide and high-k dielectric oxide thicknesses, respectively.

From this standpoint we can derive the general expression of EOT for an oxide consists of two dielectrics in series, which is given by [129]:

$$EOT = T_{low-k-ox} + \frac{low-k}{high-k} \cdot T_{high-k-ox} \qquad (I.27)$$

While the general expression of the physical thickness (PT) of the gate dielectric of TFT for an oxide consists of two dielectrics in series is given by:

$$PT = T_{low-k-ox} + T_{high-k-ox} \qquad (I.28)$$

Then:

$$PT = T_{ox} \qquad (I.29)$$

where T_{ox} is the thickness of the bi-layer dielectric oxides.

For example, for SiO_2/Si_3N_4 dielectric, the expression of EOT is written as follows:

$$EOT = T_{SiO_2} + \frac{k_{SiO_2}}{k_{Si_3N_4}} \cdot T_{Si_3N_4} \qquad (I.30)$$

where k_{SiO_2} and $k_{Si_3N_4}$ are the dielectric constants for each of SiO₂ and Si₃N₄, respectively. T_{SiO_2} and $T_{Si_3N_4}$ are the thicknesses of SiO₂ and Si₃N₄, respectively.

In this case, the overall capacitance for the SiO₂/Si₃N₄ is given by:

$$C_{ox} = \frac{\varepsilon_0 \cdot k_{SiO_2} \cdot A}{EOT} = \frac{\varepsilon_{SiO_2} \cdot A}{EOT} \tag{I.31}$$

where ε_{SiO_2} is permittivity of *SiO₂*.

While the expression of the physical thickness (*PT*) of the gate dielectric (SiO₂/Si₃N₄) in TFT is given by:

$$PT = T_{SiO_2} + T_{Si_3N_4} \tag{I.32}$$

Despite the fact that most of the bi-layer dielectric oxides have a relatively large EOT, but that this technology high relevant not only for scaling down transistor sizes, but also low-temperature technologies, without neglecting the fundamental role of the interfacial layer of low-k dielectric oxide between the high-mobility channel and the high-k dielectric oxide layer, which has some beneficial qualities with regard to carrier mobility in the device channel [130-137].

An overall picture without overlooking some of the negative aspects of this technology, the combination of all these factors that we have mentioned previously enables low-temperature TFTs with low operating voltage, steep subthreshold regions and high-mobility [138, 140].

(a)   **(b)**
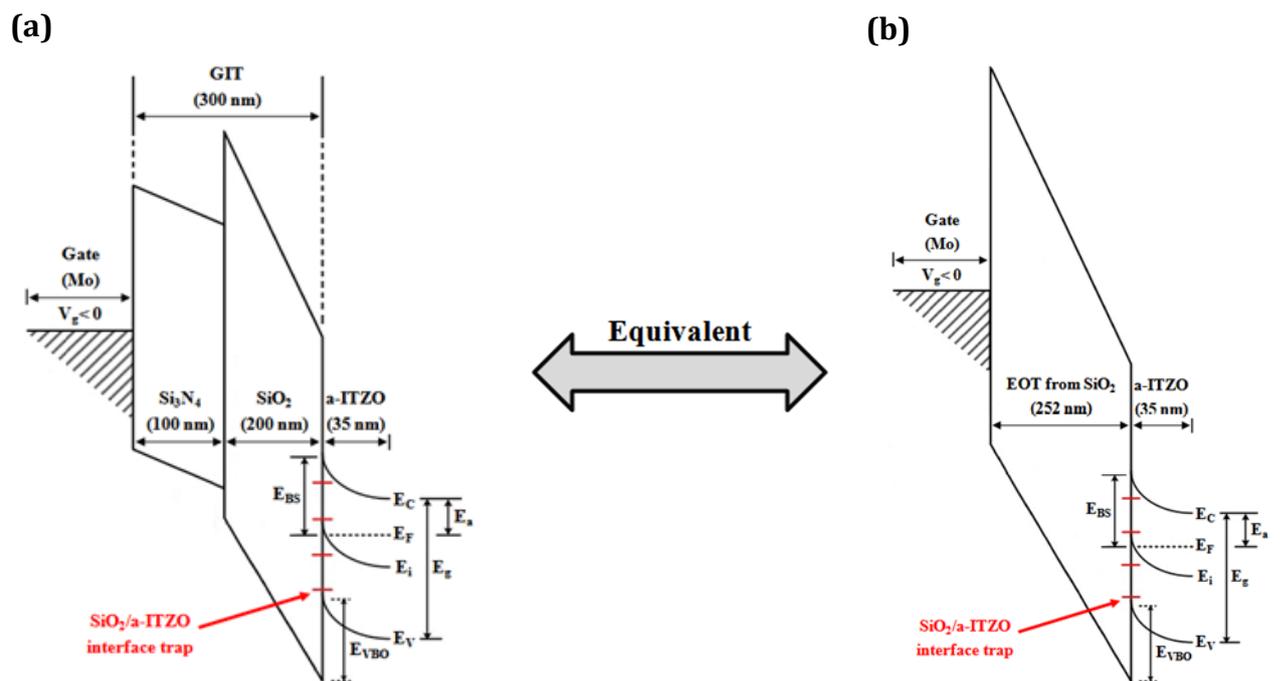
Figure I.10 The energy band diagram of the semiconductor/dielectric interface in a-ITZO TFT

where (a) shows the energy band diagram of the semiconductor/double-layered dielectric

oxide (a-ITZO/SiO$_2$/Si$_3$N$_4$) interface in a-ITZO TFT while (b) shows the energy band diagram of

the semiconductor/mono-layer equivalent dielectric oxide (a-ITZO/equivalent SiO$_2$) interface

in a-ITZO TFT [1].

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Chapter

2

Silvaco Atlas for TFT simulation

II.1 Introduction

Silvaco Atlas is a physically-based device simulator. Physically-based device simulators predict the electrical characteristics that are associated with specified physical structures and bias conditions. This is achieved by approximating the operation of a device onto a two or three-dimensional grid, consisting of a number of grid points called nodes. By applying a set of differential equations, derived from Maxwell's laws, to this grid, we can simulate the transport of carriers through a structure [1].

Physically-based simulation has become very important because of it quicker and cheaper than performing experiments, as it also provides information that is difficult or impossible to measure them empirically [1].

The main purpose of this chapter is to conduct a comprehensive theoretical study on the numerical simulation of TFT by Silvaco Atlas. For this purpose, we have carried out a bibliographic study on Silvaco Atlas and numerical simulation for TFT.

II.2 Amorphous semiconductors and defect states

Silvaco Atlas it can simulate the disordered material systems and the structure of TFT devices based on these material systems [2, 3]. We can also by Atlas define an energy distribution of continuous defect states in the band gap of amorphous semiconductor materials and use them in the simulation [4]. This is necessary for the accurate treatment of the electrical properties of materials (as a-Si:H, a-IGZO, and a-ITZO) and devices based on them.

Disordered materials contain a large number of defect states within the band gap of the material [5]. To accurately model devices made of amorphous materials, use a continuous density of states as a combination of exponentially decaying band tail states and Gaussian

distributions of mid-gap states [6]. In addition, We may need to interface model as a thermionic field emission boundary [7].

II.3 The nature of the physically-based simulation

Atlas is a physically-based device simulator. Physically-based device simulation is not a familiar concept for all engineers. Physically-based device simulators predict the electrical characteristics that are associated with specified physical structures and bias conditions. This is achieved by approximating the operation of a device onto a two or three-dimensional grid, consisting of a number of grid points called nodes. By applying a set of differential equations, derived from Maxwell's laws, to this grid, we can simulate the transport of carriers through a structure. Physically-based simulation is different from empirical modeling. The goal of empirical modeling is to obtain analytic formulae that approximate existing data with good accuracy and minimum complexity [1].

Physically-based simulation has become very important for two reasons. One, it is almost always much quicker and cheaper than performing experiments. Two, it provides information that is difficult or impossible to measure. The drawbacks of the physically-based simulation are that all the relevant physics must be incorporated into a simulator. Also, numerical procedures must be implemented to solve the associated equations. These tasks have been taken care of for Atlas users. Those who use physically-based device simulation tools must specify the problem to be simulated [1]. In Atlas, specify device simulation problems by defining [1]:

- The physical structure to be simulated.

- The physical models to be used.

- The bias conditions for which electrical characteristics are to be simulated.

To define a device through the Atlas command language, we must first define a mesh. This mesh or grid covers the physical simulation domain. The mesh is defined by a series of horizontal and vertical lines and the spacing between them. Then, regions within this mesh are allocated to different materials as required to construct the device. After the regions are defined, the location of electrodes is specified. The final step is to specify the doping in each region [1].

II.4 Atlas inputs and outputs

Figure II.1 shows the types of information that flow in and out of Atlas. Most Atlas simulations use two input files. The first input file is a text file that contains commands for Atlas to execute. The second input file is the structure file that defines the structure that will be simulated. Atlas produces three types of output files. The first type of output file is the run-time output, which gives we the progress and the error and warning messages as the simulation proceeds. The second type of output file is the log file, which stores all terminal voltages and currents from the device analysis. The third type of output file is the solution file, which stores two-dimensional (2D) and three-dimensional (3D) data relating to the values of solution variables within the device at a given bias point [1].
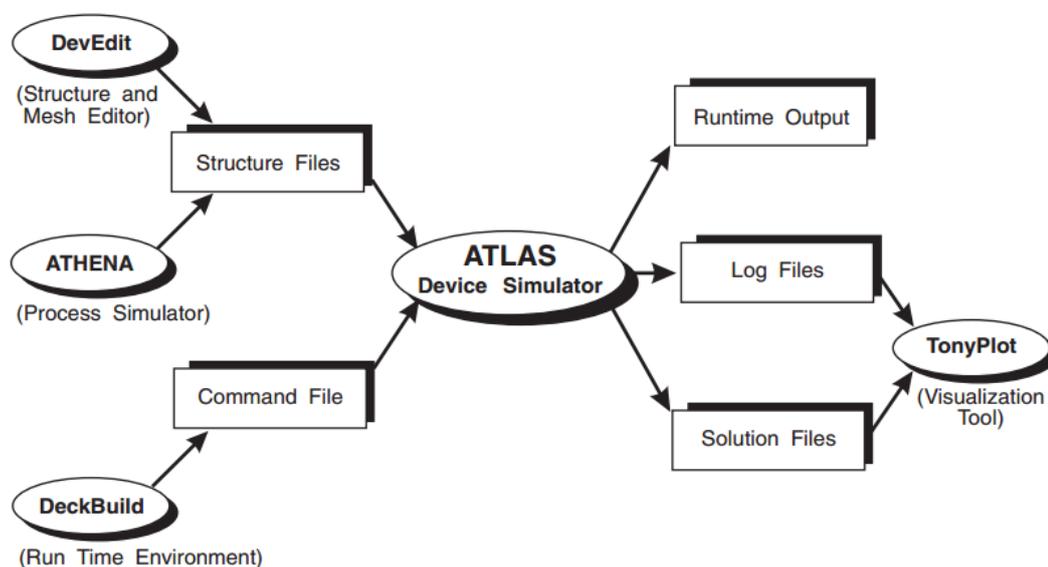
Figure II.1 Atlas inputs and outputs [1].

II.5 Transport models

There are many different transport models such as the drift-diffusion model, the drift-diffusion model, the advanced energy balance transport model or the hydrodynamic model. Although the simplest model of charge transport that is useful is the drift-diffusion model, but Atlas supplies both drift-diffusion and advanced energy balance transport models because they possess attractive advantages [1].

II.5.1 Drift-diffusion transport model

Atlas supplies drift-diffusion transport model Although it is less accurate for smaller feature sizes (for simulating deep submicron devices) because it is adequate for nearly all devices that were technologically feasible [8].

Derivations based upon the Boltzmann transport theory shown that the current densities in the continuity equations may be approximated by a drift-diffusion model [8].

In this case, the current densities are expressed in terms of the quasi-Fermi levels ϕ_n and ϕ_p as [9]:

$$\vec{j}_n = -q\mu_n n \nabla \phi_n \tag{II.1}$$

$$\vec{j}_p = -q\mu_p p \nabla \phi_p \tag{II.2}$$

Where $\vec{j}_n$ and $\vec{j}_p$ are the electron and hole current densities, respectively, q is the electron charge, μ_n and μ_p are the electron and hole mobilities, respectively, n and p are free electron and hole carrier concentrations, respectively.

The quasi-Fermi levels are linked to the carrier concentrations and the potential through the two Boltzmann approximations as [9]:

$$n = n_i exp\left[\frac{q(\Psi - \phi_n)}{kT_L}\right] \tag{II.3}$$

$$p = n_i exp\left[-\frac{q(\Psi - \phi_p)}{kT_L}\right] \tag{II.4}$$

where n_i is the intrinsic carrier concentration, Ψ is the electrostatic potential and T_L is the lattice temperature.

These two equations may then be re-written to define the quasi-Fermi potentials (the quasi-Fermi levels) as [9]:

$$\phi_n = \Psi - \frac{kT_L}{q} ln \frac{n}{n_i} \tag{II.5}$$

$$\phi_p = \Psi + \frac{kT_L}{q} ln \frac{p}{n_i} \tag{II.6}$$

By substituting these equations into the current density expressions, the following adapted current relationships are obtained [1]:

$$\vec{j}_n = qD_n \nabla \mathbf{n} - qn\mu_n \nabla \Psi - \mu_n n\left(kT_L \nabla(lnn_i)\right) \tag{II.7}$$

$$\vec{j}_p = -qD_p \nabla \mathbf{p} - qp\mu_p \nabla \Psi + \mu_p p\left(kT_L \nabla(lnn_i)\right) \tag{II.8}$$

Where D_n and D_p are the diffusion coefficients for electrons and holes, respectively.

We can express current densities in terms of electron and hole effective electric fields $(\vec{E}_n$ and $\vec{E}_p)$ by a more conventional formulation of drift-diffusion equations as [10]:

$$\vec{j}_n = qn\mu_n \vec{E}_n + qD_n \nabla \mathbf{n} \tag{II.9}$$

$$\vec{j}_p = qp\mu_p \vec{E}_p - qD_p \nabla \mathbf{p} \tag{II.10}$$

Here, the effective electric field equations are given by [10]:

$$\vec{E}_n = -\nabla(\Psi + \frac{KT_L}{q} lnn_i) \tag{II.11}$$

$$\vec{E}_p = -\nabla(\Psi + \frac{KT_L}{q} lnn_i) \tag{II.12}$$

It should be noted That the derivation of the drift-diffusion model has tacitly assumed that the Einstein relationship holds [11, 12].

II.5.2 Advanced energy balance transport model

Energy balance transport model a more advanced drift-diffusion transport model, thus becoming more popular for simulating deep submicron devices [1].

In this model, are modified to include this additional physical relationship to electron and hole current flux densities expressed as [1, 10]:

$$\vec{J}_n = qD_n\nabla n - qn\mu_n\nabla\Psi + qnD_n^T\nabla T_n \tag{II.13}$$

$$\vec{J}_p = qD_p\nabla p - qp\mu_p\nabla\Psi - qpD_p^T\nabla T_p \tag{II.14}$$

Here, T_n and T_p are the carrier temperatures for electrons and holes, respectively. D_n and D_p are the thermal diffusivities for electrons and holes, respectively. $D_n^T\nabla T_n$ and $D_p^T\nabla T_p$ are the net thermal diffusivities for electrons and holes, respectively.

II.6 The order of Atlas commands

The order in which statements occur in an Atlas input file is important. There are five groups of statements that must occur in the correct order (Table II.1). Otherwise, an error message will appear, which may cause incorrect operation or termination of the program. For example, if the material parameters or models are set in the wrong order, then they may not be used in the calculations. The order of statements within the mesh definition, structural definition, and solution groups is also important. Otherwise, it may also cause incorrect operation or termination of the program [1].

Group	Statements
Structure specification	MESH
	REGION
	ELECTRODE
	DOPING
Material models specification	MATERIAL
	MODELS
	CONTACT
	INTERFACE
Numerical method Selection	METHOD
Solution specification	LOG
	SOLVE
	LOAD
	SAVE
Results analysis	EXTRACT
	TONYPLOT

Table II.1 Atlas command groups with the primary statements in each group [1].

II.6.1 Structure specification

It is the first group in the Atlas commands file that contains four statements. These statements should be arranged as follows:

- MESH

- REGION

- ELECTRODE

- DOPING

II.6.1.1 Mesh

The specification of meshes involves a trade-off between the requirements of accuracy and numerical efficiency. Accuracy requires a fine mesh that can resolve all significant features of the solution. Numerical efficiency requires a coarse mesh that minimizes the total number of

grid points. This trade-off between accuracy and numerical efficiency is frequently a source of problems for beginners. Fortunately, enough experience to define reasonable meshes is soon acquired [1].

Atlas uses triangular meshes. Some triangulations yield much better results than others. Mesh generation is still an inexact science. Guidelines and heuristics, however, for defining satisfactory meshes exist. Good triangulations have the following features [1]:

- They contain enough points to provide the required accuracy.

- They do not contain too many unnecessary points that impair efficiency.

- They avoid or at least minimize, the number of obtuse triangles. Obtuse triangles tend to impair accuracy, convergence, and robustness.

- They avoid or at least minimize, the number of long, thin triangles. These triangles also tend to impair accuracy, convergence, and robustness.

- They allow the average size of triangles to change smoothly in the transition from a region where very small triangles must be used to a region where the use of much larger triangles is acceptable.

The error associated with a mesh can be investigated systematically by repeating a calculation using a sequence of finer meshes. This is very time consuming and is hardly ever done. The typical approach is to adequately resolve structural features, including doping, with an initial or base mesh, and then add nodes as required to resolve significant features of the solution. The insertion of additional nodes (re-gridding) is normally done by the program using user-specified criteria [1].

II.6.1.1.1 WIDTH parameter in MESH statement

The WIDTH is the device width (the width of the layers) in microns defined on the MESH statement. The electrode current is multiplied by the value of WIDTH before being saved in the logfile. When the WIDTH parameter in the MESH statement is used, the current is scaled

by this factor and is in Amperes. This is an optional parameter. All currents through Atlas device terminals calculated using the 2D Atlas model will be multiplied by this parameter to account for the third dimension of the device. width can still be used as a multiplier to the Atlas current if a 3D Atlas structure is used [1].

The WIDTH in the MESH statement is defined as follows:

MESH WIDTH=<n>

For example:

MESH WIDTH=10

II.6.1.1.2 Mesh definition

The Mesh can be defined as follows:

```
x.m l=<n> s=<n>
x.m l=<n> s=<n>
 .    .       .
 .    .       .
 .    .       .
y.m l=<n> s=<n>
y.m l=<n> s=<n>
 .    .       .
 .    .       .
 .    .       .
```
For example, the MESH shown in Figure II.2 can be defined as follows:

```
x.m l=0  s=0.25
x.m l=25 s=0.25
y.m l=0  s=0.0005
y.m l=0.020 s=0.005
y.m l=0.120 s=0.01
```
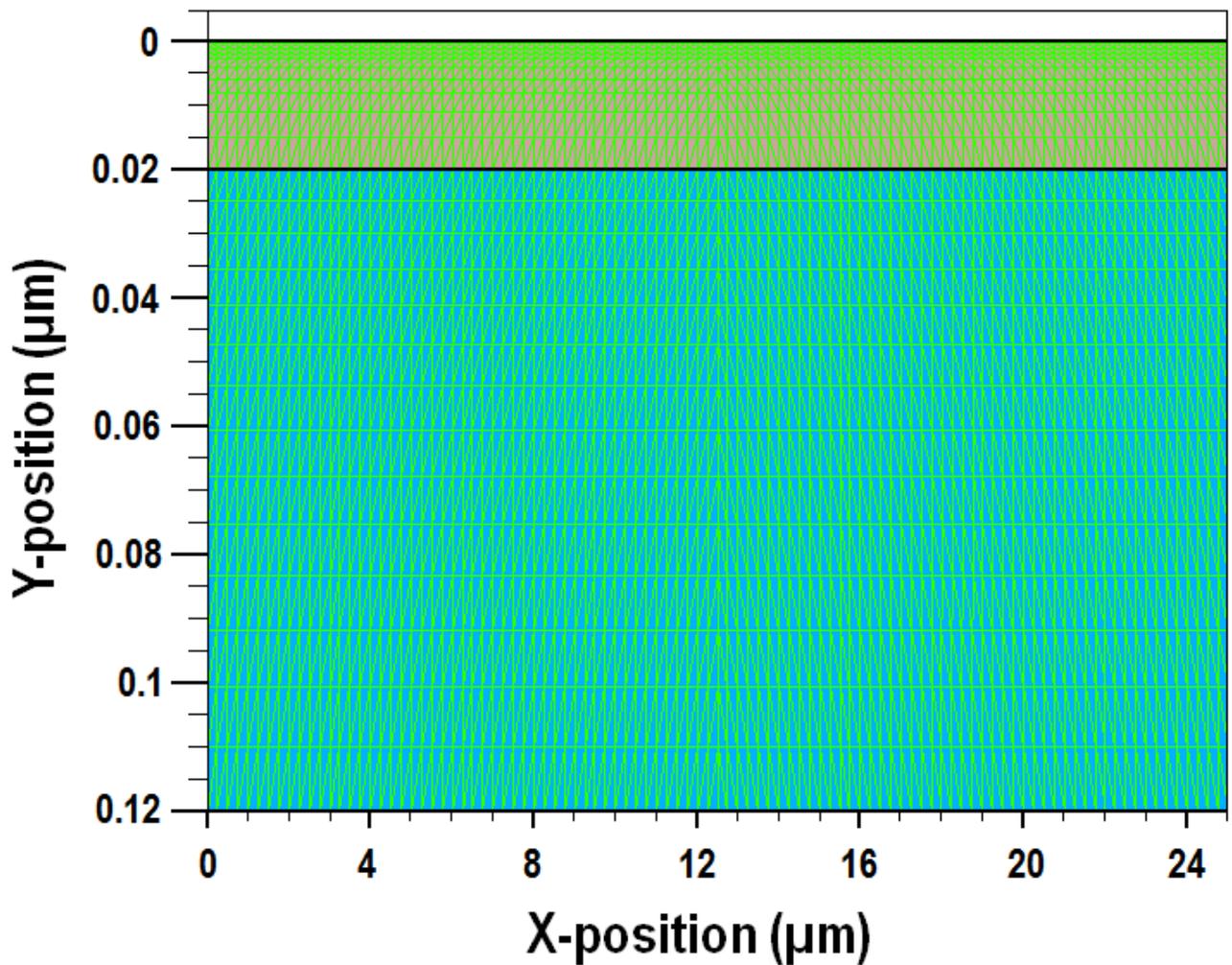
Figure II.2: Schematic diagram of the mesh generated by Silvaco Atlas.

II.6.1.2 Region

II.6.1.2.1 REGION definition

REGION is an integer parameter taking only integer numbers as input. Specifies the X and Y coordinates as cross-hairs to pin-point a region. Region numbers must start at 1 and are increased for each subsequent region statement. We can have up to 15000 different regions in Atlas. A large number of materials is available [1].

II.6.1.2.2 Specifying regions and materials

The region is specified by a REGION statement. REGION specifies the location of materials in a previously defined mesh. A region is a volume that has a uniform material composition. In the REGION statement, the material composition is specified by the MATERIAL

parameter. Can also use the X.MIN, X.MAX, Y.MIN, Y.MAX, Z.MIN, and Z.MAX parameters to specify the location, extent of the region and its geometry, in microns [1].

X.MAX: Specifies the X coordinate to specify the maximum X-value.

X.MIN: Specifies the X coordinate to specify the minimum X-value.

Y.MAX: Specifies the Y coordinate to specify the maximum Y-value.

Y.MIN: Specifies the Y coordinate to specify the minimum Y-value.

Z.MAX: Specifies the Z coordinate to specify the maximum Z-value.

Z.MIN: Specifies the Z coordinate to specify the minimum Z-value.

Once the mesh is specified, every part of it must be assigned a material type. This is done with REGION statements as follows [1]:

REGION NUM=<integer> MATERIAL=<material_type> <position parameters>

In the case of a new material not recognized by Atlas, we replace the MATERIAL parameter with the USER.MATERIAL parameter in REGION statements [1].

In this case, the REGION statements is written as follows:

REGION NUM=<integer> USER.MATERIAL=<material_type> <position parameters>
.   .   .   .
.   .   .   .
.   .   .   .
For example, a two-dimensional structure consisting of three regions (Figure II.3) can be defined as follows:

REGION NUM=1 USER.MATERIAL=a-ITZO   X.MIN=0   X.MAX=25   Y.MIN=0   Y.MAX=0.005

REGION NUM=2 MATERIAL=SiO2 X.MIN=0   X.MAX=25   Y.MIN=0.005   Y.MAX=0.0075

REGION NUM=3 MATERIAL=HfO2 X.MIN=0   X.MAX=25   Y.MIN=0.0075   Y.MAX=0.075
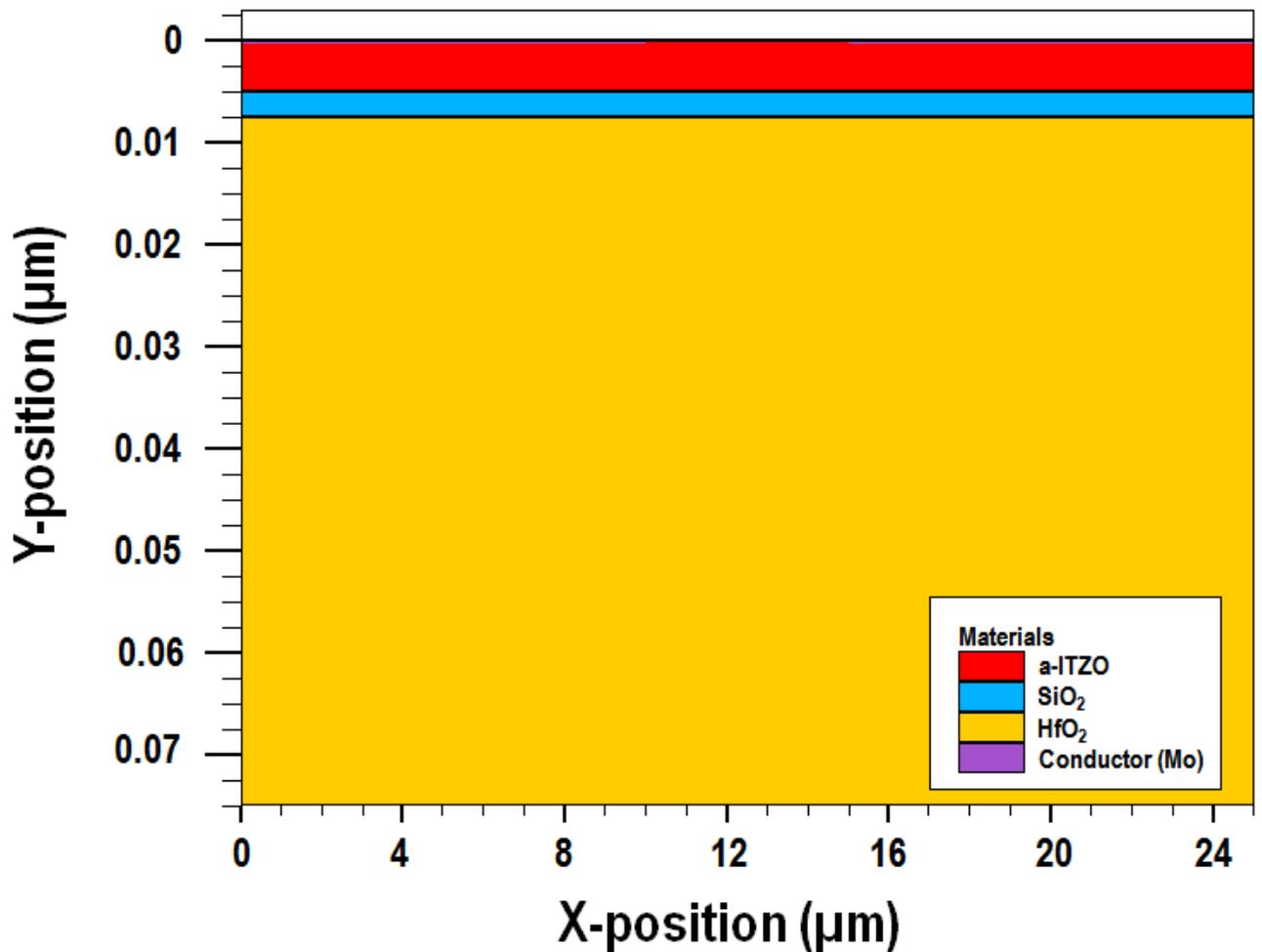
Figure II.3: Schematic diagram of a structure consisting of three regions generated by Silvaco

Atlas.

II.6.1.3 Electrode

II.6.1.3.1 ELECTRODE definition

Device electrodes are specified using the ELECTRODE statement. ELECTRODE specifies the locations and names of electrodes in a previously defined mesh. ELECTRODE should be an n-digit integer, where each of the digits is a separate electrode number [1].

II.6.1.3.2 Specifying electrodes

Once we have specified the regions and materials, we define at least one electrode. This is done with the ELECTRODE statement. Can specify up to 100 electrodes in both 2D and 3D Atlas. The position parameters are specified in microns using the X.MIN, X.MAX, Y.MIN, and

Y.MAX parameters. Also can use the RIGHT, LEFT, TOP, and BOTTOM parameters in

ELECTRODE statement to define the location [1].

Example:

ELECTRODE   NUM=<n>   [NUMBER=<n>]   NAME=<en>   [NAME=<electrode   name>]

[SUBSTRATE] <pos>[<position_parameters>] <reg>

    In this case, the electrodes shows in Figure II.4 can be defined as follows:

ELECTRODE NUM=1 NAME=Gate BOTTOM Y.MAX =0.0 X.MIN=0.0 X.MAX=25

ELECTRODE NUM=2 NAME=Source Y.MAX=0.0 X.MIN=0.0 X.MAX=10.0

ELECTRODE NUM=3 NAME=Drain Y.MAX =0.0 X.MIN=15.0 X.MAX=25.0
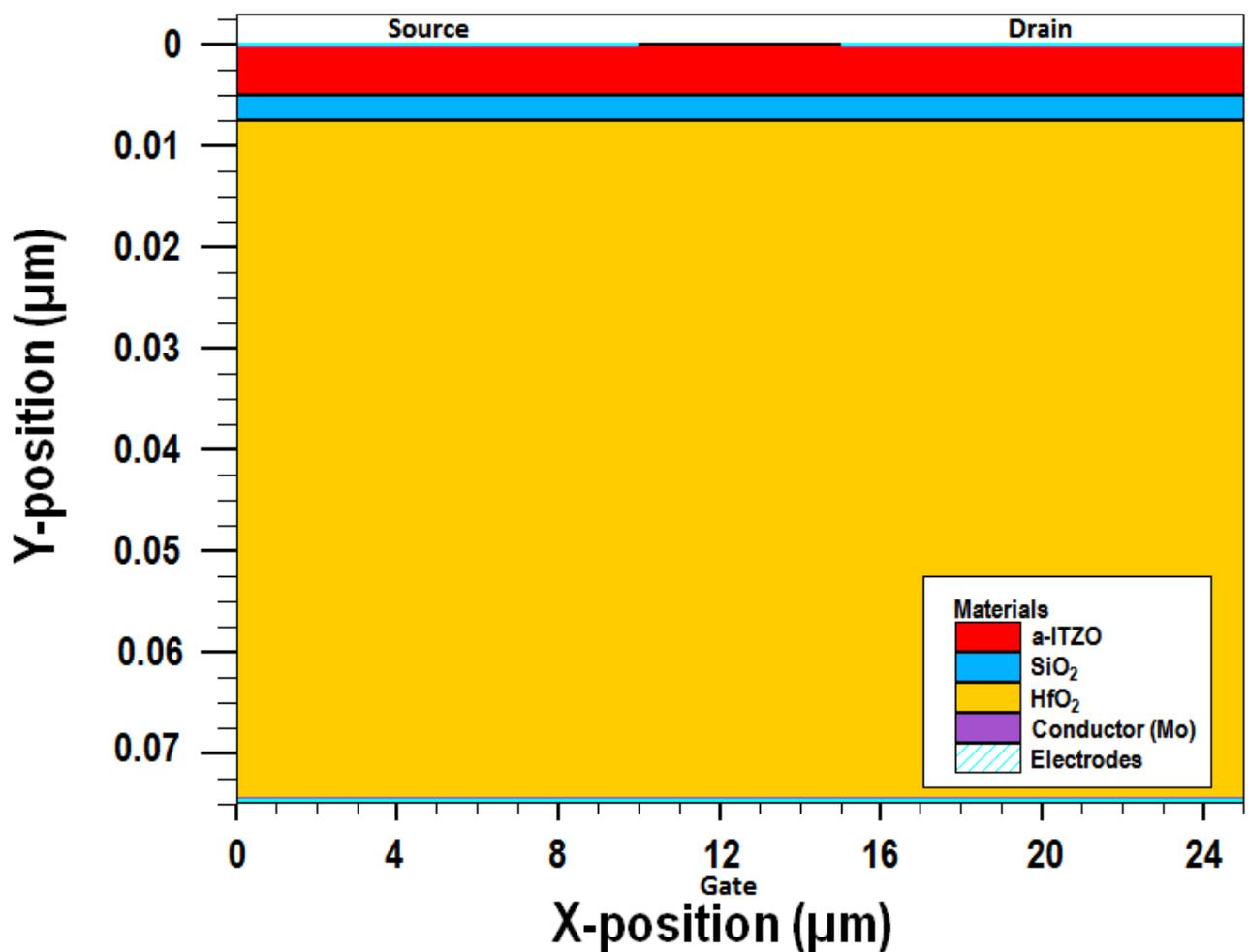
Figure II.4: Schematic diagram of a structure consisting of three regions with the source, drain

and gate electrodes generated by Silvaco Atlas.

II.6.1.4 Doping

The DOPING statement is used to define doping profiles in the device structure. Typically a sequence of DOPING statements is given each building on the others [1].

For example:

DOPING <distribution_type> <dopant_type> <position_parameters>

The statement is DOPING. All other items are parameters of the DOPING statement. UNIFORM and N.TYPE are logical parameters. CONCENTRATION is a real parameter and takes floating point numbers as input values. REGION is an integer parameter taking only integer numbers as input [1].

We defined one of the doping cases of the active layer of a-ITZO TFT we used in simulators as follows:

DOPING UNIFORM N.TYPE CONCENTRATION=4.62E15 REGION=1

The position parameters X.MIN, X.MAX, Y.MIN, and Y.MAX can be used instead of a region number.

II.6.2 Material models specification

This group includes four main statements:

- Material

- Models

- Contact

- Interface

II.6.2.1 Material

We can use the MATERIAL statement to specify the material properties of the defined regions as follows [1]:

MATERIAL <localization> <material_definition>

But we must complete the entire mesh and doping definition before any MATERIAL statements can be used [1].

II.6.2.1.1 Specifying material properties

The MATERIAL statement is used for set basic material parameters. All materials are split into three classes: semiconductors, insulators, and conductors [1]. Each class requires a different set of parameters to be specified:

For semiconductors, these parameters include the following:

EG300: Specifies the value of bandgap of the material at 300K.

AFFINITY: Specifies the electron affinity of the material.

MUN: Specifies low-field electron mobility.

MUP: Specifies low-field hole mobility. This parameter is only used if no concentration-dependent mobility model is specified.

The MUN and MUP parameters are only used if no concentration-dependent mobility model is specified.

PERMITTIVITY: Specifies relative dielectric permittivity of the material. All materials in an Atlas structure must have a defined permittivity.

NC300: Specifies the conduction band density at 300K.

NV300: Specifies valence band density at 300K.

TAUN0: Specifies SRH lifetime for electrons.

TAUP0: Specifies SRH lifetime for holes.

SOPRA: Identifies the name of a file from the SOPRA database.

II.6.2.1.2 Specifying unknown or defined materials in Atlas

As mentioned previously, all materials in Atlas are classified as a semiconductor, an insulator, or a conductor. These classes are termed user groups. In order to correctly define a new material in Atlas, we must specify [1]:

- The name of the new material (not recognized by Atlas) that was previously specified in the REGION statement using the USER.MATERIAL parameter.

- The user group it belongs to.

- The known Atlas material it is to take as a default material.

Once we set these three elements up in their appropriate places in the input deck, we can change the specific properties of them using MATERIAL statements.

A user group takes for semiconductors the following definitions:

MATERIAL MATERIAL=<>   USER.GROUP=<>   USER.DEFAULT=<> EG300=<> AFFINITY=<>

MUN=<>   MUP=<>   PERMITTIVITY=<>   NC300=<>   NV300=<>   TAUN0=<>   TAUP0

INDEX.FILE=<>

Here in this case [1]:

MATERIAL: specifies the name of the new material that was previously specified in the REGION statement using the USER.MATERIAL parameter.

USER.MATERIAL: Specifies a user-defined material name. The specified material name can be any name except that of a default material, such as a-ITZO. We should define each material with an accompanying definition in the MATERIAL statement. We can define up to 50 user-defined materials. For example, USER.MATERIAL =<material_name>.

USER.GROUP: Specifies the material group for the user-defined material. USER.GROUP can be either SEMICONDUCTOR, INSULATOR, or CONDUCTOR. For example, USER.GROUP =<material_group>.

USER.DEFAULT: Specifies which material the user-defined material should use for its default parameters. For example, USER.DEFAULT = <known_atlas_material_name>.

As an example of the syntax required to define a new material, we will define a new material called a-ITZO. For simplicity, we will omit all the other code for the complete Atlas deck and only include code for deck structure purposes.

GO ATLAS

MESH

.

.

.

REGION NUM=1 USER.MATERIAL =a-ITZOY.MIN =0   Y.MAX=0.005

ELECTRODE ...

DOPING ...

MATERIAL MATERIAL=a-ITZO USER.GROUP=semiconductor USER.DEFAULT=igzo

EG300=3.02 AFFINITY=4.65 MUN=30 MUN=0.1 NC300=1.59e19 NV300=1.21e21

INDEX.FILE=ITZO.nk

.

.

.

II.6.2.2 Models

MODELS specifies model flags to indicate the inclusion of various physical mechanisms, models, and other parameters for the simulation.

II.6.2.2.1 Defining material parameters and models

Atlas provides a comprehensive set of physical models. Once we define the mesh, geometry, and doping profiles, modifying the characteristics of electrodes, change the default material parameters, we can choose which physical models Atlas will use during the device simulation. The physical models can be grouped into five classes: mobility, recombination, carrier statistics, impact ionization, and tunneling. All models with the exception of impact ionization are specified on the MODELS statement. Impact ionization is specified on the

IMPACT statement. To choose these physical models, we use the MODELS statement. the density of states models can be enabled using the DEFECTS statement [1]. Interface properties are set by using the INTERFACE statement.

II.6.2.2.2 Models of the density of state (DOS) used in the simulation

Silvaco Atlas its can simulates the disordered material systems and the structure of TFT devices based on these material systems [13]. We can also by Atlas define an energy distribution of defect states in the band gap of semiconductor materials and used in the simulation [14]. This is necessary for the accurate treatment of the electrical properties of such materials as a-ITZO.

Disordered materials contain a large number of defect states within the band gap of the material. To accurately model devices made of amorphous materials, use a continuous density of states as a combination of exponentially decaying band tail states and Gaussian distributions of mid-gap states [15-17].

The models of the density of states (DOSs) of the a-IGZO and a-ITZO used in the simulation are shown in Figure II.5, while the input parameters of DOS models are summarized in Table II.2.
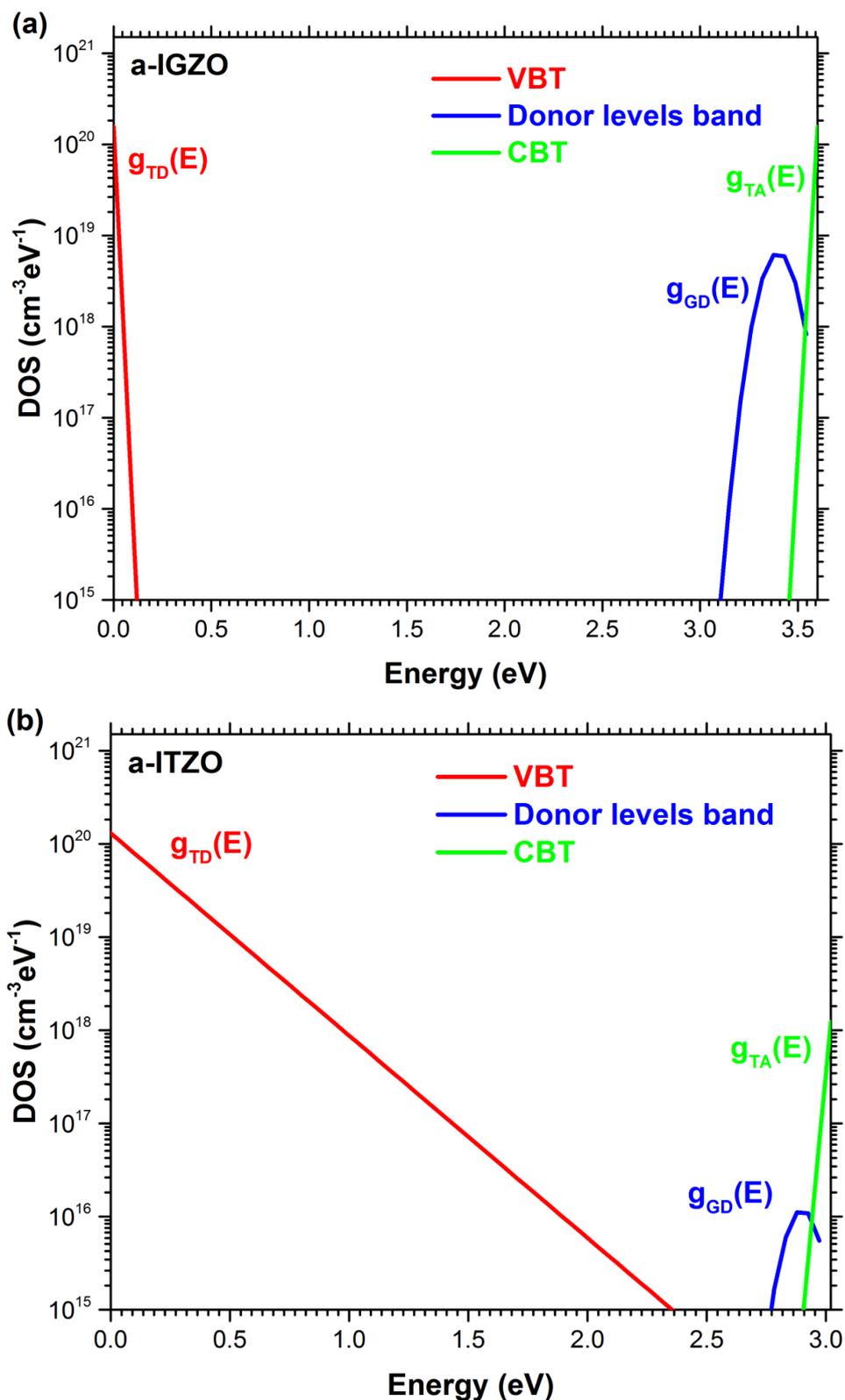
Figure II.5: Schematic of DOS models used in the simulation of the total subgap energy range of (a) a-IGZO and (b) a-ITZO [10, 14].

Trough Figure II.5 it is assumed that the subgap DOS (g(E)) for both the a-IGZO and a-ITZO is composed of three bands : acceptor-like exponentially conduction band tail (CBT) states (g$_{TA}$(E)), donor-like exponentially valence band tail (VBT) states (g$_{TD}$(E)) and donor-like Gaussian shallow levels band states (g$_{GD}$(E)) [14-18]. This DOS can be modeled as [14, 19-22]:

$$g(E) = g_{TA}(E) + g_{TD}(E) + g_{GD}(E) \tag{II.17}$$

The acceptor-like exponentially CBT states density is given by [23, 24]:

$$g_{TA}(E) = N_{TA}exp\left[\frac{E-E_C}{W_{TA}}\right] \tag{II.18}$$

where E is the trap energy, E_C is the conduction band energy, N_{TA} is the effective density at E_C and W_{TA} is the characteristic slope energy of the conduction band tail states while the subscripts (T and A) are stand for tail and acceptor states, respectively.

The donor-like exponentially VBT states density is also given by a similar expression [1, 25]:

$$g_{TD}(E) = N_{TD}exp\left[\frac{E_V-E}{W_{TD}}\right] \tag{II.19}$$

where E is the trap energy, E_V is the valence band energy, N_{TD} is the effective density at E_V and W_{TD} is the characteristic slope energy of the valence band tail states while the subscripts (T and D) are stand for tail and donor states, respectively.

The donor-like Gaussian levels band states density is given by [26]:

$$g_{GD}(E) = N_{GD}exp\left[-\left[\frac{E-E_{GD}}{W_{GD}}\right]^2\right] \tag{II.20}$$

where E is the trap energy, N_{GD} is the maximum density of donor-like states in Gaussian distribution, E_{GD} is the peak energy of donor-like Gaussian distribution and W_{GD} is the characteristic decay energy for Gaussian distribution of donor-like states while the subscripts (G and D) are a stand for Gaussian and donor states, respectively.

Region	Parameter	Description	Value	Ref
a-IGZO (n-type channel)	N_{TA}/N_{TD} $(\times 10^{20}\ cm^{-3}eV^{-1})$	The density of acceptor-like states at E_c and donor-like states at E_V, respectively	1.55/1.55	[14]
	W_{TA}/W_{TD} $(\times 10^{-2}\ eV)$	The characteristic decay energy of the CBT and VBT, respectively	1.3/1.2	[14]
	N_{GD} $(cm^{-3}eV^{-1})$	The maximum density of the shallow donor-like Gaussian states	6.5×10^{18}	[27]
	W_{GD} (eV)	The characteristic deviation of the shallow donor-like Gaussian states	0.1	[14]
	E_{GD} (eV)	The energy that corresponds to the maximum density of the shallow donor-like Gaussian states	2.9	[14]
	SIGTAE/SIGTAH $(\times 10^{-15}\ cm^2)$	Capture cross-section for electrons/holes in CBT	1/1	[14]
	SIGTDE/SIGTDH $(\times 10^{-15}\ cm^2)$	Capture cross-section for electrons/holes in VBT	1/1	[14]
	SIGGDE/SIGGDH $(\times 10^{-15}\ cm^2)$	Capture cross-section for electrons in the shallow donor-like Gaussian states	1/1	[14]
a-ITZO (n-type channel)	N_{TA}/N_{TD} $(\times 10^{20}\ cm^{-3}eV^{-1})$	The density of acceptor-like states at E_c and donor-like states at E_V, respectively	122/1.30	[28]
	W_{TA}/W_{TD} $(\times 10^{-2}\ eV)$	The characteristic decay energy of the CBT and VBT, respectively	1.6/2.0	[28]
	N_{GD} $(cm^{-3}eV^{-1})$	The maximum density of the shallow donor-like Gaussian states	1.19×10^{16}	[28]
	W_{GD} (eV)	The characteristic deviation of the shallow donor-like Gaussian states	8.3×10^{-2}	[28]
	E_{GD} (eV)	The energy that corresponds to the maximum density of the shallow donor-like Gaussian states	2.9	[28]
	SIGTAE/SIGTAH $(\times 10^{-16}\ cm^2)$	Capture cross-section for electrons/holes in CBT	1/100	[29]
	SIGTDE/SIGTDH $(\times 10^{-16}\ cm^2)$	Capture cross-section for electrons/holes in VBT	100/1	[29]
	SIGGDE/SIGGDH $(\times 10^{-16}\ cm^2)$	Capture cross-section for electrons in the shallow donor-like Gaussian states	100/1	[29]

Table II.2 The input parameters of the DOS models for both the a-IGZO and a-ITZO.

The DEFECT statement is used to specify the density of defect states (DOS) as a combination of exponentially decaying band tail states and Gaussian distributions of mid-gap states [1].

The density of state models shown in Figure II.5 are defined by using the DEFECTS statement in the MODELS as follows:

For a-IGZO:

MODELS Fermi

DEFECTS NTA=1.55e20 NTD=1.55e20 WTA=0.013 WTD=0.12 \

NGA=0.0 NGD=6.5e18 EGD=2.9 WGD=0.1 \

SIGTAE=1e-15 SIGTAH=1e-15 SIGTDE=1e-14 SIGTDH=1e-16 \

SIGGAE=1e-15 SIGGAH=1e-15 SIGGDE=1e-15 SIGGDH=1e-15 \

dfile=tft_don.dat afile=tft_acc.dat

For a-ITZO:

MODELS Fermi

DEFECTS NTA=1.22e18 NTD=1.30e20 WTA=0.016 WTD=0.20 \

NGA=0.0 NGD=1.19e16 EGD=2.87 WGD=0.083 \

SIGTAE=1e-16 SIGTAH=1e-14 SIGTDE=1e-14 SIGTDH=1e-16 \

SIGGAE=1e-16 SIGGAH=1e-14 SIGGDE=1e-14 SIGGDH=1e-16 \

dfile=tft_don.dat afile=tft_acc.dat

FERMI: Specifies that Fermi-Dirac carrier statistics be used.

The resultant distribution of defects versus energy can be plotted in the files, don.dat and acc.dat.

II.6.2.3 Contact

CONTACT specifies the physical attributes of an electrode. If the CONTACT statement is not used for a given electrode an electrode in contact with semiconductor material is assumed by default to be ohmic. We can assign the WORKFUNCTION parameter on the CONTACT statement. If a work function is defined, the electrode is treated as a Schottky contact. The CONTACT statement is used to specify the metal work function of one or more electrodes. The

NAME parameter is used to identify which electrode will have its properties modified. The NUMBER parameter is used to identify a contact number for which electric field lines are calculated [1].

The syntax is as follows:

CONTACT NUMBER=<n> NAME=<ename> WORKFUNCTION=<n>

For example, the contacts for molybdenum are defined as follows:

CONTACT NUMBER=1 NAME=gate WORKFUNCTION=4.53

CONTACT NUMBER=1 NAME=source WORKFUNCTION=4.53

CONTACT NUMBER=1 NAME=drain WORKFUNCTION=4.53

II.6.2.4 Interface

The INTERFACE statement consists of a set of boundary condition parameters for the interface and a set of parameter to localize the effect of these parameters. INTERFACE specifies interface parameters at semiconductor/insulator boundaries. The INTERFACE statement is used to define the interface charge density and surface recombination velocity at interfaces between semiconductors and insulators [1].

Syntax

INTERFACE [<params>]

In many cases, the interface of interest is restricted to a specific region. This can be accomplished with the X.MIN, X.MAX, Y.MIN, and Y.MAX parameters on the INTERFACE statement. These parameters define a rectangle, where the interface properties apply, restricts the interface charge to the semiconductor-insulator boundary within the specified rectangle. In addition to fixed charge, surface recombination velocity and thermionic emission are enabled and defined with the INTERFACE statement [1].

By default, the INTERFACE statement is applied to semiconductor-insulator interfaces. Interface charge can, however, be added at the interfaces between two semiconductor regions

or at the edges of semiconductor regions. The CHARGE parameter defines the interface charge value in cm^{-2}. The S.I, S.S, and S.X parameters control whether the charge is placed between semiconductor-insulator regions, semiconductor-semiconductor regions or at the semiconductor domain edges. We can control the location of the added charge by using the position parameters [1].

INTTRAP activates interface defect traps at discrete energy levels within the bandgap of the semiconductor and sets their parameter values [1].

Syntax

INTTRAP <type> E.LEVEL=<r> DENSITY=<r> <capture parameters>

For example:

INTTRAP DONOR E.LEVEL=2.9 DENSITY=5.e10 DEGEN=1 \

SIGN=1.00e-16 SIGP=1.00e-14

INTTRAP ACCEPTOR E.LEVEL=0.4 DENSITY=1.e10 DEGEN=12 \

SIGN=1.00e-14 SIGP=1.00e-16

Where:

DEGEN: Specifies the degeneracy factor of the trap center.

DONOR: Specifies a donor-type trap level.

ACCEPTOR: Specifies an acceptor-type trap level.

ACCEPTOR: Specifies a uniform density of ionized acceptors in the quantum wells.

E.LEVEL: Sets the energy of the discrete trap level. For acceptors, E.LEVEL is relative to the conduction band edge. For donors, it depends on the valence band edge.

DENSITY: Sets the maximum density of states of the trap level.

SIGN: Specifies the capture cross-section of the trap for electrons.

SIGP: Specifies the capture cross-section of the trap for holes.

The I.C, I.I, I.M, S.C, S.I, S.M, and S.S parameters can be written in an INTTRAP statement for Insulator-Conductor, Insulator-Insulator, Insulator-Metal, semiconductor-Conductor, semiconductor-insulator, semiconductor-Metal, and semiconductor- semiconductor interface states, respectively [1].

We can control the location of the added traps by using the position parameters (the X.MIN, X.MAX, Y.MIN, and Y.MAX parameters).

II.6.3 Numerical method selection

This group includes main one statement which is METHOD.

II.6.3.1 Method

METHOD sets the numerical methods to be used to solve the equations and parameters associated with algorithms. The METHOD statement is used to set the numerical methods for subsequent solutions. All structure and model definitions should precede the METHOD statement and all biasing conditions should follow it. Parameters in the METHOD statement are used to set the solution technique, specify options for each technique and tolerances for convergence. Several different numerical methods can be used for calculating the solutions to semiconductor device problems. Numerical methods are given in the METHOD statements of the input file [1].

Different combinations of models will require ATLAS to solve up to six equations. For each of the model types, there are basically three types of solution techniques: (a) decoupled (GUMMEL), (b) fully coupled (NEWTON) and (c) BLOCK. The GUMMEL method will solve for each unknown, in turn, keeping the other variables constant, repeating the process until a stable solution is achieved. The NEWTON method solves the total system of unknowns together. The BLOCK methods will solve some equations fully coupled while others are de-coupled [1].

Generally, the GUMMEL method is useful where the system of equations is weakly coupled but has only linear convergence. The NEWTON method is useful when the system of equations is strongly coupled and has quadratic convergence. The NEWTON method may, however, spend extra time solving for quantities, which are essentially constant or weakly coupled. NEWTON also requires a more accurate initial guess to the problem to obtain convergence. Thus, a BLOCK method can provide for faster simulations times in these cases over NEWTON. GUMMEL can often provide better initial guesses to problems. It can be useful to start a solution with a few GUMMEL iterations to generate a better guess [1].

Then, switch to NEWTON to complete the solution. Specification of the solution method is carried out as follows [1]:

METHOD GUMMEL BLOCK NEWTON

The exact meaning of the statement depends on the particular models it applied to [1].

II.6.4 Solution specification

This group also includes four main statements:

- LOG

- SOLVE

- LOAD

- SAVE

II.6.4.1 Log

LOG specifies the filename for the circuit voltages and currents that will be saved [86]. LOG allows all terminal characteristics of a run to be saved to a file. Any DC, transient, or AC data generated by SOLVE statements after the LOG statement is saved [1].

Syntax

LOG [OUTFILE=<filename>]

For example:

LOG OUTF=myfile.log

This example saves all I-V data in a file, myfile.log.

The contents of LOG files varies for different types of simulations (e.g., DC, transient, AC). The content is set by the first SOLVE statement after the LOG statement [1].

Correct transient parameters would have not been stored if the LOG statement had been placed before the first SOLVE statement, which is DC [1].

The LOG statements are used to save the Id/Vds curve from each gate voltage to separate files. We recommend that we save the data in this manner rather than to a single LOG file [1].

Log files store the terminal characteristics calculated by ATLAS. These are current and voltages for each electrode in DC simulations. In transient simulations, the time is stored. In AC simulations, the small signal frequency and the conductances and capacitances are saved [1].

II.6.4.2 Solve

SOLVE instructs Atlas to perform a solution for one or more specified bias points [1]. We can syntax as follows:

SOLVE VGATE=0.0 VSTEP=-0.1 VFINAL=-5.0 NAME=gate

SOLVE VGATE=0.1 VFINAL=5.0 NAME=gate

This example is very useful during bias ramps in overcoming convergence difficulties around transition points such as the threshold voltage [1].

Each SOLVE statement must specify an initial bias condition. Once any DC condition has been solved, either a transient or AC analysis may be performed. We may also solve for carrier generation due to incident light under DC, or AC analysis transient conditions [1].

One important rule in Atlas is that when the voltage on an electrode is not specified in a given SOLVE statement, the value from the last SOLVE statement is assumed [1].

When the voltage on a particular electrode is never defined on any SOLVE statement and voltage is zero, we don't need to explicitly state the voltage on all electrodes on all SOLVE statements [1].

Atlas also supports the reverse case through current boundary conditions. The current through the electrode is specified in the SOLVE statement and the voltage at the contact is calculated. Current boundary conditions are set using the CONTACT statement. The syntax of the SOLVE statement is altered once current boundary conditions are specified [1].

II.6.4.3 Load

LOAD loads previous solutions from files as initial guesses to other bias points. The LOAD statement requires that one of the following file parameter syntax be used [1].

LOAD INFILE=<filename>

INFILE name of a file (file name) to be loaded as an initial guess for further simulation.

II.6.4.4 Save

SAVE saves all node point information into an output file, simulation results into files for visualization or for future use as an initial guess [1].

Syntax

SAVE OUTFILE=<filename>.

Example

SAVE OUTFILE=my_filename.str

OUTFILE: Specifies that after the simulation is finished the solution is to be written to a file called my_filename.str. In other words, only one structure file will output after the simulation has finished. Even if we have several [1].

II.6.5 Results analysis

This group includes two main statements:

II.6.5.1 Extract

Atlas does not support arithmetic expressions in the syntax. We can, however, evaluate and use expressions by using the EXTRACT statements. EXTRACT statements are used to measure parameters from both log and solution files. It allows we to extract device parameters. The command has a flexible syntax that allows we to construct specific EXTRACT routines. EXTRACT operates on the previous solved curve or structure file. By default, EXTRACT uses the currently open log file [1].

A typical example of using EXTRACT is the extraction of the threshold voltage of an transistor. In the following example, the threshold voltage is extracted by calculating the maximum slope of the Id/ Vg curve, finding the intercept withthe X axis and then subtracting half of the applied drain bias [1].

EXTRACT   NAME="nvt"   XINTERCEPT(MAXSLOPE(CURVE   (V."GATE",   (I."DRAIN")))   \-
(AVE(V."DRAIN"))/2.0)

To extract peak drain current from a run immediately after solution, type:

LOG OUTF=myfile.log

SOLVE ...

EXTRACT NAME="peak Id" max(i."drain")

Extractions can only be done after completion of the simulation. Therefore, EXTRACT should be specified after re-initialization of Atlas (go atlas) [1].

The results of the extraction will be displayed in the run-time output and will be by default stored in the file results [1].

II.6.5.2 Tonyplot

TONYPLOT starts the graphical post-processor TonyPlot. All graphics in Atlas is performed by saving a file and loading the file into TonyPlot. The TONYPLOT command causes Atlas to automatically save a structure file and plot it in TonyPlot. The TonyPlot window will

appear displaying the material boundaries. Use the Plot: Display menu to see more graphics options [1].

tonyplot -overlay tft_1a.log tft_1b.log tft_1.dat -set tft_1.set

tonyplot -overlay tft_don.dat -set tft_don.set

tonyplot -overlay tft_acc.dat -set tft_acc.set

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Chapter

3

Results and discussions

III.1 Introduction

Although several AOS materials based on zinc oxide can be used as active layers for TFT, there is growing interest in a-ITZO because it is considered as promising material for the channel of TFT in the high-performance electronic devices for the next generation because it has many good features [1]. It can accomplish a mobility higher than amorphous indium-gallium-zinc-oxide (a-IGZO) that is considered the most prominent of these materials, a high transparency to visible light, a lower cost than a-IGZO and large-area uniformity at the low-temperature process as well as the use of the plastic substrate [2-5].

In order to significantly improve the performance of the TFT devices, researchers sought to reduce the physical thickness of the gate dielectric. But the problem is that the physical thickness of the gate dielectric has been significantly reduced to a certain extent where the reliability of the TFT devices is severely affected, due to increased leakage current [6-8].

In this chapter, we will simulate the a-IGZO TFT and a-ITZO TFT devices and we will compare the performance of both devices. Then we will focus on the performance and reliability of a-ITZO TFTs by simulating the effect of high-k gate dielectrics, the physical thickness of the gate dielectric, the effective thickness (equivalent oxide thickness) of the gate dielectric, the bi-layer dielectrics, the mono-layer dielectrics, and the interfacial dielectrics on the performance of the a-ITZO TFT and its reliability, in addition, we studied the effect of the defects of the semiconductor-dielectric and dielectric-dielectric interfaces as well as the oxide on the performance a-ITZO TFT.

III.2 a-IGZO TFT VS a-ITZO TFT performance

Two-dimensional cross-section of the a-IGZO and a-ITZO TFTs structure used with regions, materials, and dimensions is shown in Figure III.1, while the input parameters of transistors structure are summarized in Table III.1.

Region	Parameter	Description	Value	Ref
a-IGZO (n-type channel)	$L(\mu m)/W(\mu m)/T(nm)$	Length/Width/Thickness	25/10/5	[9]
	$N_d(cm^{-3})$	n doping concentration	4.62×10^{15}	[9]
	$E_g(eV)$	Band gap	3.2	[10]
	$\chi(eV)$	Electronic affinity	4.60	[11]
	$\mu_n/\mu_p \ (cm^2 V^{-1} s^{-1})$	Low-field electron/hole mobility	15/0.1	[12]
	$N_C/N_V \ (\times 10^{19} \ cm^{-3})$	Conduction/valence band density at $300K$	5/5	[12]
	$\sigma_{TAE}/\sigma_{TAH} \ (\times 10^{-15} \ cm^2)$	Capture cross-section for electrons/holes in CBT	1/1	[10]
	$\sigma_{TDE}/\sigma_{TDH} \ (\times 10^{-15} \ cm^2)$	Capture cross-section for electrons/holes in VBT	1/1	[10]
	$\sigma_{GDE}/\sigma_{GDH} \ (\times 10^{-15} \ cm^2)$	Capture cross-section for electrons in the shallow donor-like Gaussian states	1/1	[10]
a-ITZO (n-type channel)	$L(\mu m)/W(\mu m)/T(nm)$	Length/Width/Thickness	25/10/5	[9]
	$N_d(cm^{-3})$	n doping concentration	4.62×10^{15}	[9]
	$E_g(eV)$	Band gap	3.02	[9]
	$\chi(eV)$	Electronic affinity	4.65	[13]
	$\mu_n/\mu_p \ (cm^2 V^{-1} s^{-1})$	Low-field electron/hole mobility	30/0.1	[9]
	$N_C/N_V \ (\times 10^{19} \ cm^{-3})$	Conduction/valence band density at $300K$	1.59/121	[9]
	$\sigma_{TAE}/\sigma_{TAH} \ (\times 10^{-16} \ cm^2)$	Capture cross-section for electrons/holes in CBT	1/100	[14]
	$\sigma_{TDE}/\sigma_{TDH} \ (\times 10^{-16} \ cm^2)$	Capture cross-section for electrons/holes in VBT	100/1	[14]
	$\sigma_{GDE}/\sigma_{GDH} \ (\times 10^{-16} \ cm^2)$	Capture cross-section for electrons in the shallow donor-like Gaussian states	100/1	[14]
SiO$_2$	$L(\mu m)/W(\mu m)/T(nm)$	Length/Width/Thickness	25/10/70	[9]
	$E_g(eV)$	Band gap	9	[9]
	k_{SiO_2}	The relative permittivity	3.9	[9]
Mo source and drain contacts	$L(\mu m)/W(\mu m)/T(nm)$	Length/Width/Thickness	10/10/0.1	[9]
	$L_{SD}(\mu m)$	The source-drain spacing	5	[9]
	$\Phi_{Mo}(eV)$	The work function of Mo	4.53	[15]
Mo gate electrode contact	$L(\mu m)/W(\mu m)/T(nm)$	Length/Width/Thickness	25/10/0.1	[9]
	$L_{OV}(\mu m)$	The gate-to-S/D overlap length	10	[9]
	$\Phi_{Mo}(eV)$	The work function of Mo	4.53	[15]

Table III.1 The input parameters of the a-IGZO and a-ITZO TFT devices.
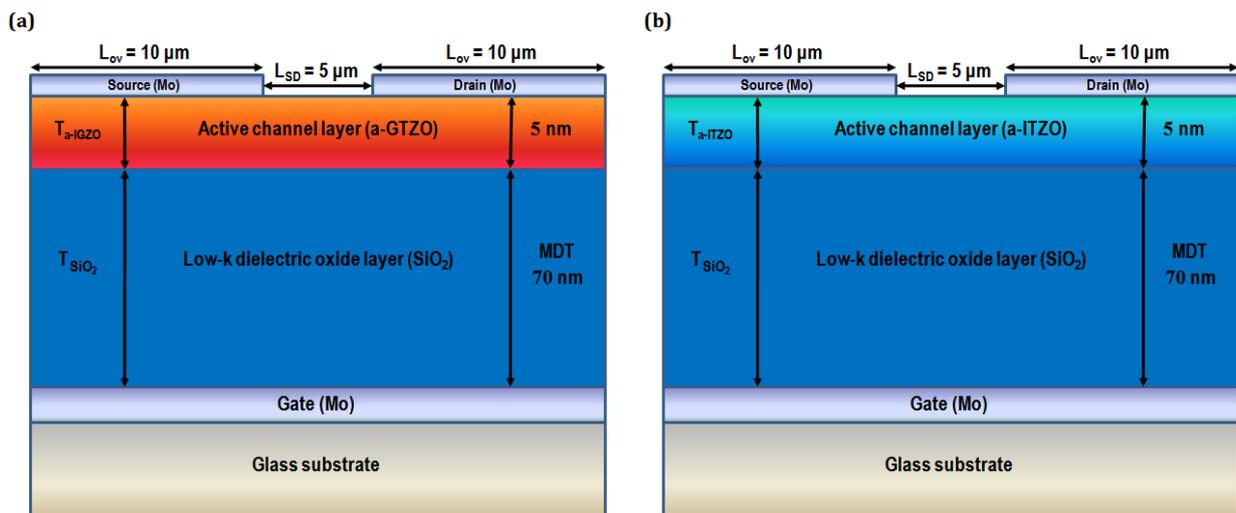
Figure III.1 Schematic diagram of a two-dimensional cross-section of the bottom-gate TFTs structure, dimensions, regions, and materials depending on the types of channel material: (a) a-IGZO and (b) a-ITZO.

The evolution of the transfer characteristics of the a-IGZO and a-ITZO TFTs in the linear and semi-logarithmic plots is shown in Figure III.2.
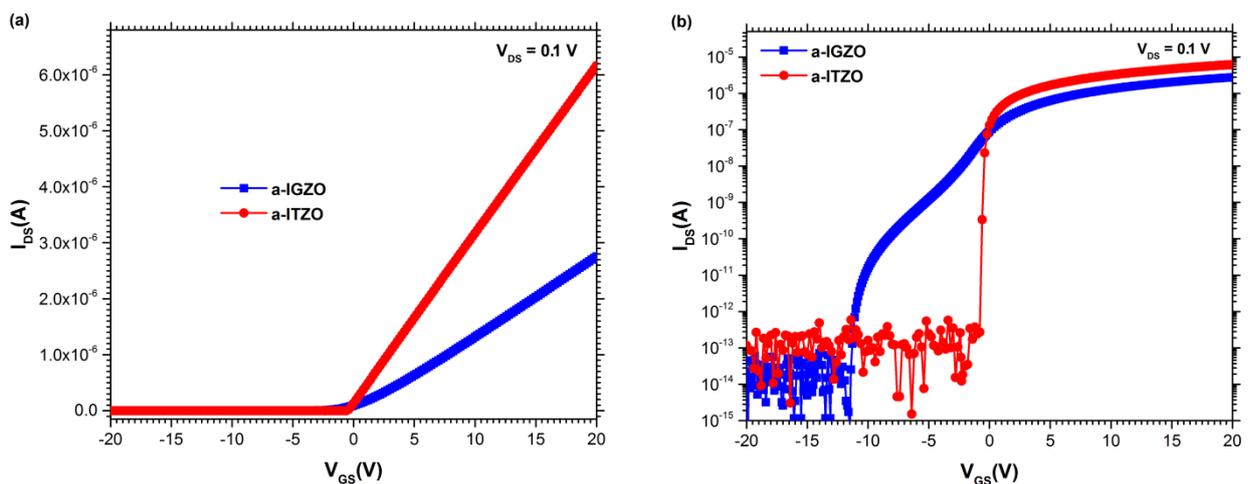
Figure III.2 The calculated of transfer $(I_{DS} - V_{GS})$ characteristics of the a-IGZO and a-ITZO TFTs where (a) shows the evolution of the transfer characteristics in the linear plot while (b) shows the evolution of the transfer characteristics in the semi-logarithmic plot.

Through these results shown in Figure III.2, we note that replacing a-IGZO by a-ITZO in TFT improves transistor properties through raising the current (the drain current) of TFT as well as cancel the hump that appears in the transfer characteristic curve of TFT caused by the predominance of defects in the semiconductor bulk and the semiconductor-dielectric interface.

From the transfer characteristic curves in the linear plot (Figure III.2.a) we calculated the threshold voltage (V_T) and the field-effect mobility (μ_{FE}), while we calculated I_{on}, I_{on}/I_{off} ratio, subthreshold swing (SS), and turn-on voltage (V_{on}) using the transfer characteristic curves in the semi-logarithmic plot (Figure III.2.b). All the obtained results for the previous parameters (Output parameters) of TFT devices as well as the capacitance per unit area (C_i) that was calculated using Equation I.16, are shown in Table III.2.

Case	$C_i(F/cm^2)$	$V_T(V)$	$SS(V/decade)$	$\mu_{FE}(cm^2V^{-1}s^{-1})$	$I_{on}(A)$	I_{on}/I_{off}	$V_{on}(V)$
a-IGZO	4.93×10^{-8}	0.56	7.63×10^{-2}	14.86	2.76×10^{-6}	3.36×10^{7}	-1.01
a-ITZO	4.93×10^{-8}	-0.50	6.80×10^{-2}	29.96	6.15×10^{-6}	6.97×10^{7}	-0.80

Table III.2 The variations of the extracted parameters: V_T, SS, μ_{FE}, I_{on}, I_{on}/I_{off} and V_{on} as well as C_i depending on the types of channel material.

The results show a-ITZO TFT superiority on a-IGZO TFT, where it has higher performance with significantly higher mobility than the a-IGZO TFT for the same value of the gate capacitance per unit area.

Figure III.3 represents the evolution of output ($I_{DS} - V_{DS}$) characteristics, which was used in the calculation of the electrical resistivity for the active layers of the TFTs (a-IGZO and a-ITZO layers) in different gate tensions (V_{GS}) where these evolutions also show that a-ITZO TFT is superior in performance by raising current.
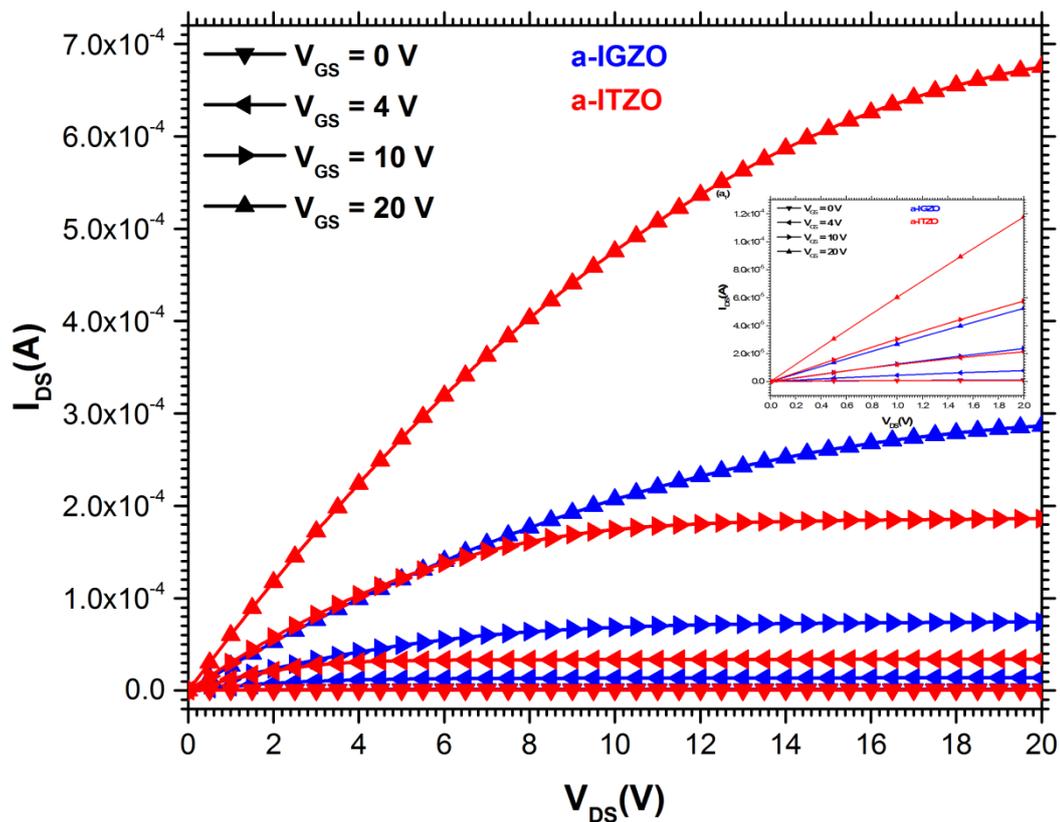
Figure III.3 The evolution of output ($I_{DS} - V_{DS}$) characteristics of the a-IGZO and a-ITZO TFTs.

From the output characteristic curves, especially in the linear region, we calculated the electrical resistivity values of the active layers of the a-IGZO and a-ITZO TFT devices that have been obtained from the drain current-drain voltage ($I_{DS} - V_{DS}$) measurements at a different gate tensions (V_{GS}) using Equation I.14 for an input voltage $\approx 0\ V$ (Linear region) [16, 17], results are listed in Table III.3.

$V_{GS}(V)$	$0\ V$	$4\ V$	$10\ V$	$20\ V$
a-IGZO				
$\rho(\Omega cm)$	6.09×10⁻¹	4.41×10⁻²	1.57×10⁻²	7.40×10⁻³
$C_i(F/cm^2)$		4.93×10⁻⁸		
a-ITZO				
$\rho(\Omega cm)$	1.48×10⁻¹	1.54×10⁻²	6.43×10⁻³	3.27×10⁻³
$C_i(F/cm^2)$		4.93×10⁻⁸		

Table III.3 The variations of ρ and C_i depending on the types of channel material.

From Table III.3, we note that the a-ITZO active layer exhibits much less resistivity than a-IGZO. In all cases these the resistivity increase with the increase of the gate tension.

III.3 Effect of high-k gate dielectrics

A good solution to the leakage current associated with the thinner thickness of the SiO_2 would be by increasing the physical thickness without increasing the effective thickness of the gate dielectric (the electrical thickness of gate dielectric). This is referred to what is known by the equivalent oxide thickness (EOT) which reduces the gate leakage current and at the same time keep an adequate gate capacitance per unit area [18].

The increase of the physical thickness without increasing the effective thickness of the gate dielectric can be achieved by replacing the low-k dielectric SiO_2 (*k=3.9*) with a high-k dielectric. According to relative approximation, the high-*k* dielectric can be physically thick without being electrically thick, leading to an increase of the gate capacitance per unit area without the associated leakage effects [19, 20]. For example, a high-k dielectric material with dielectric constant (*k=39*) compared to *3.9* for SiO_2 can be ten times thicker than SiO_2 which helps to reduce the leakage of electrons across the dielectric pad of gate.

III.3.1 Device structure

A simplified two-dimensional cross-section of the staggered bottom-gate a-ITZO TFT device structure used in this work is shown in Figure III.4(a, b). The device structure input parameters are summarized in Table III.4 for the case (a) when the SiO_2 is used as a gate dielectric. For the case (b) many high-k materials are used as a gate dielectric in the aim to study in more detail the effect of the corresponding EOT on the TFT performance. The structural and physical parameters of the used high-k materials are presented in Table III.3.

(a)

$L_{ov} = 10\ \mu m$ $L_{SD} = 5\ \mu m$ $L_{ov} = 10\ \mu m$

| Source (Mo) | | Drain (Mo) |

$T_{a\text{-}ITZO}$ Active channel layer (a-ITZO)   20 nm

T_{SiO_2} Low-k dielectric oxide layer (SiO₂)   (Variable)

Gate (Mo)

Glass substrate

(b)

$L_{ov} = 10\ \mu m$ $L_{SD} = 5\ \mu m$ $L_{ov} = 10\ \mu m$

| Source (Mo) | | Drain (Mo) |

$T_{a\text{-}ITZO}$ Active channel layer (a-ITZO)   20 nm

High-k dielectric oxide layer
(Variable)   100 nm

Gate (Mo)

Glass substrate
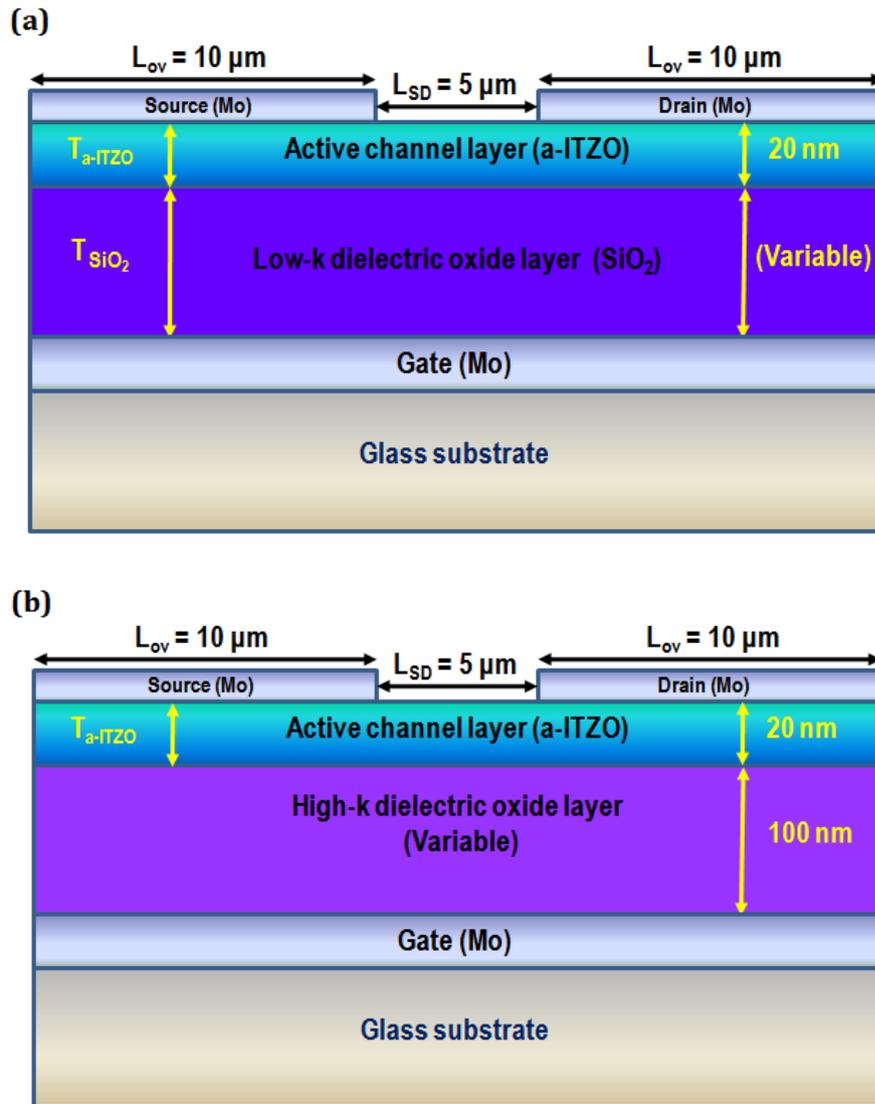
Figure III.4 Schematic diagram of a two-dimensional cross-section of the staggered bottom-gate a-ITZO TFT; dimensions, regions, and materials used in the simulation for (a) low-k SiO₂ gate dielectric and (b) high-k gate dielectric.

The generated structure and mesh of the a-ITZO TFT by Atlas from Silvaco is presented in Figure III.5.
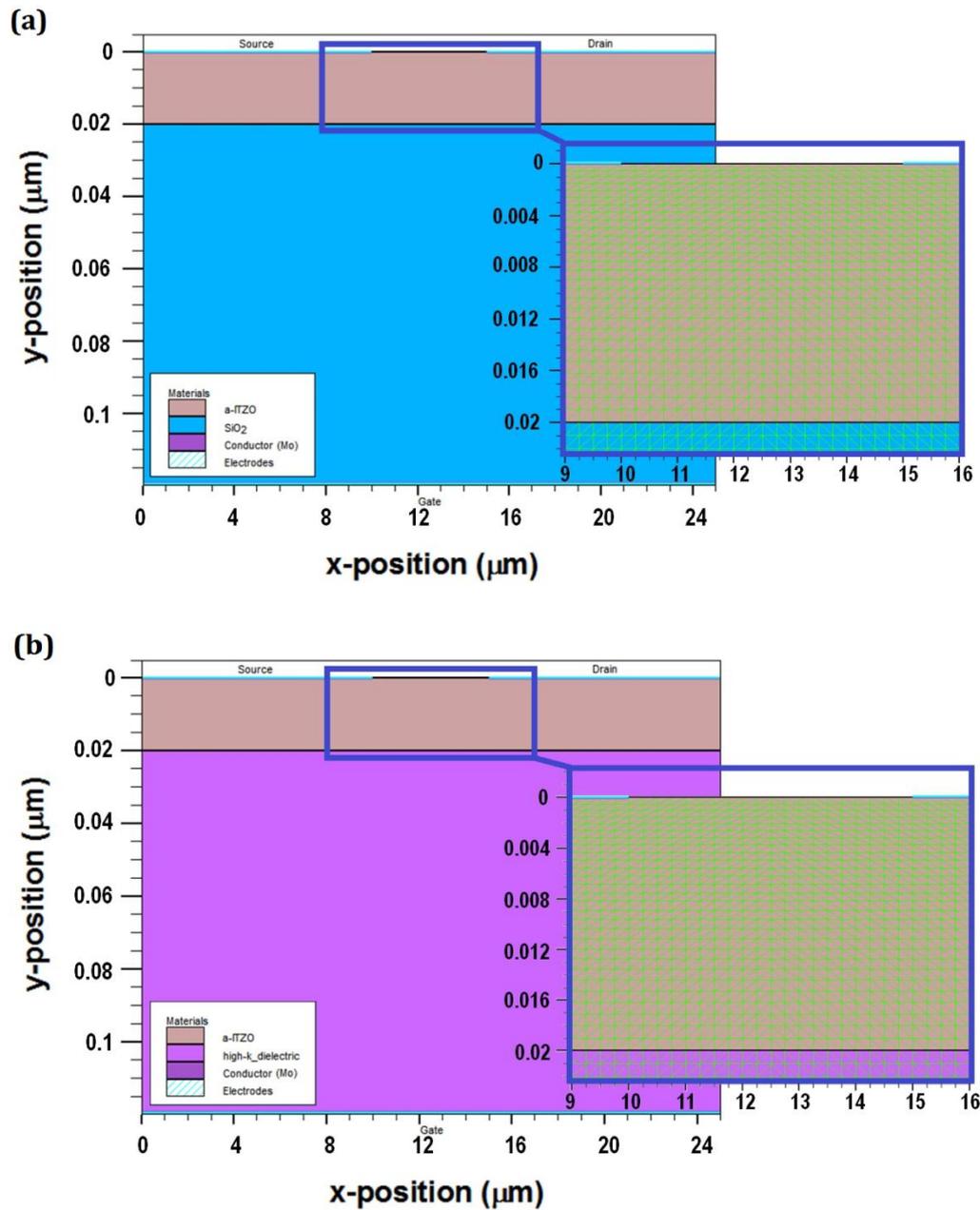
Figure III.5 The two-dimensional cross-section of the staggered bottom-gate a-ITZO TFT generated by Silvaco Atlas for (a) low-k SiO$_2$ gate dielectric and (b) high-k gate dielectric.

Region	Parameter	Description	Value	Ref
a-ITZO (n-type channel)	$L(\mu m)/W(\mu m)/T(nm)$	Length/Width/Thickness	25/10/20	[9]
	$N_d(cm^{-3})$	n doping concentration	4.62×10^{15}	[9]
	$E_g(eV)$	Band gap	3.02	[9]
	$\chi(eV)$	Electronic affinity	4.65	[13]
	$\mu_n/\mu_p\ (cm^2 V^{-1} s^{-1})$	Low-field electron/hole mobility	30/0.1	[9]
	$N_C/N_V\ (\times 10^{19}\ cm^{-3})$	Conduction/valence band density at $300K$	1.59/121	[9]
	$\sigma_{TAE}/\sigma_{TAH}\ (\times 10^{-16}\ cm^2)$	Capture cross-section for electrons/holes in CBT	1/100	[14]
	$\sigma_{TDE}/\sigma_{TDH}\ (\times 10^{-16}\ cm^2)$	Capture cross-section for electrons/holes in VBT	100/1	[14]
	$\sigma_{GDE}/\sigma_{GDH}\ (\times 10^{-16}\ cm^2)$	Capture cross-section for electrons in the shallow donor-like Gaussian states	100/1	[14]
SiO₂	$L(\mu m)/W(\mu m)/T(nm)$	Length/Width/Thickness	25/10/Variable	[9]
	$E_g(eV)$	Band gap	9	[9]
	k_{SiO_2}	The relative permittivity	3.9	[9]
Mo source and drain contacts	$L(\mu m)/W(\mu m)/T(nm)$	Length/Width/Thickness	10/10/0.1	[9]
	$L_{SD}(\mu m)$	The source-drain spacing	5	[9]
	$\Phi_{Mo}(eV)$	The work function of Mo	4.53	[15]
Mo gate (G) electrode contact	$L(\mu m)/W(\mu m)/T(nm)$	Length/Width/Thickness	25/10/0.1	[9]
	$L_{OV}(\mu m)$	The gate-to-S/D overlap length	10	[9]
	$\Phi_{Mo}(eV)$	The work function of Mo	4.53	[15]

Table III.4 The input parameters of the a-ITZO TFT devices.

High-k materials	L(μm)/W(μm)/T(nm)	Band gap energy (eV)	Relative permittivity
Si₃N₄	25/10/100	5 [21]	7.5 [21]
Al₂O₃	25/10/100	8.7 [22, 23]	8.5-10.5 [22, 23]
Y₂O₃	25/10/100	5.6 [21, 24]	12-20 [21, 24]
Gd₂O₅	25/10/100	5.4 [25]	12-23 [25]
Zr$_x$Si$_{1-x}$O$_y$	25/10/100	6 [25]	15-25 [25]
ZrO₂	25/10/100	5.8 [26]	25 [26]
CeO₂	25/10/100	5.5 [27]	26 [27]
La₂O₃	25/10/100	4.3 [21]	27 [21]
Ta₂O₅	25/10/100	4-4.5 [28, 29]	20-35 [28, 29]
HfO₂	25/10/100	5.7 [30]	35 [30]
TiO₂	25/10/100	3-3.5 [28]	30-100 [28]
Nb₂O₅	25/10/100	3.32-4.8 [31-34]	50-200 [31, 34]
SrZrO₃	25/10/100	5.4 [35]	180 [35]
BaSrTiO₃	25/10/100	3.03-3.4 [36, 37]	200-300 [37]
SrTiO₃	25/10/100	3.27 [38]	300 [37]

Table III.5 Band gap energy and relative permittivity of the used high-k dielectric materials to

study the EOT effect.

III.3.3 Effect of the physical thickness of the gate dielectric

Figure III.6 shows the effect of the SiO_2 gate dielectric thickness decrease on the transfer $(I_{DS} - V_{GS})$ characteristics of a-ITZO TFT (in the linear and semi-logarithmic plots).
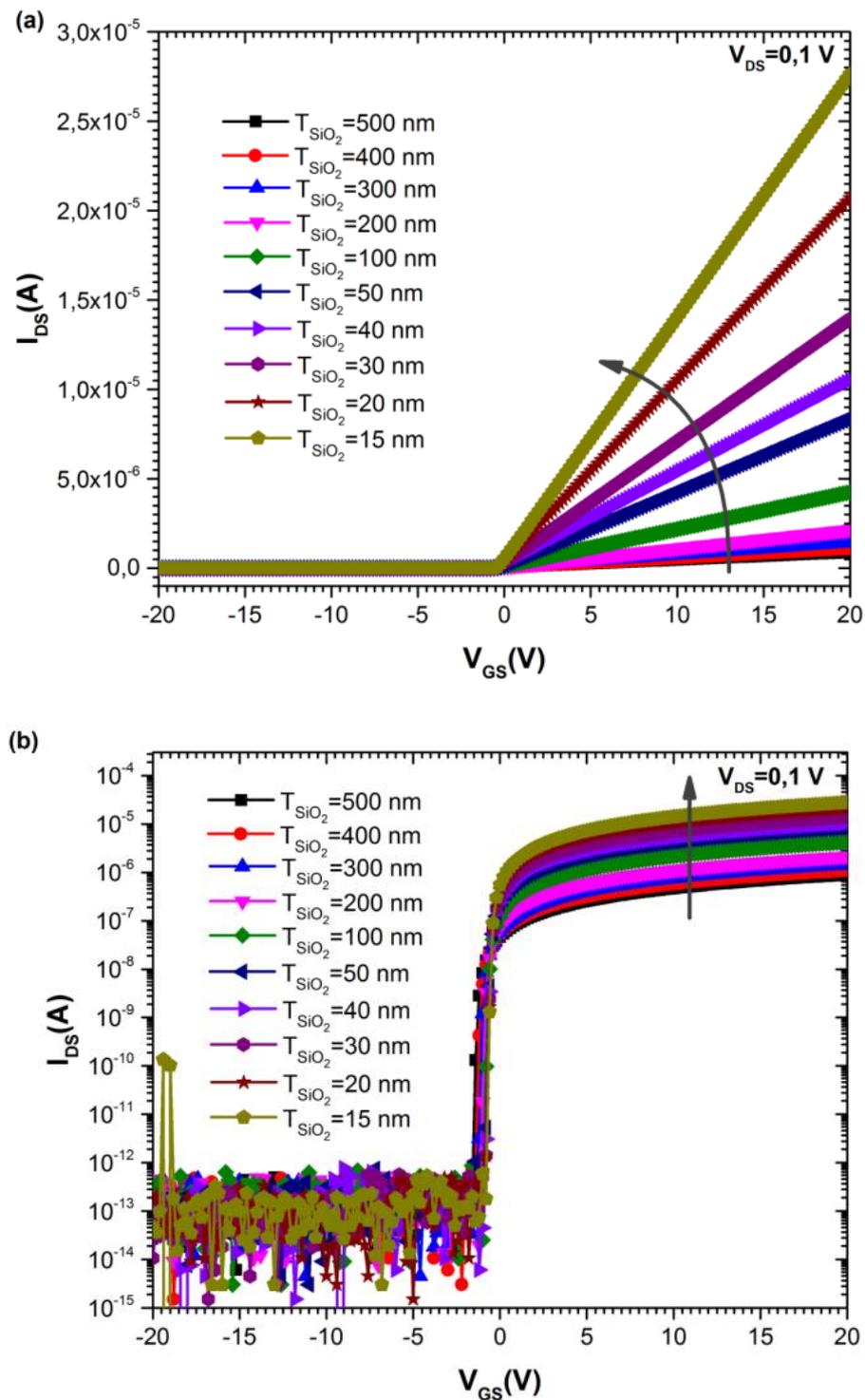
Figure III.6 The transfer $(I_{DS} - V_{GS})$ characteristics of the a-ITZO TFT depending on the SiO_2 gate dielectric thicknesses; (a) in the linear plot and (b) in the semi-logarithmic plot.

The obtained results approve the fact that the decrease of the SiO₂ gate dielectric thickness improves the transfer characteristic of the a-ITZO TFT by raising the source-drain current in the channel.

From the transfer characteristics in the linear plot (Figure III.6.a) are extracted V_T and μ_{FE}, while I_{on}, I_{on}/I_{off} ratio, SS, and V_{on} are calculated from the transfer characteristic curves in the semi-logarithmic plot (Figure III.6.b). The outputs obtained in addition to C_i, calculated using Equation I.16, are summarized in Table III.6.

T_{SiO_2} (nm)	C_i (F/cm^2)	$V_T(V)$	μ_{FE} ($cm^2V^{-1}s^{-1}$)	$I_{on}(A)$	I_{on}/I_{off}	$V_{on}(V)$	SS ($V/decade$)
500	6.91×10⁻⁹	-1.15	29.93	8.86×10⁻⁷	8.19×10⁶	-1.54	7.74×10⁻²
400	8.63×10⁻⁹	-1.05	29.89	1.10×10⁻⁶	1.02×10⁷	-1.39	7.63×10⁻²
300	1.15×10⁻⁸	-0.91	29.83	1.45×10⁻⁶	1.34×10⁷	-1.30	7.56×10⁻²
200	1.73×10⁻⁸	-0.75	29.78	2.15×10⁻⁶	1.99×10⁷	-1.08	7.45×10⁻²
100	3.45×10⁻⁸	-0.60	29.75	4.26×10⁻⁶	3.94×10⁷	-0.90	7.36×10⁻²
50	6.91×10⁻⁸	-0.51	29.69	8.42×10⁻⁶	7.80×10⁷	-0.88	7.23×10⁻²
40	8.33×10⁻⁸	-0.50	29.57	1.05×10⁻⁵	9.72×10⁷	-0.83	7.18×10⁻²
30	1.15×10⁻⁷	-0.48	29.47	1.40×10⁻⁵	1.30×10⁸	-0.81	7.14×10⁻²
20	1.73×10⁻⁷	-0.46	29.33	2.06×10⁻⁵	1.91×10⁸	-0.79	7.10×10⁻²
15	2.30×10⁻⁷	-0.44	29.21	2.76×10⁻⁵	2.55×10⁸	-0.75	6.09×10⁻²

Table III.6 The effect of the SiO₂ dielectric gate thickness (T_{SiO_2}) reduction on the extracted parameters: V_T, μ_{FE}, I_{on}, I_{on}/I_{off}, V_{on}, SS and C_i.

From the obtained results, the decrease in the SiO₂ gate dielectric thickness T_{SiO_2} from 500 nm to 15 nm improves significantly the a-ITZO TFT response since it leads to:

- The increase in I_{on} and I_{on}/I_{off} ratio, respectively, from $I_{on} = 8.86 \times 10^{-7} A$ and $I_{on}/I_{off} = 8.19 \times 10^6$ to $I_{on} = 2.76 \times 10^{-5} A$ and $I_{on}/I_{off} = 2.55 \times 10^8$.

- The increase in the capacitance per unit area from $C_i = 6.91 \times 10^{-9} \, F/cm^2$ to $C_i = 2.30 \times 10^{-7} \, F/cm^2$.

- A significant decrease in the threshold voltage from $V_T = -1.15 \, V$ to $V_T = -0.44 \, V$.

- A decrease in the subthreshold swing from the value $SS = 7.74 \times 10^{-2} \, V/decade$ to the value $SS = 6.09 \times 10^{-2} \, V/decade$.

- A reduction in the turn-on voltage from the value $V_{on} = -1.54 \, V$ to the value $V_{on} = -0.75 \, V$.

However, the field-effect mobility seems to be slightly influenced by the SiO$_2$ thickness reduction since it decreases slightly from the value $\mu_{FE} = 29.93 \, cm^2 V^{-1} s^{-1}$ to the value $\mu_{FE} = 29.21 \, cm^2 V^{-1} s^{-1}$.

We can confirm that the decrease of the SiO$_2$ thickness is beneficial for the TFT performance improvement. However, if the thickness is more reduced (to $2\sim 1 \, nm$), this leads to the appearance of the quantum effect such as the current leakage toward the gate. This induces power dissipation through the device and consequently it reliability becomes unstable.

III.3.4 Effect of the effective thickness of the gate dielectric

To avoid this issue the SiO$_2$ is replaced by high-k dielectric materials that can be thicker physically without being thicker electrically. However, most of the high-k dielectric materials have band gap energy lower than SiO$_2$ gap energy (Figure III.7), since there is almost an inverse relationship between the dielectric constant (k) and the band gap energy (E_g). Therefore, it is preferred to use dielectric materials having a band gap energy larger enough to reduce the current leakage through the gate dielectric. The values of the dielectric constant (k) and the band gap energy E_g for different dielectric materials are shown in Figure III.7.
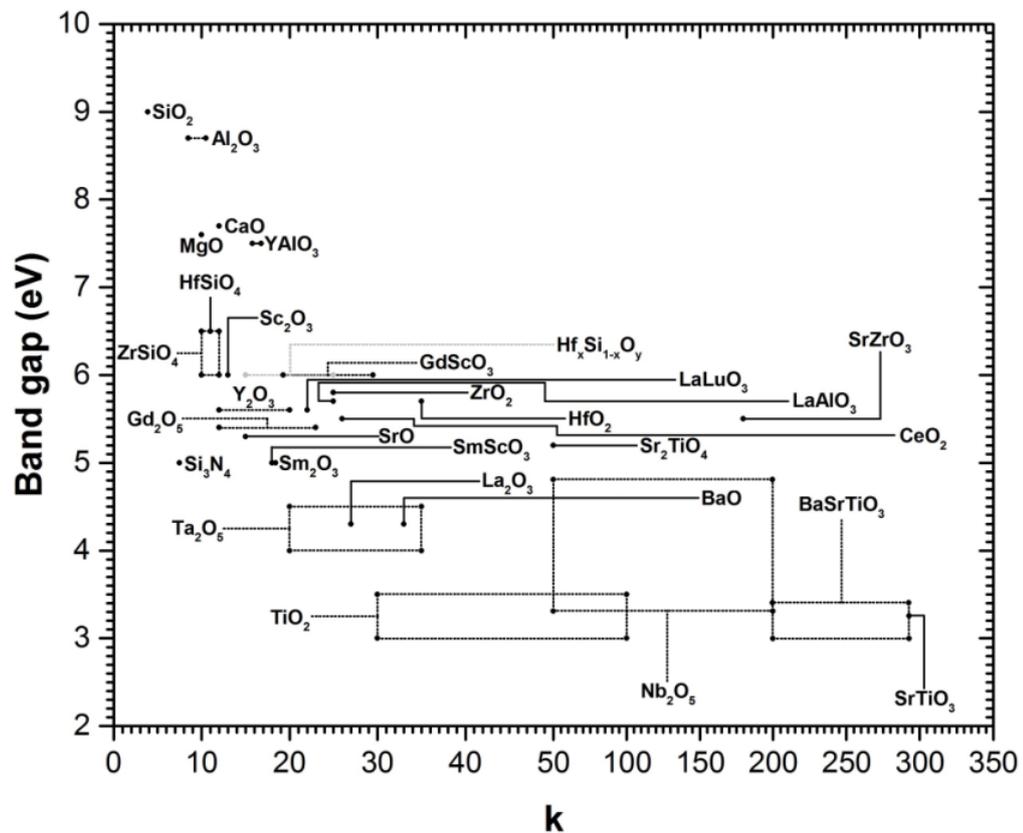
Figure III.7 Band gap energy as a function of the dielectric constant for different dielectric materials [17, 23-42].

Consequently, the optimal dielectric materials are those that have a high dielectric constant and a wide band gap. Most of the prominent materials for this purpose (From Figure III.7) are Al_2O_3, CaO, MgO, $YAlO_3$, $HfSiO_4$, $GdScO_3$, $GdScO_3$, ZrO_2, $Hf_xSi_{1-x}O_y$, $LaLuO_3$, $LaAlO_3$, $SrZrO_3$, CeO_2, HfO_2, and Sr_2TiO_4.

In order to confirm the relationship between the dielectric constant, the *EOT* and the a-ITZO TFT performance, the SiO_2 is replaced by a number of dielectric materials that are given in Table III.7.

Figure III.8 shows the evolution of the transfer characteristics of the a-ITZO TFT using the gate dielectrics given in Table III.7. The extracted outputs are summarized in Table III.8.

Dielectric materials	Dielectric constant (k)	Band gap energy (E_g)
SiO_2	3.9	9
Si_3N_4	7.5	5
Al_2O_3	9.5	8.7
Y_2O_3	16	5.6
Gd_2O_5	18	5.4
$Zr_xSi_{1-x}O_y$	20	6
ZrO_2	25	5.8
CeO_2	26	5.5
La_2O_3	27	4.3
Ta_2O_5	27.5	4.25
HfO_2	35	5.7
TiO_2	65	3.25
Nb_2O_5	125	4.06
$SrZrO_3$	180	5.4
$BaSrTiO_3$	250	3.21
$SrTiO_3$	300	3.27

Table III.7 Dielectric constants and band gap energies for a set of gate dielectrics.
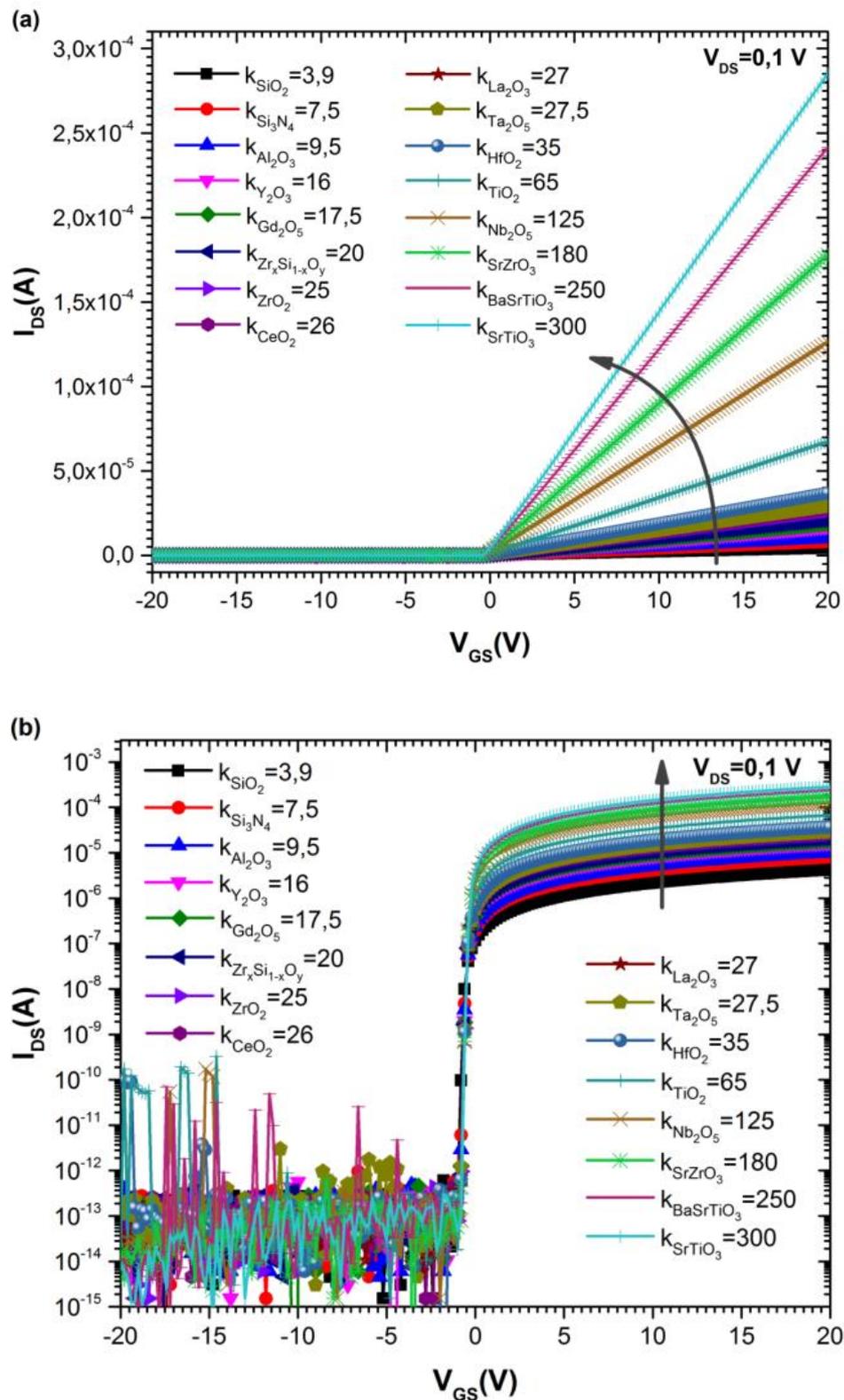
Figure III.8 The transfer ($I_{DS} - V_{GS}$) characteristics of the a-ITZO TFT depending on the dielectric constant; (a) linear plot and (b) semi-logarithmic plot.

| dielectric	k	EOT (nm)	C_i (F/cm^2) $\times 10^{-8}$	$V_T(V)$	μ_{FE} ($cm^2 V^{-1} s^{-1}$)	I_{on} (µA)	I_{on}/I_{off}	$V_{on}(V)$	SS (V/dec) $\times 10^{-2}$
SiO_2	3.9	100	3.45	-0.610	29.75	2.23	2.06×10^7	-0.957	7.59
Si_3N_4	7.5	52	6.64	-0.559	29.73	8.08	7.48×10^7	-0.937	6.91
Al_2O_3	9.5	41.05	8.41	-0.544	29.71	10.2	9.44×10^7	-0.874	6.60
Y_2O_3	16	24.37	14.2	-0.527	29.69	17.0	1.57×10^8	-0.835	6.35
Gd_2O_5	18	22.28	15.9	-0.520	29.68	18.6	1.72×10^8	-0.833	6.31
$Zr_xSi_{1-x}O_y$	20	19.5	17.7	-0.511	29.67	21.4	1.98×10^8	-0.821	6.30
ZrO_2	25	15.6	22.1	-0.501	29.65	26.5	2.46×10^8	-0.813	6.21
CeO_2	26	15	23.0	-0.493	29.64	27.4	2.54×10^8	-0.800	6.14
La_2O_3	27	14.44	23.9	-0.485	29.63	28.6	2.65×10^8	-0.796	6.02
Ta_2O_5	27.5	14.18	24.3	-0.480	29.62	29.2	2.70×10^8	-0.793	5.98
HfO_2	35	11.14	31.0	-0.471	29.59	36.7	3.40×10^8	-0.790	5.96
TiO_2	65	6	57.5	-0.460	29.42	67.3	6.23×10^8	-0.783	5.86
Nb_2O_5	125	3.12	111	-0.449	29.38	126	1.17×10^9	-0.775	5.79
$SrZrO_3$	180	2.17	159	-0.443	29.22	178	1.65×10^9	-0.764	5.63
$BaSrTiO_3$	250	1.56	221	-0.435	29.11	241	2.23×10^9	-0.750	5.27
$SrTiO_3$	300	1.3	266	-0.428	29.03	286	2.65×10^9	-0.749	5.04

Table III.8 The variations of the extracted parameters: EOT, C_i, V_T, μ_{FE}, I_{on}, I_{on}/I_{off}, V_{on}, and SS, respectively, depending on the dielectric constant (k).

When the dielectric constant increases from 39 to 300, the obtained results indicate that this leads to the increase in I_{on}, I_{on}/I_{off} ratio and C_i and a decrease in EOT, V_T, μ_{FE}, V_{on}, and SS. In more details:

- The equivalent oxide thickness decreases, according to Equation I.21, from $EOT = 100\ nm$ to $EOT = 1.3\ nm$.

- The capacitance per unit area increases from the value $C_i = 3.45 \times 10^{-8}\ F/cm^2$ to the value $C_i = 2.66 \times 10^{-6}\ F/cm^2$, according to Equation I.24, due to the decrease of EOT.

- The current I_{on} and the I_{on}/I_{off} ratio increase significantly from the values $I_{on} = 2.23 \times 10^{-6}\ A$ and $I_{on}/I_{off} = 2.06 \times 10^7$, respectively, to the values $I_{on} = 2.86 \times 10^{-4}\ A$ and $I_{on}/I_{off} = 2.65 \times 10^9$. This is due to the increase in capacitance per unit area and leads to a high response velocity (fast reaction) of the device.

- The threshold voltage decreases from the value $V_T = -0.610\ V$ to the value $V_T = -0.428\ V$.

- The subthreshold swing decreases from the value $SS = 7.59 \times 10^{-2} \, V/decade$ to the value $SS = 5.04 \times 10^{-2} \, V/decade$.

- The turn-on voltage decreases from the value $V_{on} = -0.957 \, V$ to the value $V_{on} = -0.749 \, V$.

However, the field-effect mobility exhibits less sensitivity since it decreases slightly from the value $\mu_{FE} = 29.75 \, cm^2 V^{-1} s^{-1}$ to the value $\mu_{FE} = 29.03 \, cm^2 V^{-1} s^{-1}$. This is due to the presence of similar changes in the capacitance per unit area and the maximum slope of the transfer characteristic in the linear plot.

As results indicate above, the more influenced parameters by the increase of the dielectric constant (k) are the capacitance per unit area and the source-drain current while the other parameters present slight variations. This can be attributed to the fact that the transfer characteristics of a-ITZO TFTs were calculated in the ideal case without taking into account the presence of possible defects at the semiconductor/dielectric (a-ITZO/dielectric) interface namely in case of high-k dielectrics. Because practically, the situation is more complicated for the devices that use high-k dielectrics in combination with semiconductors such as TFT, which requires the search for an experimental model for the density of interface trap states for each high-k dielectric material to extract the device parameters, which can vary greatly depending on the density value of the semiconductor/dielectric (a-ITZO/dielectric) interface defects. In this case, it is expected that besides the channel current and the capacitance more effects will occur in the other output parameters, especially in V_T and V_{on}, which can be severely affected by this type of defect.

III.4 Effect of bi-layer dielectrics

The band gap energy of the chosen high-k dielectrics should be high enough to prevent again the current leakage. The chosen high-k dielectrics are oxides of the transition metals such as TaO_2, TiO_2, Al_2O_3, ZrO_2, and HfO_2, ferroelectric materials such as $BaSrTiO_3$, and metal

silicates such as $ZrSiO_4$ and $HfSiO_4$. Promising results, namely a significant increase of the channel current, were obtained especially when the dielectric constant (k) exceeds 200 with a band gap energy > 3 eV.

In the future, there is hope to introduce high-k dielectric materials with a larger energy band gap and a higher dielectric constant, in addition to a good quality interface, a low interface trap density, and good morphological properties as well as a good thermal stability, which are indispensable in the TFT technology of the next generation.

However, another problem has to be mentioned which is that most of the high-k dielectric materials have much poorer properties than the conventional SiO_2, such as a low interface quality (larger interface and bulk trap density compared to SiO_2), poor morphological properties, and a low thermal stability [39]. In addition, the most high-k dielectrics have energy band gap less than that of SiO_2, while it is known that the dielectric materials that have higher band gap energy can prevent or reduce the current leakage through the gate dielectric with less thickness than the dielectrics that have a lower band gap energy [40].

A better solution would be to using a bi-layer dielectric consisting of a very thin dielectric layer which possesses good morphological properties such as SiO_2 ($k = 3.9$) and another thicker dielectric layer with high-dielectric constant (high-k) such as HfO_2 ($k = 35$). This design gives a better interface quality (low interface traps density) and a lower effective gate dielectric oxide.

The used dielectric oxides (low-k/high-k) in this work are SiO_2/HfO_2, with a large physically thickness and relatively small EOT. Despite the fact that most of the bi-layer dielectric oxides have a large physically thickness, they have relatively small EOT. As it is a technology of a great interest not only for scaling down transistor sizes but also because it is a low-temperature technology. In addition, the fundamental role of the interfacial layer of low-k

dielectric oxide between the high-mobility channel and the high-k dielectric oxide layer, which has some beneficial qualities with regard to carrier mobility in the device channel [41, 42].

However, if we consider the poor quality of the interface of the high-k materials, we will get much less performance. This is the reason why we used a capacitor based on a bi-layer dielectric (SiO$_2$/HfO$_2$) with a higher total physical thickness (70 nm). The addition of the SiO$_2$ layer is in the aim to prevent the poor quality of the HfO$_2$ interface. This bi-layer region is equivalent electrically to a thinner SiO$_2$ layer (10 nm), without the associated leakage effects (ALE).

This means as shown in Figure III.9.a, that a capacitor based on the bi-layer dielectric (SiO$_2$/HfO$_2$) with a total physical thickness of 70 nm, can provide the same electrical characteristics and then the same electrical properties that are offered by capacitor based on the equivalent oxide to a thinner SiO$_2$ ($EOT = 10\ nm$), Figure III.9.b, without ALE.

It also provides electrical properties better than the capacitor based on the mono-layer SiO$_2$ dielectric, for the same physical thickness, 70 nm, presented in Figure III.9.c.
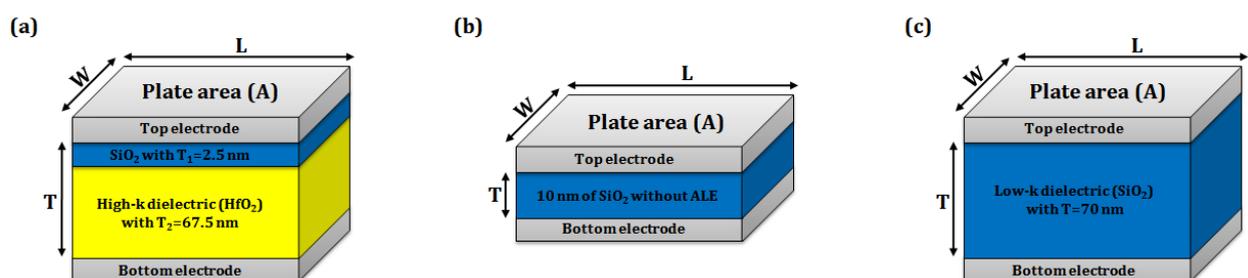
Figure III.9 Schematic diagram of the three-dimensional structure of a simple parallel plate capacitor depending on the different types of gate dielectrics: (a) 70 nm of a bi-layer dielectric oxide (SiO$_2$/HfO$_2$), (b) 10 nm of SiO$_2$ without associated leakage effect (ALE) and (c) 70 nm of SiO$_2$.

III.4.1 Device structure

Two-dimensional cross-section of the bottom-gate a-ITZO-based TFT devices structure, regions, materials, and dimensions are shown in Figure III.10, while a schematic structure of the simulated a-ITZO TFTs produced by Atlas is shown in Figure III.11. The input parameters of the devices are summarized in Table III.9.
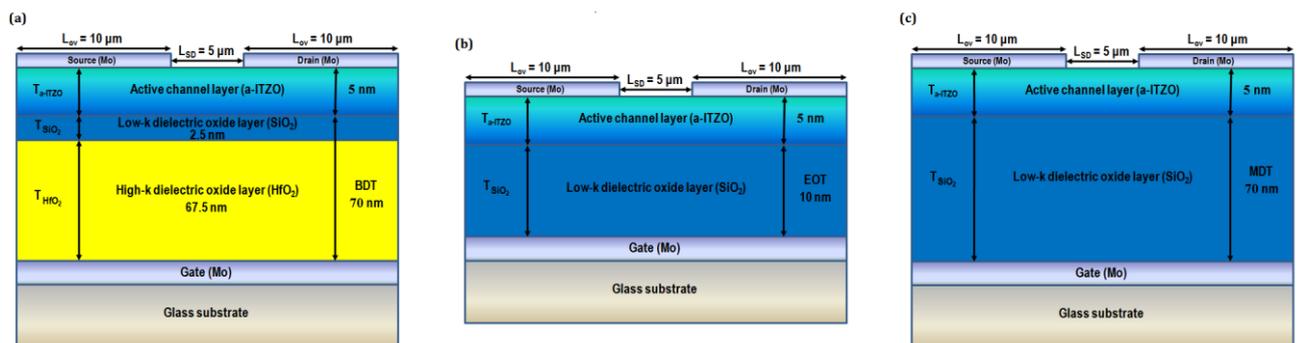
Figure III.10 Schematic diagram of a two-dimensional cross-section of the bottom-gate a-ITZO TFTs structure, dimensions, regions, and materials depending on the different types of gate dielectrics.
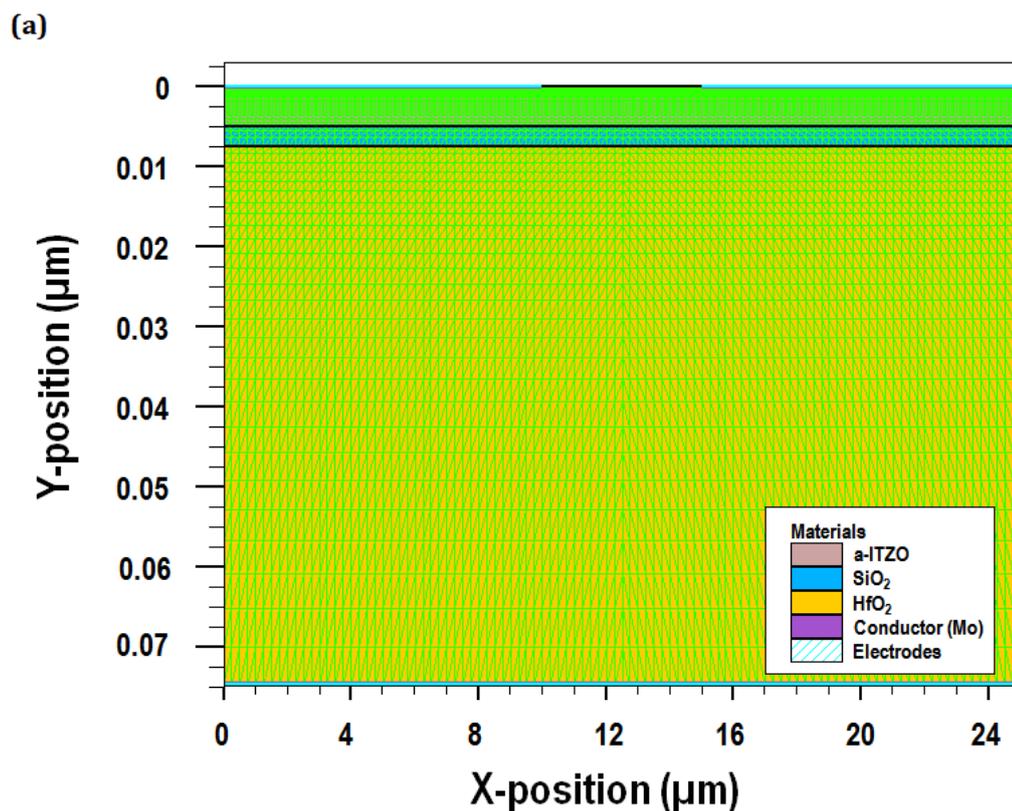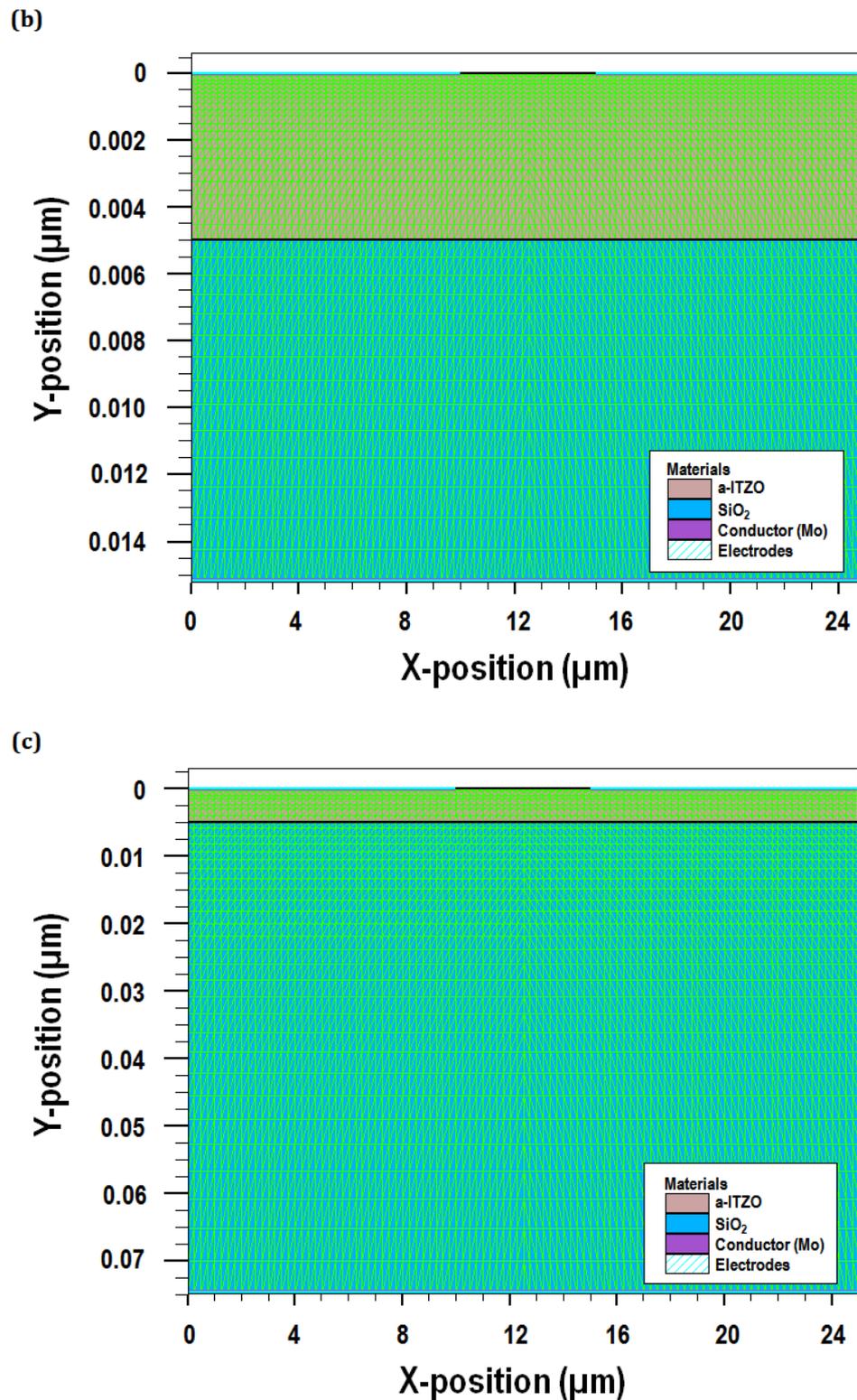
Figure III.11 Schematic diagram of the two-dimensional cross-section of the bottom-gate a-ITZO TFT structures generated by Silvaco Atlas depending on the different types of gate dielectrics: (a) 70 nm of the bi-layer low-k(SiO_2)/high-k(HfO_2) gate dielectric, (b) the equivalent 10 nm of SiO_2 without ALE and (c) 70 nm of low-k SiO_2 gate dielectric.

Region	Parameter	Description	Value	Ref
a-ITZO (n-type channel)	$L(\mu m)/W(\mu m)/T(nm)$	Length/Width/Thickness	25/10/5	[9], Con
	$N_d(cm^{-3})$	The n doping concentration	5.14×10^{15}	[9]
	$E_g(eV)$	Band gap	3.02	[9]
	$\chi(eV)$	Electronic affinity	4.65	[13]
	$\mu_n/\mu_p \ (cm^2V^{-1}s^{-1})$	Low-field electron/hole mobility	30/0.1	[9]
SiO$_2$	$L(\mu m)/W(\mu m)/T(nm)$	Length/Width/Thickness	25/10/Var	[9]
	$E_g(eV)$	Band gap	9	[9]
	k_{SiO_2}	The relative permittivity	3.9	[9]
HfO$_2$	$L(\mu m)/W(\mu m)/T(nm)$	Length/Width/Thickness	25/10/67.5	[9], Con
	$E_g(eV)$	Band gap	5.7	[30]
	k_{HfO_2}	The relative permittivity	30	[30]
Mo source and drain contacts	$L(\mu m)/W(\mu m)/T(nm)$	Length/Width/Thickness	10/10/0.1	[9, 10]
	$L_{SD}(\mu m)$	The source-drain spacing	5	[9]
	$\Phi_{Mo}(eV)$	The work function of Mo	4.53	[15]
Mo gate electrode contact	$L(\mu m)/W(\mu m)/T(nm)$	Length/Width/Thickness	25/10/0.1	[9, 10]
	$L_{OV}(\mu m)$	The gate-to-S/D overlap length	10	[9]
	$\Phi_{Mo}(eV)$	The work function of Mo	4.53	[15]

Table III.9 Structure input parameters of the a-ITZO-based TFT.

III.4.2 Effect of equivalent oxide thickness (EOT) of the gate dielectric

A bi-layer dielectric is employed which consists of a very thin low-k SiO$_2$ dielectric layer ($k = 3.9$) that ensures a low interface traps density with the channel in the juxtaposition of a high-k HfO$_2$ ($k = 35$) dielectric layer relatively thicker. This bi-layer provides a lower electrical dielectric thickness (a lower effective gate dielectric thickness) (Figure III.12).
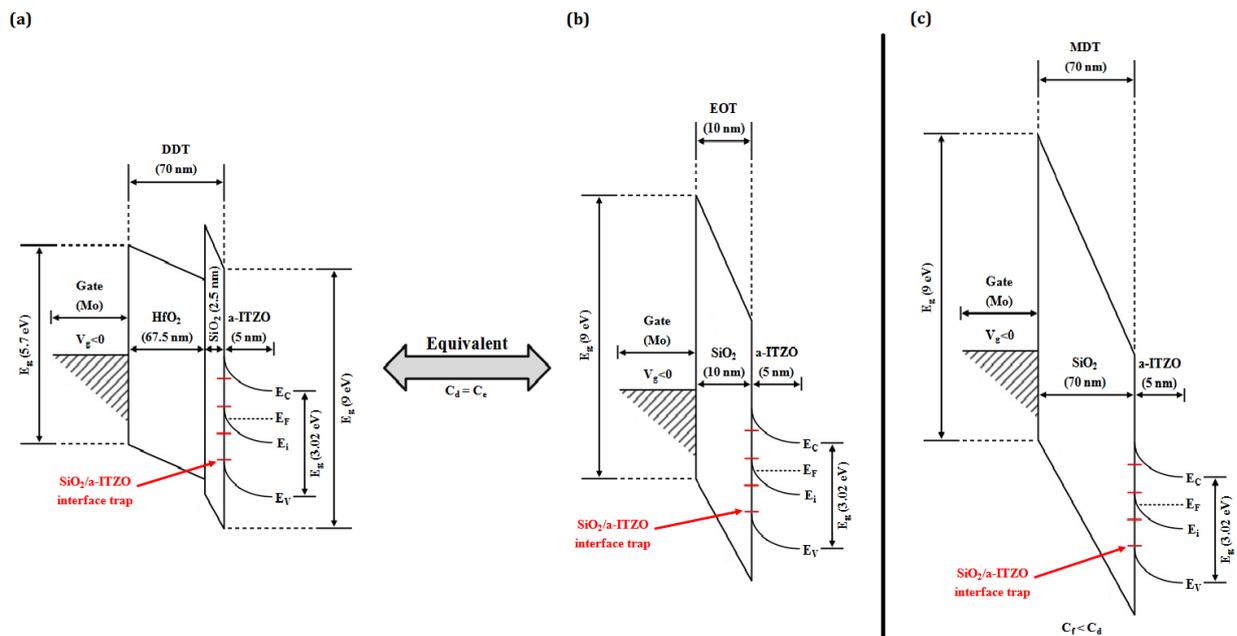
Figure III.12 Schematic band energy diagram of the channel/dielectric interface in the a-ITZO TFT with (a) 70 nm of the bi-layer SiO$_2$/HfO$_2$ gate dielectric, (b) the equivalent 10 nm of SiO$_2$ without ALE and (c) 70 nm of SiO$_2$ mono-layer.

Figure III.13 presents the transfer ($I_{DS} - V_{GS}$) characteristics (linear plot and semi-logarithmic plot) for the three cases considered in this study and a fourth additional case for comparison:

- a bi-layer (SiO$_2$/HfO$_2$) with a total thickness of 70 nm (named case (a)). This bi-layer oxide is equivalent to 10 nm of SiO$_2$ without the associated leakage current.

- a 10 nm of a single thinner layer of SiO$_2$ (named case (b)).

- a thicker SiO$_2$ layer of 70 nm (named case (c)).

- a thicker SiO$_2$ layer of 70 nm but with a-IGZO as channel material (named case (d)). This case has been added to position the performance of the TFTs studied compared to the conventional a-IGZO TFT. The material and structure input parameters used for the a-IGZO are identical to those given in [4].
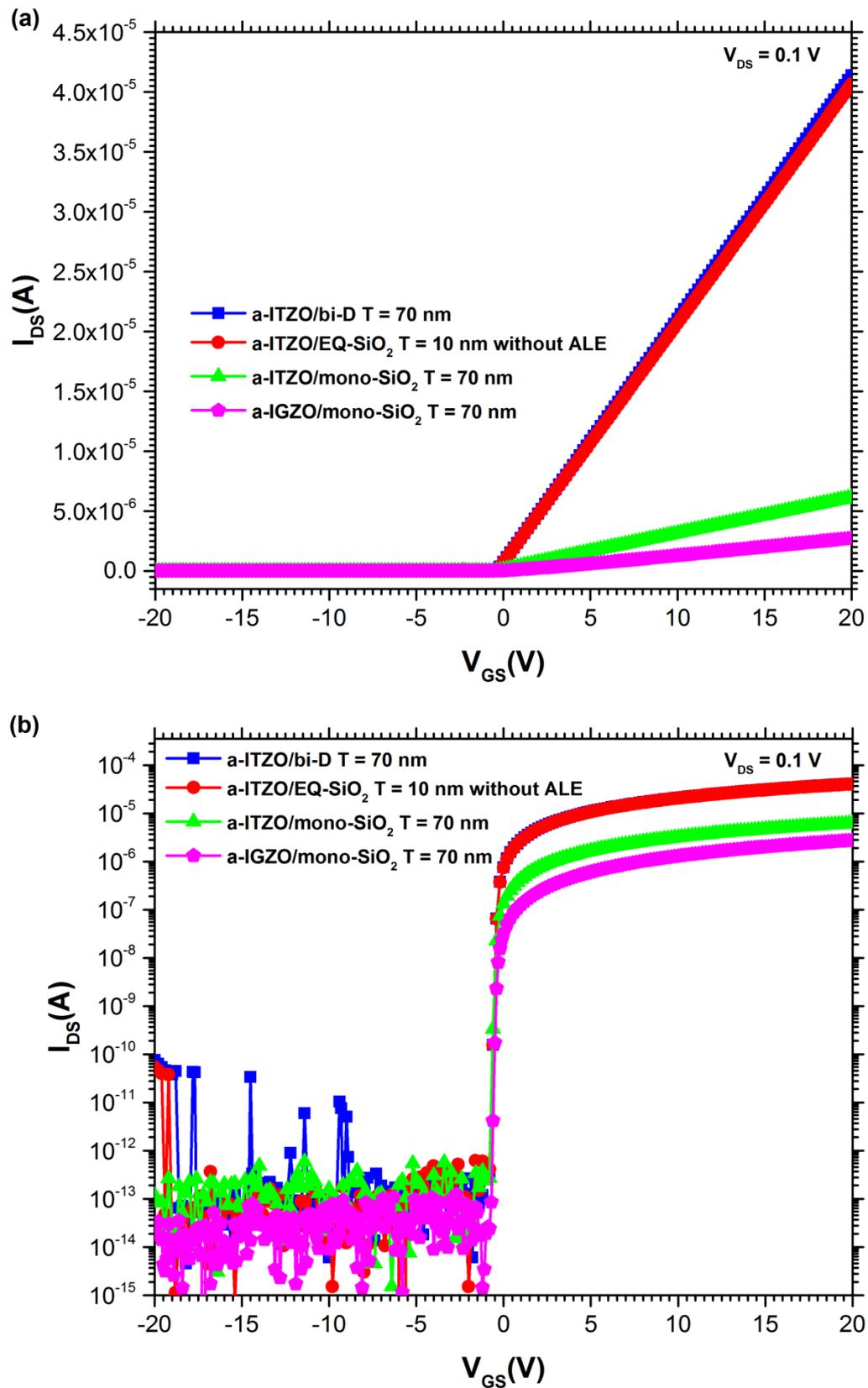
Figure III.13 The simulated a-ITZO TFT transfer ($I_{DS} - V_{GS}$) characteristics for the different

types of the gate dielectrics: (a) in the linear plot and (b) in the semi-logarithmic plot.

From the obtained curves the a-ITZO TFTs exhibits better performance than the conventional a-IGZO TFT. The cases (a) and (b) provide the same electrical characteristics which are better than the case (c). However in fact for the case (b) if we take into account the associated leakage current the real transfer characteristic will be poorer. In this case, the situation is more complex, requiring correction of quantum mechanics to extract the cumulative capacitance and extracting the parameters of the device which will greatly depend on the leakage current value.

Then the use of the bi-layer dielectrics (case (a)) is more suitable in comparison to a single thinner layer of SiO$_2$ (case (b)) with the associated leakage current. It is also preferred than 70 nm of pure SiO$_2$ (case(c)) with the related capacitance decrease. The case (a) with a total physical thickness of 70 nm and electrical thickness of 10 nm prevent at the same time the leakage current and the capacitance reduction. This leads to raising the current with lowering energy consumption and then raising transistor performance as well as improving device reliability. This will be confirmed by the electrical output extraction in the next.

From the transfer characteristic curves in the linear plot (Figure III.13.a), we calculated both V_T and μ_{FE}, while from the transfer characteristic curves in the semi-logarithmic plot (Figure III.13.b) we calculated the following parameters: SS, V_{on}, I_{on} and I_{on}/I_{off} ratio.

All the results obtained for the previous parameters (output parameters) of the a-ITZO TFT devices as well as the gate capacitance per unit area are presented in Table III.10.

Case	$C_i(F/cm^2)$	$V_T(V)$	$SS(V/decade)$	$\mu_{FE}(cm^2V^{-1}s^{-1})$	$I_{on}(A)$	I_{on}/I_{off}	$V_{on}(V)$
(a)	3.45×10^{-7}	-0.45	6.42×10^{-2}	29.34	4.12×10^{-5}	4.67×10^8	-0.79
(b)	3.45×10^{-7}	-0.45	6.45×10^{-2}	29.36	4.08×10^{-5}	4.62×10^8	-0.79
(c)	4.93×10^{-8}	-0.50	6.80×10^{-2}	29.96	6.15×10^{-6}	6.97×10^7	-0.80
(d)	4.93×10^{-8}	0.56	7.63×10^{-2}	14.86	2.76×10^{-6}	3.36×10^7	-1.01

Table III.10 The a-ITZO TFT parameters extracted for cases (a), (b) and (c). Case (d) is

extracted parameters for the conventional a-IGZO TFT.

Indeed from the obtained results, summarized in Table III.10, the cases (a) and (b) gives almost the same optimum electrical outputs. But we remember that for the case (b) these results are ideal (since the ALE is not taking into account). For the a-IGZO TFT (case (d)), the obtained results confirm that its electrical outputs are poorer than that of a-ITZO TFTs.

Returning to the three first cases, degradation is noticed in case (c) particularly in the capacitance which decreases from 3.45×10^{-7} to 4.93×10^{-8} F/cm^2 and in both I_{on} and I_{on}/I_{off} ratio that decrease respectively from $\sim4.1\times10^{-5}$ to 6.15×10^{-6} A and from 4.6×10^8 to 6.97×10^7. While for the other parameters the variations are practically insignificant.

The optimum values of C_i, I_{on} and I_{on}/I_{off} ratio leads to a higher transfer speed (fast response) of the transistor.

Figure 14.a and 14.b show, respectively, the calculated EOT and C_i depending on the dielectric constant k and the physical thickness of the dielectric material.

The EOT decreases by increasing k and/or by decreasing the physical thickness of the dielectric material. Similarly by doing this C_i increases.

(a)

(b)
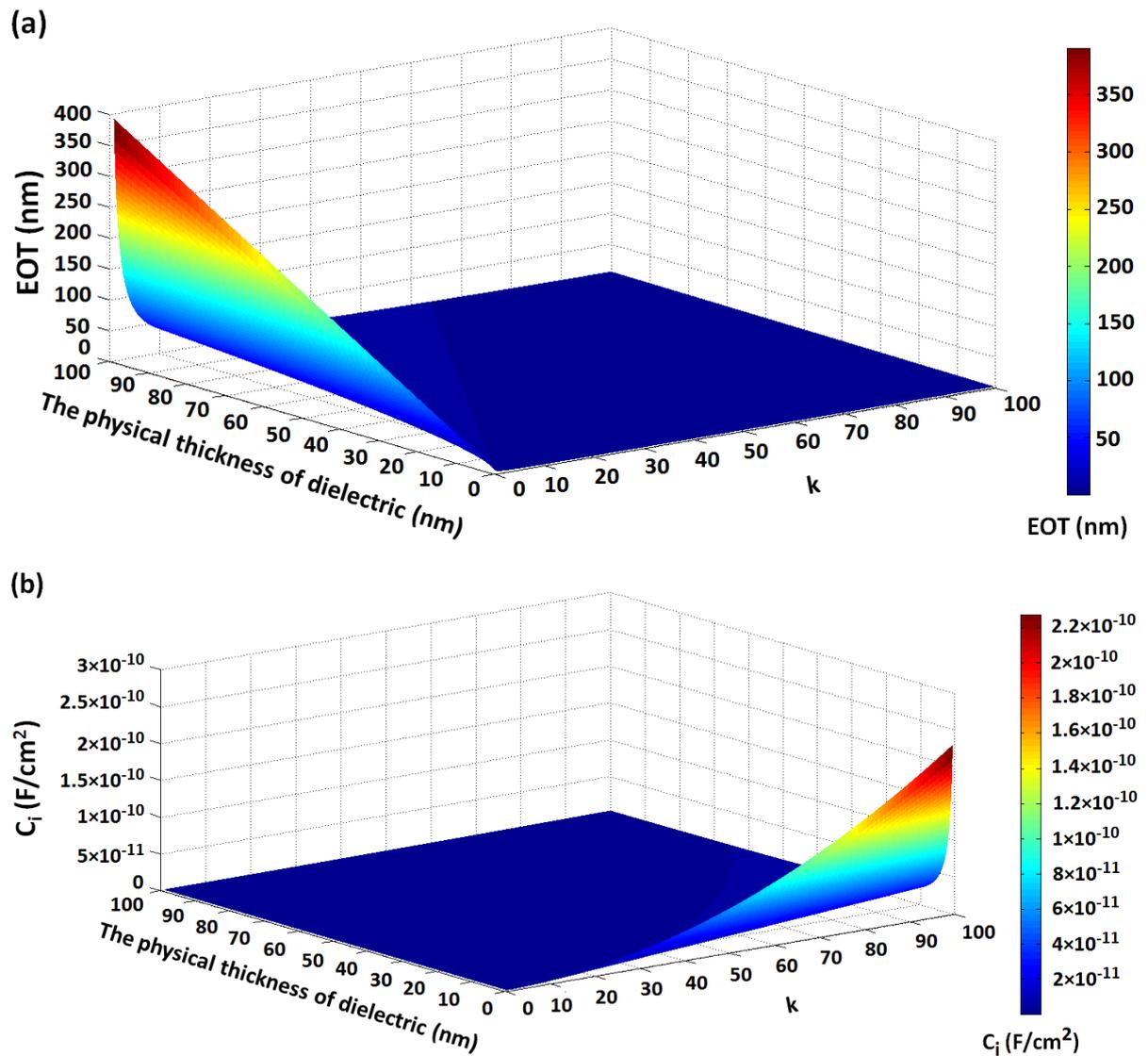
Figure III.14 The evolutions of (a) the EOT and (b) C_i depending on k and the physical thickness

of the dielectric material.

Figure III.15 presents the evolution of the $I_{DS} - V_{DS}$ characteristics for different gate

voltages (V_{GS}). Cases (a) and (b) gives almost identical variations while case (c) shows a lower

feature. Taking into account that the $(I_{DS} - V_{DS})$ characteristic of the case (b) is ideal (since the

ALE is neglected), it is obvious that the case (a) is more suitable then (b) and (c) to achieve a

better response of the TFT.
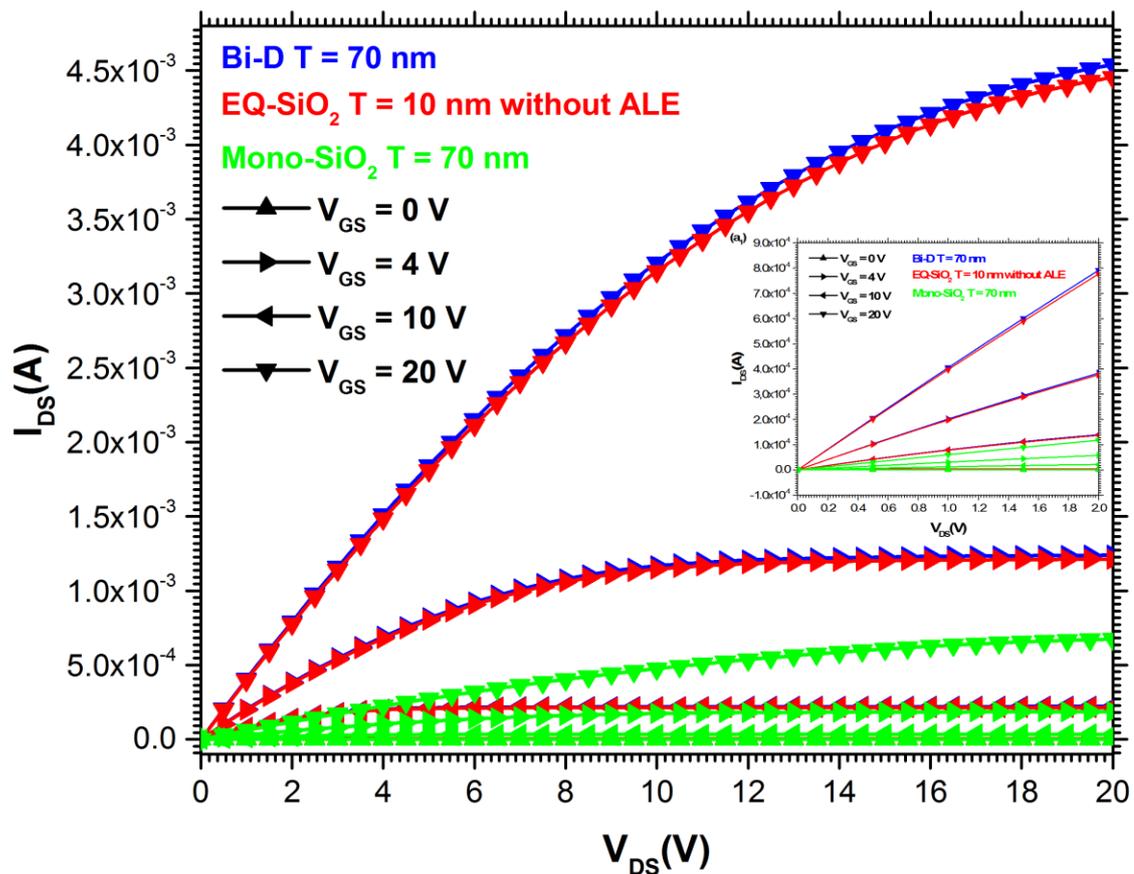
Figure III.15 The evolution of the $I_{DS} - V_{DS}$ characteristics of the a-ITZO TFTs depending on the different types of the gate dielectrics: bi-layer dielectric thickness (Bi-D T), equivalent SiO$_2$ thickness (EQ- SiO$_2$ T) and monolayer SiO$_2$ thickness (Mono-SiO$_2$ T).

From the $I_{DS} - V_{DS}$ characteristics, we calculated the electrical resistivity of the active layer of a-ITZO TFT. Results are listed in Table III.11.

$V_{GS}(V)$	$0\,V$	$4\,V$	$10\,V$	$20\,V$
$Case\,(a)$				
$\rho(\Omega cm)$	2.60×10^{-2}	2.36×10^{-3}	9.68×10^{-4}	4.87×10^{-4}
$C_i(F/cm^2)$		3.45×10^{-7}		
$Case\,(b)$				
$\rho(\Omega cm)$	2.64×10^{-2}	2.40×10^{-3}	9.86×10^{-4}	4.96×10^{-4}
$C_i(F/cm^2)$		3.45×10^{-7}		
$Case(c)$				
$\rho(\Omega cm)$	1.48×10^{-1}	1.54×10^{-2}	6.43×10^{-3}	3.27×10^{-3}
$C_i(F/cm^2)$		4.93×10^{-8}		

Table III.11 The calculated ρ and C_i for the cases (a), (b) and (c).

Indeed from the obtained results, the case (a) gives the lower resistivity values which ensure the better response of the TFT.

III.4.3 Effect of the oxide and interface states

We finish this study by examining separately the effect of the interface states that may be between the two dielectrics SiO_2 and HfO_2 of the a-ITZO bi-layer dielectrics and the defect states that can be in the SiO_2. The last one can interact with free carriers in the channel and induce a charge trapping in the oxide.

Figure III.16 shows the transfer $(I_{DS} - V_{GS})$ characteristics (linear plot and semi-logarithmic plot) for different interface state densities. The output parameters extracted in this case are summarized in Table III.12.
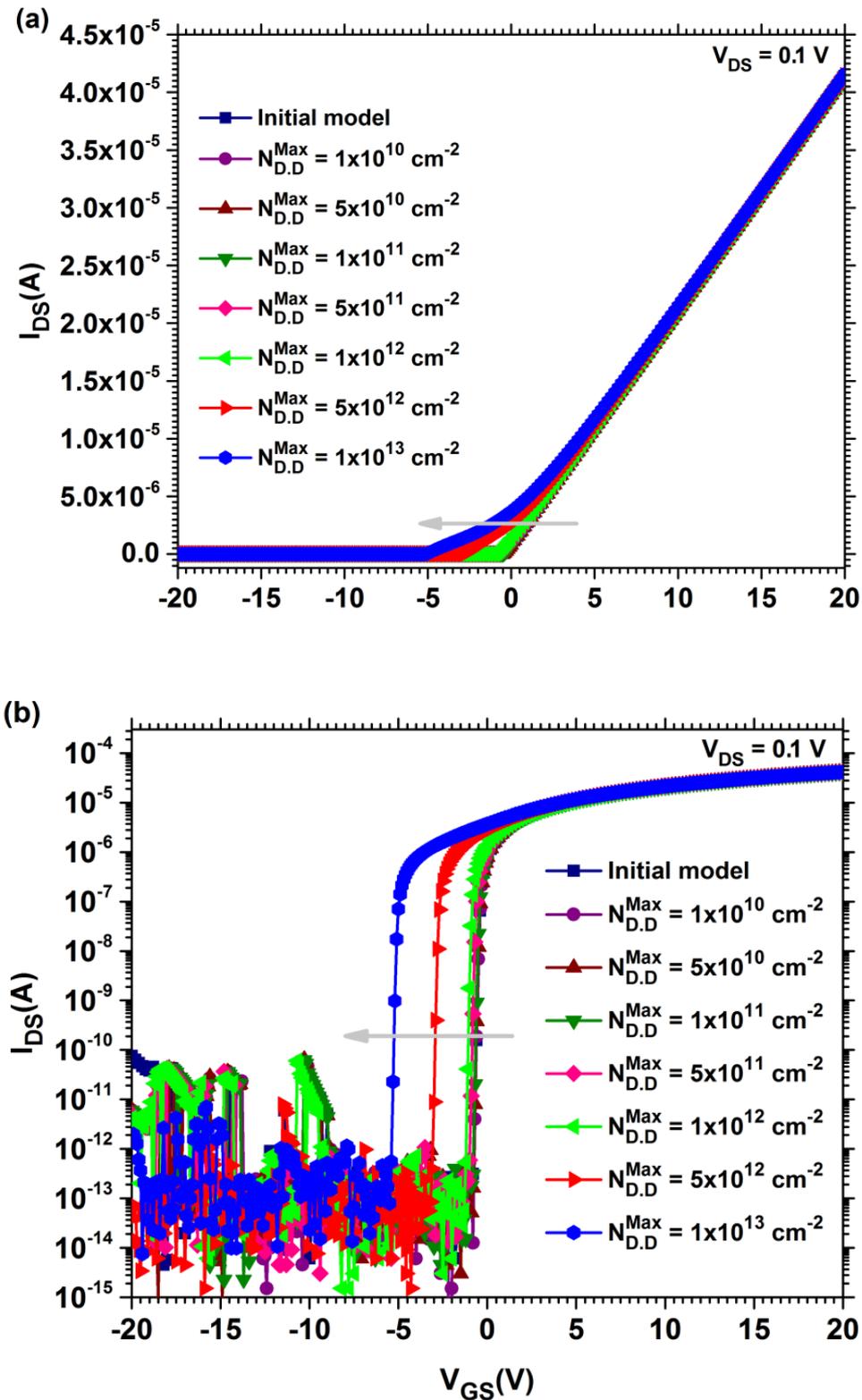
Figure III.16 Transfer ($I_{DS} - V_{GS}$) characteristics of the a-ITZO TFT with bi-layer (SiO$_2$/HfO$_2$) gate dielectric: (a) linear plot and (b) semi-logarithmic plot, for different SiO$_2$/HfO$_2$ interface state densities.

$N_{D.D}^{Max}(cm^{-2})$	$V_T(V)$	$SS(V/decade)$	$\mu_{FE}(cm^2V^{-1}s^{-1})$	$I_{on}(A)$	I_{on}/I_{off}	$V_{on}(V)$
Initial model	-0.45	6.42×10^{-2}	29.34	4.12×10^{-5}	4.67×10^{8}	-0.79
1×10^{10}	-0.46	6.65×10^{-2}	29.21	4.12×10^{-5}	4.67×10^{8}	-0.83
5×10^{10}	-0.47	6.68×10^{-2}	29.09	4.12×10^{-5}	4.67×10^{8}	-0.84
1×10^{11}	-0.49	6.69×10^{-2}	28.97	4.12×10^{-5}	4.67×10^{8}	-0.85
5×10^{11}	-0.57	6.71×10^{-2}	28.79	4.12×10^{-5}	4.67×10^{8}	-1.04
1×10^{12}	-0.72	6.75×10^{-2}	28.62	4.12×10^{-5}	4.67×10^{8}	-1.24
5×10^{12}	-1.07	6.82×10^{-2}	28.41	4.13×10^{-5}	4.68×10^{8}	-3.12
1×10^{13}	-1.87	6.93×10^{-2}	28.13	4.14×10^{-5}	4.69×10^{8}	-5.46

Table III.12 The extracted output parameters of the a-ITZO TFT with bi-layer (SiO$_2$/HfO$_2$) gate dielectric for different SiO$_2$/HfO$_2$ interface state densities.

From the obtained results the increase of the SiO$_2$/HfO$_2$ interface state density upper 10^{12} cm^{-2} induces a slight decrease in the mobility and namely a shift of the threshold voltage toward negative voltages. This means that the presence of this type of states with a considerable high density can destabilize the performance of the a-ITZO TFT based on bi-layer dielectric. But with good fabrication conditions, the interface state density should not exceed $10^{10} \sim 10^{11}$ cm^{-2} and it is expected that its effect on the TFT performance will be minor.

However, the effect of defects in SiO$_2$ and in the a-ITZO/SiO$_2$ interface that can result from different stresses during operation is more serious. These defects affect significantly the electrical properties of a-ITZO TFT, as shown in Figures III.17 and III.18, and then on the electrical properties as summarized in Tables III.12 and III.13 respectively.
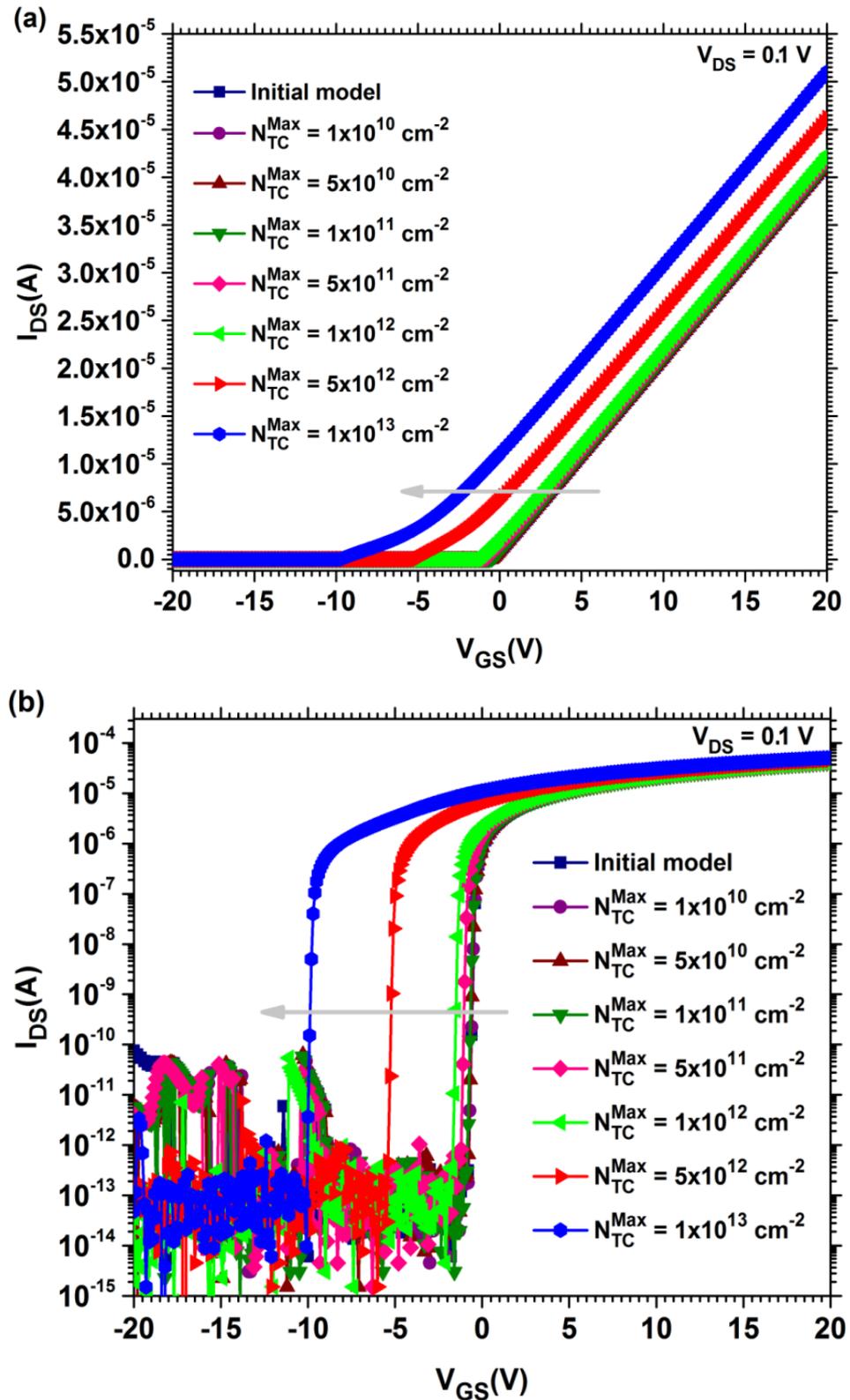
Figure III.17 Transfer characteristics of the a-ITZO TFT with bi-layer SiO_2/HfO_2 gate dielectrics: (a) linear plot and (b) semi-logarithmic plot, for different densities of trapped charge states in SiO_2.

$N_{TC}^{Max}(cm^{-2})$	$V_T(V)$	$SS(V/decade)$	$\mu_{FE}(cm^2V^{-1}s^{-1})$	$I_{on}(A)$	I_{on}/I_{off}	$V_{on}(V)$
Initial model	-0.45	6.42×10^{-2}	29.34	4.12×10^{-5}	4.67×10^8	-0.79
1×10^{10}	-0.47	6.67×10^{-2}	29.18	4.13×10^{-5}	4.68×10^8	-0.84
5×10^{10}	-0.50	6.71×10^{-2}	29.05	4.14×10^{-5}	4.69×10^8	-1.00
1×10^{11}	-0.54	6.75×10^{-2}	28.93	4.15×10^{-5}	4.70×10^8	-1.10
5×10^{11}	-0.62	6.80×10^{-2}	28.73	4.18×10^{-5}	4.74×10^8	-1.50
1×10^{12}	-0.85	6.86×10^{-2}	28.55	4.23×10^{-5}	4.79×10^8	-1.94
5×10^{12}	-2.84	6.93×10^{-2}	28.43	4.62×10^{-5}	5.23×10^8	-5.45
1×10^{13}	-5.30	7.05×10^{-2}	28.04	5.10×10^{-5}	5.78×10^8	-10.06

Table III.13 The extracted output parameters of the a-ITZO TFT with bi-layer (SiO_2/HfO_2) gate

dielectric for different densities of trapped charge states in SiO_2.
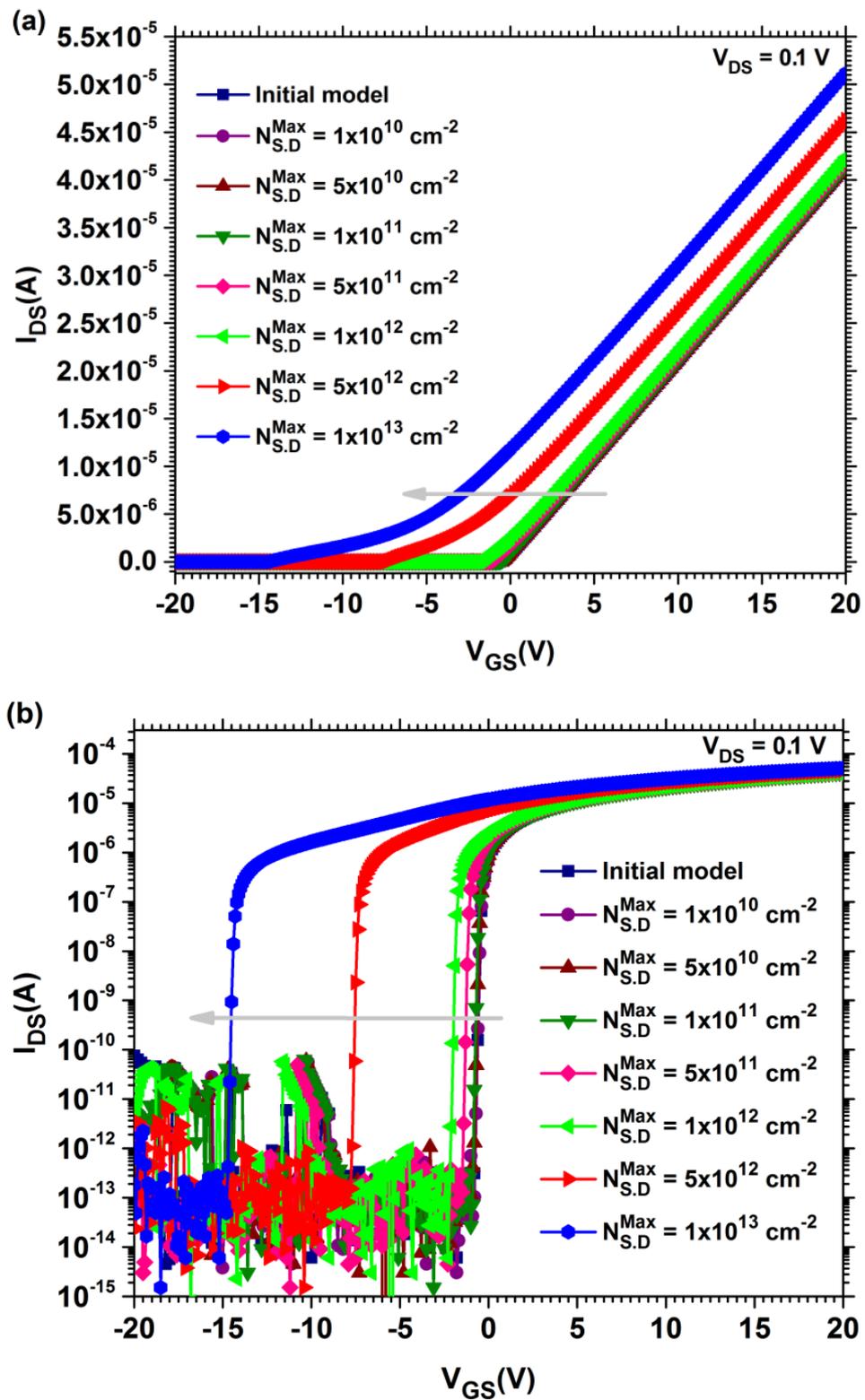
Figure III.18 Transfer characteristics of the a-ITZO TFT with bi-layer SiO_2/HfO_2 gate dielectrics: (a) linear plot and (b) semi-logarithmic plot, for different densities of the a-ITZO/SiO_2 interface states.

$N_{S.D}^{Max}(cm^{-2})$	$V_T(V)$	$SS(V/decade)$	$\mu_{FE}(cm^2V^{-1}s^{-1})$	$I_{on}(A)$	I_{on}/I_{off}	$V_{on}(V)$
Initial model	-0.45	6.42×10^{-2}	29.34	4.12×10^{-5}	4.67×10^8	-0.79
1×10^{10}	-0.48	6.69×10^{-2}	29.14	4.13×10^{-5}	4.68×10^8	-0.90
5×10^{10}	-0.54	6.72×10^{-2}	29.04	4.14×10^{-5}	4.69×10^8	-1.01
1×10^{11}	-0.59	6.75×10^{-2}	28.89	4.15×10^{-5}	4.70×10^8	-1.02
5×10^{11}	-0.98	6.82×10^{-2}	28.61	4.19×10^{-5}	4.75×10^8	-1.51
1×10^{12}	-1.55	6.89×10^{-2}	28.46	4.24×10^{-5}	4.81×10^8	-2.29
5×10^{12}	-3.09	6.98×10^{-2}	28.34	4.64×10^{-5}	5.26×10^8	-7.80
1×10^{13}	-5.69	7.20×10^{-2}	27.92	5.12×10^{-5}	5.80×10^8	-14.79

Table III.14 The extracted output parameters of the a-ITZO TFT with bi-layer (SiO$_2$/HfO$_2$) gate dielectric for different densities of the a-ITZO/SiO$_2$ interface states.

Therefore, it is recommended to use dielectrics that have good thermal stability in order to avoid the instability in the electrical properties of the device caused by trapped charges in the dielectric oxide and in the semiconductor/dielectric interface, resulting from stresses on the device during operation.

III.5 Effect of the interfacial dielectrics

In this section SiO$_2$ is replaced totally with an other dielectric material possessing higher properties which is Al$_2$O$_3$. It has a relatively high dielectric constant ($k = 9.5$), a very wide band gap ($E_g = 8.7\ eV$) close to the energy band gap of SiO$_2$, a good semiconductor/dielectric interface quality, a low density of semiconductor/dielectric interface traps, a good morphological properties and a good thermal stability [45-48].

Region	Parameter	Description	Value	Ref
SiO₂	$L(\mu m)/W(\mu m)/T(nm)$	Length/Width/Thickness	25/10/10 25/10/0	[9], Var
	$E_g(eV)$	Band gap	9	[9]
	$k_{\mathrm{SiO_2}}$	The relative permittivity	3.9	[9]
	$\chi(eV)$	Electronic affinity	0.9	[54]
	m_e^*/m_h^*	The relative effective mass for electron/hole	0.42/0.33	[55]
	$N_e^{Bulk}/N_h^{Bulk} (\times 10^{17} cm^{-3})$	The electron/hole trapping density in bulk dielectric layer	0.08/316	[56, 57]
Al₂O₃	$L(\mu m)/W(\mu m)/T(nm)$	Length/Width/Thickness	25/10/0 25/10/10	[9], Var
	$E_g(eV)$	Band gap	8.7	[22, 23]
	$k_{\mathrm{Al_2O_3}}$	The relative permittivity	9.5	[22, 23]
	$\chi(eV)$	Electronic affinity	1.7	[58]
	m_e^*/m_h^*	The relative effective mass for electron/hole	0.4/0.36	[59]
	$N_e^{Bulk}/N_h^{Bulk} (\times 10^{17} cm^{-3})$	The electron/hole trapping density in bulk dielectric layer	25/260	[60, 61]
HfO₂	$L(\mu m)/W(\mu m)/T(nm)$	Length/Width/Thickness	25/10/20 25/10/20	[9], Can
	$E_g(eV)$	Band gap	5.7	[30]
	$k_{\mathrm{HfO_2}}$	The relative permittivity	35	[30]
	$\chi(eV)$	Electronic affinity	2.25	[62]
	m_e^*/m_h^*	The relative effective mass for electron/hole	0.7/0.3	[63]
	$N_e^{Bulk}/N_h^{Bulk} (\times 10^{17} cm^{-3})$	The electron/hole trapping density in bulk dielectric layer	136/0.23	[64, 65]

Table III.15 The input parameters for the dielectrics used.

Figure III.19.a represents the evolution of the transfer characteristics in the linear plot, while Figure III.19.b represents the evolution of the transfer characteristics in the semi-logarithmic plot. Where we note that the TFT based on the bi-layer dielectric (Al₂O₃/HfO₂) with a physical thickness ($PT = 30 \, nm$) it can provide electrical characteristics higher than TFT device based on the bi-layer dielectric (SiO₂/HfO₂) for the same physical thickness. This is due to the fact that the dielectric constant of Al₂O₃ ($k = 9.5$) is higher than the dielectric constant of SiO₂ ($k = 3.9$). This leads, according to the relative approximation of Al₂O₃/HfO₂ k, to obtain a lower effective gate dielectric thickness, which is known as the equivalent oxide thickness ($EOT = 10 \, nm$). Thus, obtaining a high capacitance per unit area without the associated leakage effects (ALE). This will leads to raising the current and then the performance of the transistor. Because high-k dielectric materials using the relative approximation of low/high k can be physically thicker without being electrically thicker, which leads to the increase of the gate capacitance per unit area without ALE.
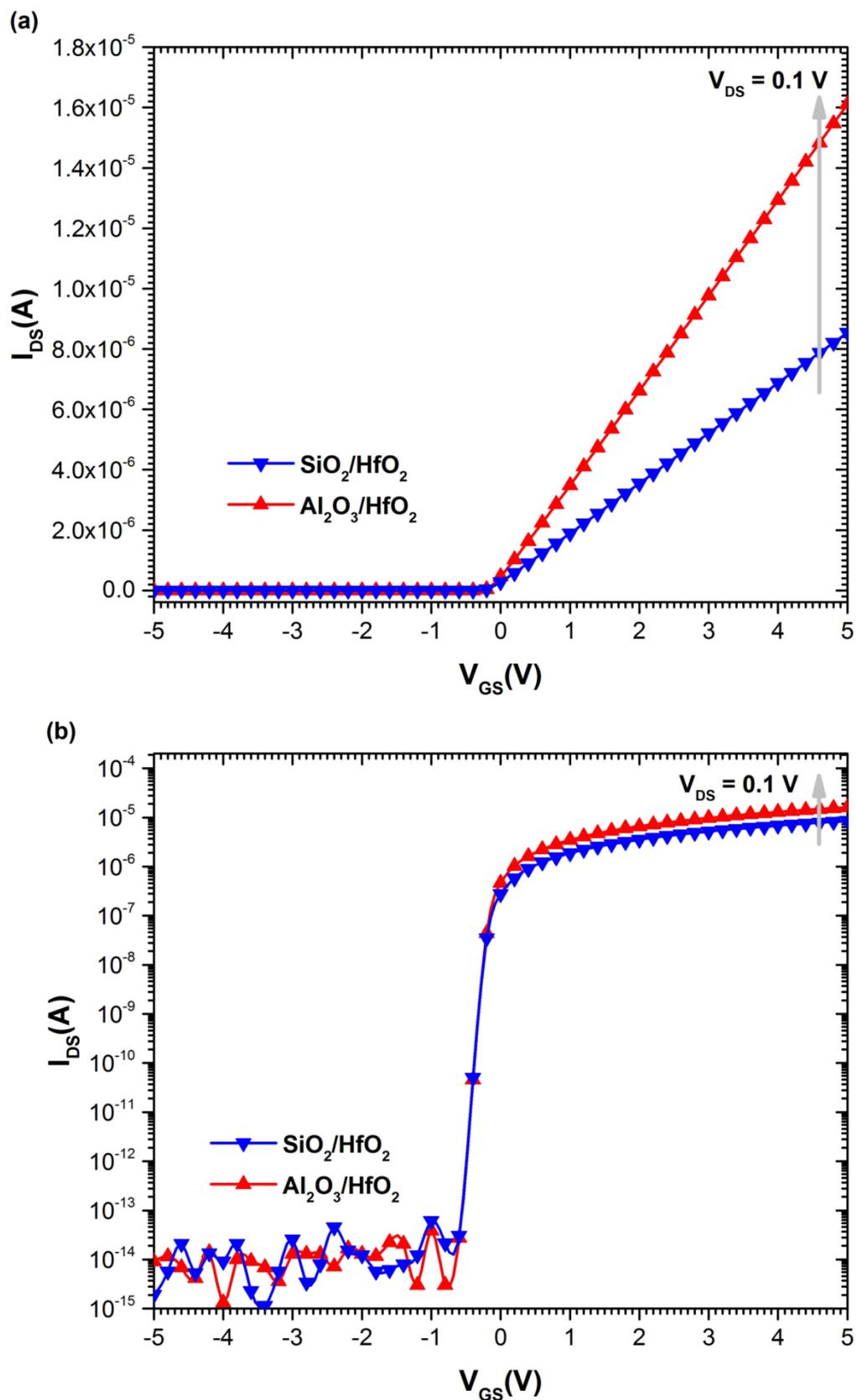
Figure III.19 The calculated of transfer ($I_{DS} - V_{GS}$) characteristics of the a-ITZO TFT depending on the different types of the interfacial dielectrics: (a) transfer characteristics in the linear plot and (b) transfer characteristics in the semi-logarithmic plot.

From the transcript characteristic curves in the linear plot (Figure III.19.a), we calculated the field effect mobility (μ_{FE}) while from the transfer characteristic curves in the semi-logarithmic plot (Figure III.19.b) we calculated each of I_{on} and I_{on}/I_{off} ratio.

All the results obtained for the previous parameters of the a-ITZO TFT devices, in addition to the equivalent oxide thickness (EOT) and the gate capacitance per unit area as well as the physical thickness of gate dielectric (PT) are presented in Table III.16.

dielectric	*PT* (nm)	*EOT* (nm)	$C_i(F/cm^2)$	$I_{on}(A)$	I_{on}/I_{off}	$\mu_{FE}(cm^2V^{-1}s^{-1})$
SiO$_2$/HfO$_2$	30	12.23	2.82×10^{-7}	8.54×10^{-6}	8.27×10^{8}	29.31
Al$_2$O$_3$/HfO$_2$	30	6.33	5.45×10^{-7}	1.61×10^{-5}	1.56×10^{9}	24.11

Table III.16 The variations of the extracted parameters: PT, EOT, C_i, I_{on}, I_{on}/I_{off} and μ_{FE}.

Our results show that TFT based on the bi-layer dielectric (Al$_2$O$_3$/HfO$_2$) with a physical thickness ($PT = 30\ nm$) can provide electrical properties better than properties provided by the TFT device based on the bi-layer dielectric (SiO$_2$/HfO$_2$) for the same physical thickness where:

Equivalent oxide thickness decreases from the value $EOT = 12.23\ nm$ in the TFT based on the bi-layer dielectric (SiO$_2$/HfO$_2$) with a physical thickness ($PT = 30\ nm$) to the value $EOT = 6.33\ nm$ in the TFT based on the bi-layer dielectric (Al$_2$O$_3$/HfO$_2$) for the same physical thickness. This is due to the decrease of the low/high$k$ ratio because of the increase of k (because the dielectric constant of the interfacial dielectric layer increases from the value $k = 3.9$ for SiO$_2$ to the value $k = 9.5$ for Al$_2$O$_3$) [66].

In addition, we note an increase in the capacitance per unit area from the value $C_i = 2.82 \times 10^{-7} F/cm^2$ to $C_i = 5.45 \times 10^{-7} F/cm^2$. This is due to the decrease in the effective thickness of the gate dielectric, which is known as the electrical thickness of the gate dielectric and also EOT because the TFT based on the bi-layer dielectric (Al$_2$O$_3$/HfO$_2$) with a physical thickness ($PT = 30\ nm$) has an equivalent oxide thickness ($EOT = 6.33\ nm$) smaller than EOT

of the TFT based on the bi-layer dielectric (SiO₂/HfO₂) ($EOT = 12.23 \, nm$)   for the same physical thickness [67].

Also, The current I_{on} and the I_{on}/I_{off} ratio, both increase from the values $I_{on} = 8.54 \times 10^{-6}A$ and $I_{on}/I_{off} = 8.27 \times 10^{8}$ to $I_{on} = 1.61 \times 10^{-5}A$ and $I_{on}/I_{off} = 1.56 \times 10^{9}$, respectively. This is due to the increase in the capacitance per unit area because of the decrease in EOT, which leads to the raising of the current (drain current) and then increasing both I_{on} and I_{on}/I_{off} ratio. The increase in this ratio leads to a higher switching speed (fast reaction) and then higher performance of the transistor [30, 68].

However, the field effect mobility decreases from the value $\mu_{FE} = 29.31 \, cm^2V^{-1}s^{-1}$ to $\mu_{FE} = 24.11 \, cm^2V^{-1}s^{-1}$. This is due to the increase in the gate capacitance per unit area [69].

III.6 Effect of the leakage current

It is known that most of the TFT devices based on dielectrics with high thicknesses display very small values to the charge leakage through the gate dielectric. However, the current leakage may be noticeable when a relatively high electrical voltage is applied to the gate. This leakage in current through the gate dielectric is due to many different leakage mechanisms, which may all contribute to leakage of current at the same time. This can affect the performance of any TFT device, especially its reliability, which are very important for the applications of dielectrics-based devices in combination with semiconductors such as TFT. Because a study of different leakage mechanisms through the gate dielectric is of great importance to the success of any TFT device. Therefore, the leakage current must be below a certain level to meet the specific reliability standards under normal operation of the device. Most leakage mechanisms that can contribute to the leakage of current through the gate dielectric are shown in Figure III.20.

(a)
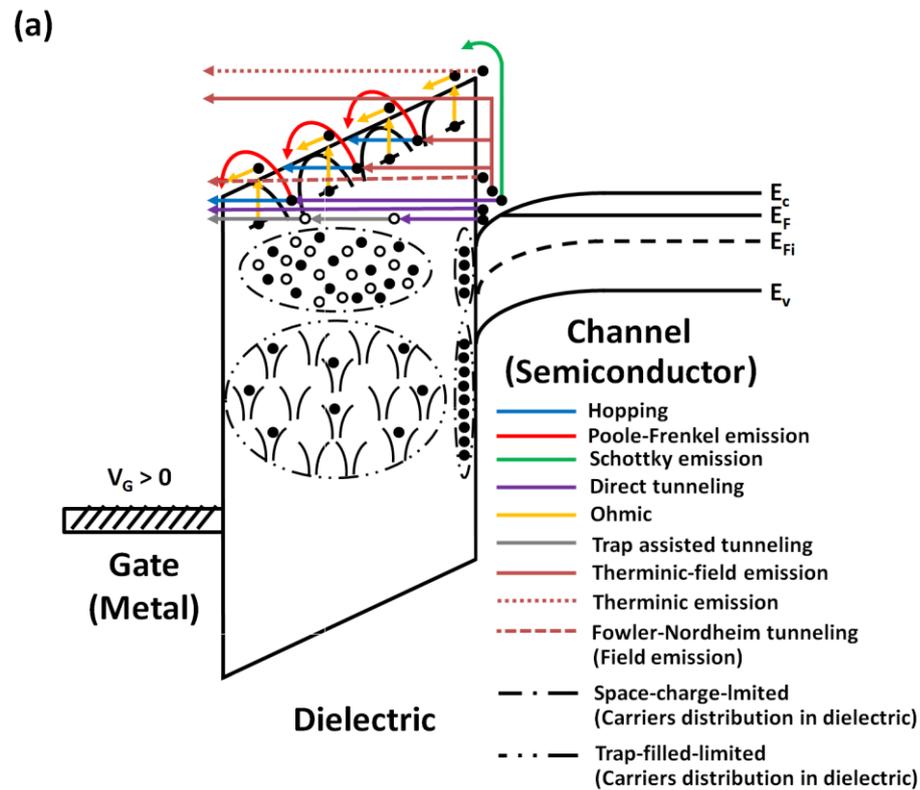
Figure III.20 The energy band diagram of the semiconductor/dielectric interface in TFT depending on the type of gate bias with most leakage mechanisms that can contribute to the charge leakage through the gate dielectric.

Figure III.21 represents the energy band diagram of the semiconductor/bi-layer dielectric oxide interface in TFT devices and the different band offsets where we note that there is a clear contrast between the band offsets. This variation can clearly affect the leakage value between the two devices, which varies depending on the leakage mechanism.
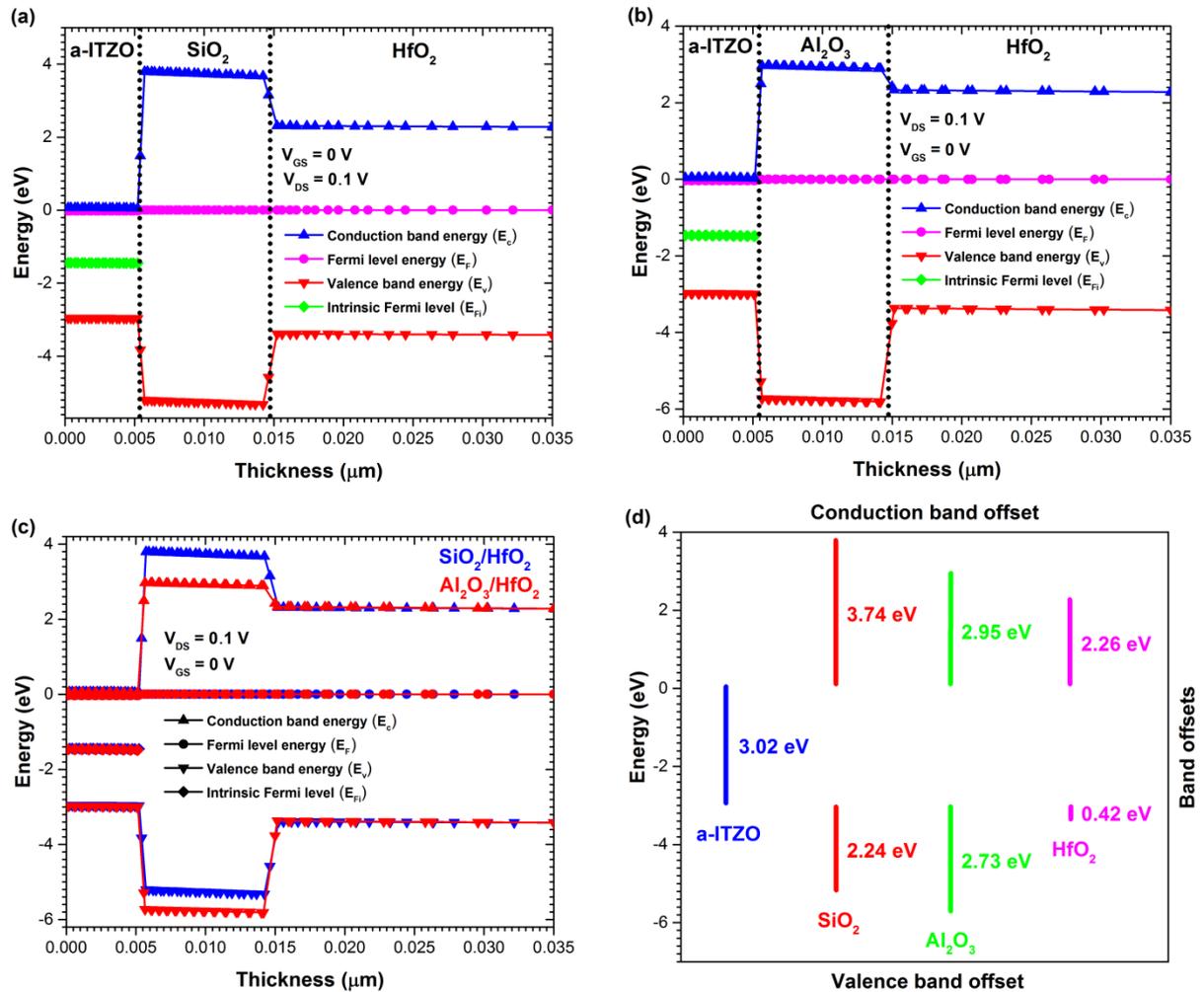
Figure III.21 The energy band diagram of the semiconductor/bi-layer dielectric oxide interface in a-ITZO TFTs and the different band offsets where (a) and (b) show the energy band diagrams of a-ITZO/SiO₂/HfO₂ and a-ITZO/Al₂O₃/HfO₂ interfaces, respectively, and (c) shows comparative diagram of the energy bands while (d) shows the different band offsets in a-ITZO TFTs.

Figure III.22 represents the evolution of the leakage current density in the linear and logarithmic plots depending on the quality of the interfacial dielectric layer. This evolution shows that a-ITZO TFT device based on Al₂O₃/HfO₂ gives a leakage current density higher than the density provided by a-ITZO TFT based on SiO₂/HfO₂, which means that there is a difference in reliability between the two devices.
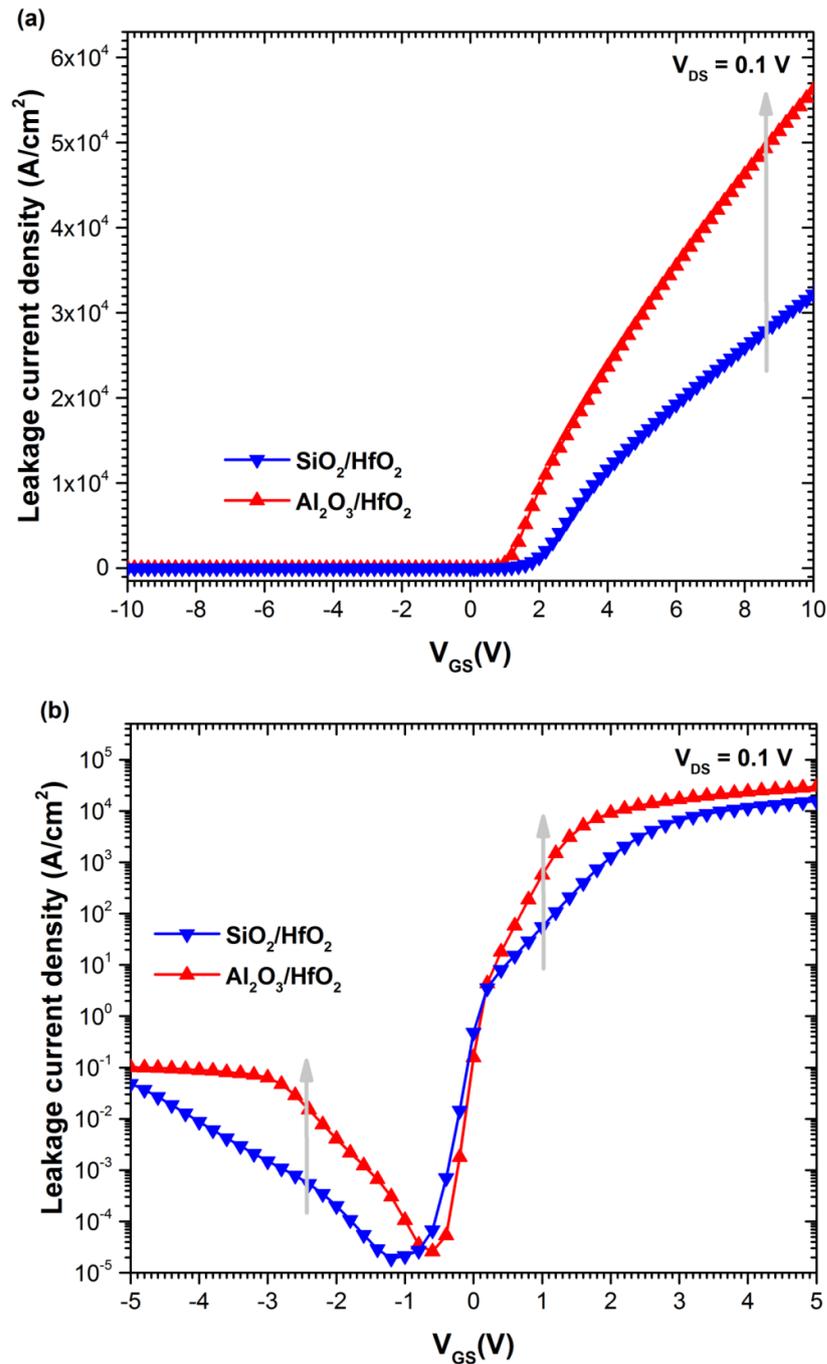
Figure III.22 The calculated of the leakage current density of the a-ITZO TFTs depending on the different types of the interfacial dielectrics: (a) the evolutions of the leakage current density in the linear plot while (b) the evolutions of the leakage current density in the semi-logarithmic plot.

Although there is a clear disparity in the leakage value between the two devices, this does not mean that it has a significant impact on the reliability of the devices. The leakage

mechanisms that contribute to the charge leakage through the gate dielectric are shown in Figure III.23.
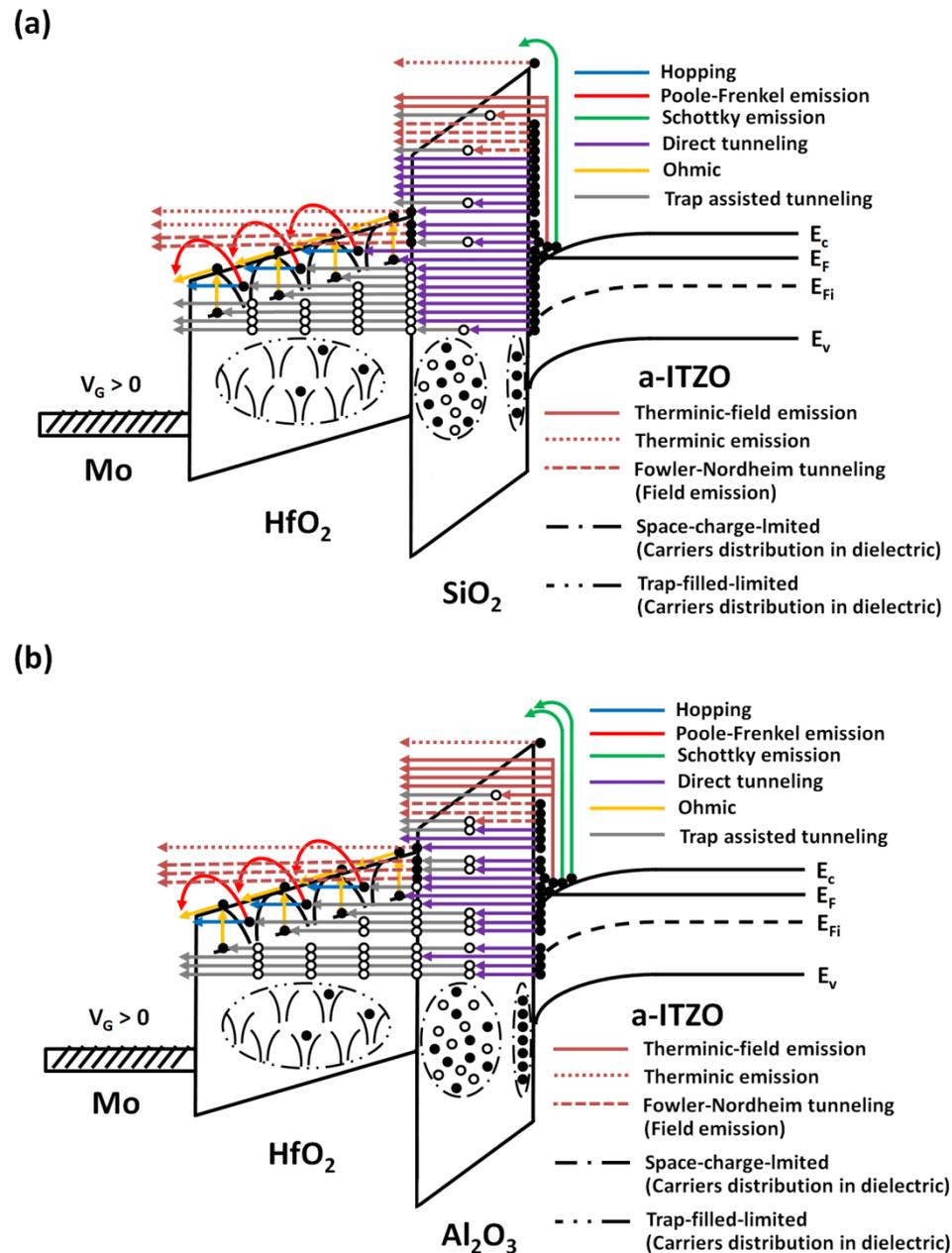
Figure III.23 The energy band diagram of the semiconductor/dielectric interface in TFTs with different leakage mechanisms that contribute to the charge leakage through the gate dielectric depending on the different types of the interfacial dielectrics: (a) with an interfacial low-k SiO_2 and (b) with an interfacial high-k Al_2O_3.

In order to investigate the impact of this leakage on reliability, we performed a comparative study of the effect of the leakage current on the performance of the devices to determine whether it has a significant impact on reliability.

Figure III.24 represents the evolution of the transfer characteristics of a-ITZO TFT devices with the associated leakage effects (ALE) along with the transfer characteristics of a-ITZO TFT devices without ALE depending on the quality of the interfacial dielectric material.
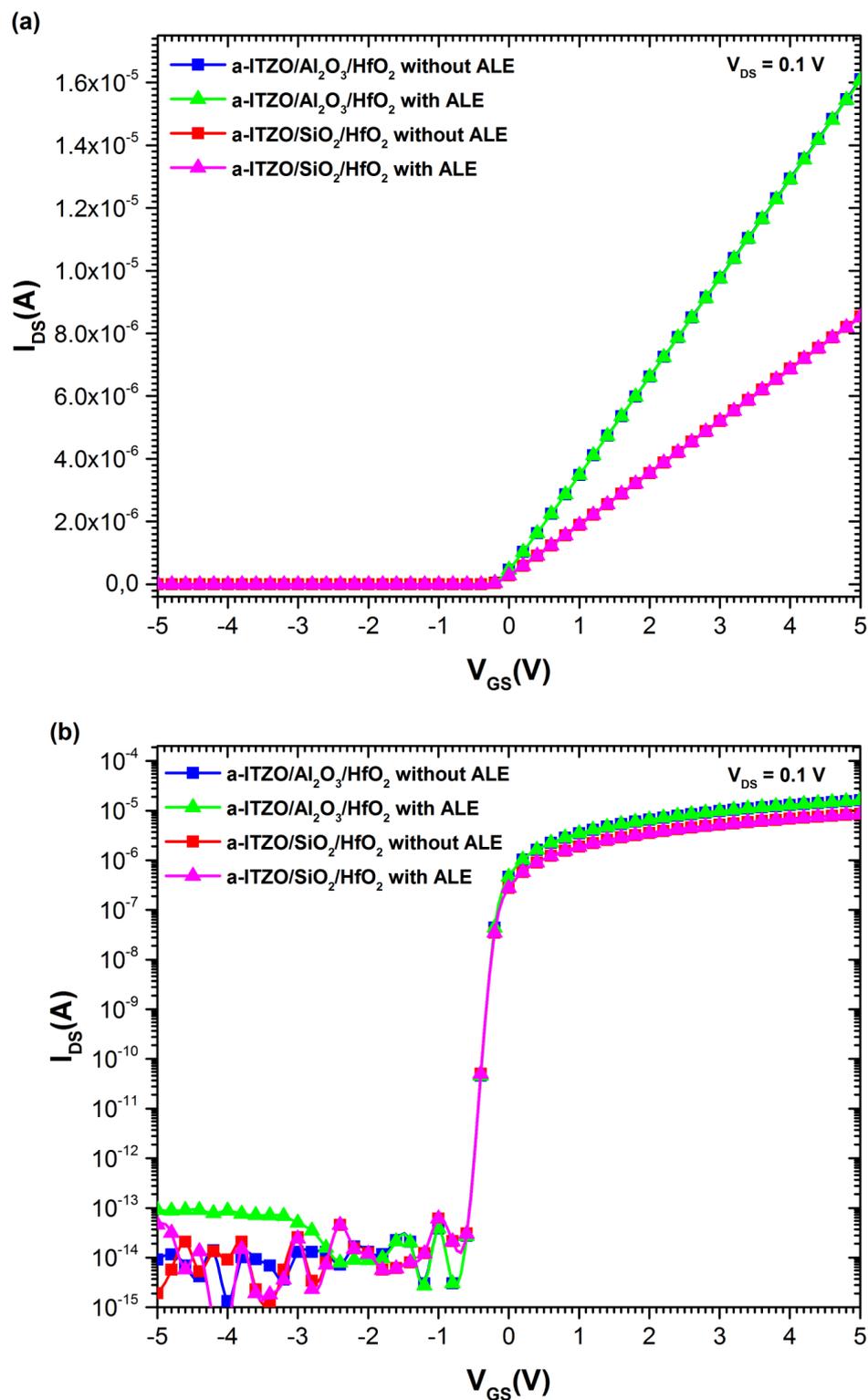
(a)

(b)

Figure III.24 The calculated of transfer ($I_{DS} - V_{GS}$) characteristics of the a-ITZO TFTs

with/without ALE depending on the different types of the interfacial dielectrics: (a) transfer

characteristics in the linear plot and (b) transfer characteristics in the semi-logarithmic plot.

Although there is a difference in the value of leakage between the two devices, its effect is very poor on the performance of the device and its reliability, especially for low gate tensions.

III.6 Conclusion

In the TFT based on bi-layer, without neglecting the fundamental role of the interfacial low-k dielectric layer (SiO$_2$) between the channel and the high-k dielectric, which has some beneficial qualities with regard to the carrier mobility in the transistor channel, through replacing the interfacial low-k dielectric oxide layer such as SiO$_2$ between the high-mobility channel and the high-k dielectric oxide layer by an interfacial high-k dielectric such as Al$_2$O$_3$, we can continue to reduce the effective dielectric oxide thickness, which is referred as EOT, while at the same time using a physically thicker dielectric with almost maintaining low density of the interface and oxide traps. Thus raising transistor performance with high reliability through increasing the capacitance per unit area, raising the drain current, reducing or preventing the current leakage and reducing the energy consumption with almost maintaining low trapping rate of the carriers in the oxide and interface.

However, we can continue to raise the transistor performance to higher values for the same physical thickness by replacing the HfO$_2$ layer with a dielectric material having a higher dielectric constant (higher than 35) and a wide energy band gap as well as a good thermal stability. Recently, the most prominent among these materials are: Sr$_2$TiO$_4$ ($E_g = 5.2\ eV$, $k = 50$), SrZrO$_3$ ($E_g = 5.5\ eV$, $k = 180$) and TiO$_2$ ($E_g = 3.5\ eV$, $k = 170$). And the hope remains for the next generation TFT is to introduce dielectrics with many attractive features such as a higher dielectric constant, a wider energy band gap and a good interface quality as well as good thermal stability, which are indispensable in the technology of the devices based on dielectrics in combination with semiconductors such as TFT in the future.

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GENERAL CONCLUSION

In this work we have already found and confirmed that the correct selection of the dielectric material is very important in determining the performance/reliability of any device based on semiconductors in combination with dielectrics such as TFT where:

The performance of any TFT device is increased by:

- Increasing the dielectric constant of the dielectric material, which leads to the reduction of the electric thickness of the gate dielectric or the so-called EOT, the increasing the gate capacitance per unit area and then the current (drain current).

- Minimize the defects of the semiconductor/dielectric interface and the dielectric oxide by adding an interfacial low-k dielectric layer between the a-ITZO channel and the high-k dielectric layer, having very wide band gap and good morphological characteristics such as SiO_2. Or replacing it with another dielectric layer having high-k and other good properties similar to those owned by SiO_2 as very wide band gap, good quality of the interface and oxide (the density of oxide traps and low interface), and a good thermal stability, such as Al_2O_3. This leading to the reduction of the trapping rate of free carriers in the interface and oxide and then to increase current. Without neglecting the basic role of the SiO_2 layer in the raising the mobility of free carriers at the transistor channel.

The reliability of the device (TFT) is improved by:

- Increase the physical thickness of the gate dielectric to a certain extent to allow for the reduction or prevention of the direct tunneling current leakage (preventing the leakage of the carriers from the gate to the a-ITZO-based channel and vice versa through the gate dielectric) and thereby reducing the power consumption as well as the decrease in temperature.

- Increase the band gap energy of the dielectric material as it is known that the wide energy band gap can prevent the current leakage through gate dielectric with a mechanism different from the thickness mechanism that we talked about.

Currently, the dielectric material that can achieve all these good specifications; high performance, high reliability and good stability at the same time is Al_2O_3.

However, we can continue to raise the transistor performance to higher values for the same physical thickness by replacing the bottom layer of the high-k HfO$_2$ with a dielectric material having a higher dielectric constant (higher than 35) and a wide energy band gap as well as a good thermal stability. Recently, the most prominent among these materials are: Sr$_2$TiO$_4$ ($E_g = 5.2\ eV, k = 50$), SrZrO$_3$ ($E_g = 5.5\ eV, k = 180$) and TiO$_2$ ($E_g = 3.5\ eV, k = 170$).

The hope remains for the next generation a-ITZO TFT is to introduce the double-layer dielectrics with a relatively large physical thickness that improves the reliability of TFT and a very small electric thickness that raises the performance of TFT to more higher values with good stability of electrical properties which are indispensable in the technology of the devices based on dielectrics in combination with semiconductors such as TFT in the future.