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Modelling of semiconductor diodes made of high defect concentration, irradiated, high resistivity and semi-insulating material: The capacitance–voltage characteristics

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Abstract

Full modelling is reported of the capacitance of a long PIN semiconductor diode with a high concentration of generation–recombination (g–r) centres and different concentrations of deep traps. There are considerable differences from the textbook results given for normal lifetime diodes which have low concentrations of g–r centres. For a low density of g–r centres, the capacitance is the usual value. That is it decreases as $V^{-1/2}$ with increasing reverse bias while it increases rapidly with increasing forward bias. For high density of g–r centres and in reverse bias a departure from this voltage dependence is observed, while in forward bias a negative capacitance appears. This agrees with experiment. From these results we present a physical understanding of the processes involved. There are specific applications of these results to radiation damaged devices, lifetime killed diodes and devices made from high resistance and semi-insulating materials, especially in the interpretation of the C–V curves to evaluate the fixed space charge density.

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Keywords: Semi-insulating; Semiconductor; Diode; Radiation damage; Modelling

1. Introduction

There are many materials in current use, such as semi-insulating, lifetime killed or highly irradiated semiconductors, which show relaxation semiconductor behaviour [1,2]. This may not be immediately apparent since some of the properties often do not seem very unusual and can be analysed using normal lifetime semiconductor theory with apparently reasonable results. This is especially likely since the materials are often poorly characterised and highly defected so that there is not a clear expectation for what is reasonable. However the normal analysis is not appropriate and may give incorrect values for the material properties such as the effective doping and trap density. Thus a PIN diode made from relaxation material shows Ohmic characteristics which would suggest, incorrectly, that there was no blocking contact or internal field. A very apparent and unusual property is the negative capacitance shown experimentally by relaxation diodes in forward bias [3,4].

The necessary conditions for a relaxation material are that it has a high resistivity; that is it is a nearly intrinsic or compensated semiconductor or semi-insulator, and that it has a very high density of generation–recombination (g–r) centres. It is a relaxation rather than a lifetime semiconductor because any disturbance of the equilibrium space charge is neutralised by electron–hole pair generation rather than by the inflow of free carriers.

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Most previous calculations on relaxation materials have been carried out as a demonstration of the relaxation theory, while others have been done to show that experimental observations are consistent with a specific model. The present work is designed as a practical and helpful analysis to enable the experimenter to understand the internal state of his sample and what its likely impurity content may be. Here we describe the main features which are observed experimentally, model them using a typical diode structure as an example, explain the physical processes occurring and discuss the implications and applications. The aim is to explain the physical reasons underlying the experimental results and the effects of different types of defects.

We have carried out similar calculations to illustrate the I–V characteristics and the internal electric field distribution in relaxation diodes and a full background description is given there [5,6].

Experiments on high resistivity and defected material which may be expected to show relaxation-like properties show a variety of features. These samples are not easy to study quantitatively since the material contains both g–r centres and a variety of traps at high density. The capacitance in forward bias is not often studied because instruments may not be able to record the data and the sample naturally has a low Q in forward, and even in reverse, bias. Semi-insulating GaAs and high resistivity silicon have been studied by the Lancaster group for both native and irradiated samples [4,6–8]. The radiation levels are those likely to be experienced by detectors in current accelerators. The significant features of the capacitance are; a departure from the usual $V^{-1/2}$ dependence of the capacitance in reverse bias, but low, or negative, capacitance in forward bias with an associated reduction in capacitance at small negative bias.

2. Calculation of the capacitance

The modelling was carried out using the package Kurata [9]. The details of the numerical calculation are given in our previous publications [5,6].

In a lifetime semiconductor diode using the depletion approximation the incremental capacitance is simply the change in charge each side of the depletion region so that it appears as a parallel plate capacitance. Experimentally one measures the charge inflow (the integrated current) after the application of a voltage increment or the out of phase current responding to an applied sine wave voltage. In our case the internal charge distribution is complex with static and mobile charges and there are redistributions internally so that this simple approach to the calculation is inappropriate. Here we use an energy method in which the lumped circuit capacitive energy $1/2CV^2$ is equated to the integral of the energy density, given by E^2, through the sample [10]. Thus,

$$C_{\mathrm{W}} = \frac{1}{|\psi|}\frac{\mathrm{d}G}{\mathrm{d}\psi} \tag{1}$$

where ψ is the potential difference defined as

$$\psi = V_{\mathrm{bi}} - V$$

and G the potential energy given by

$$G = \frac{\varepsilon_{\mathrm{r}}\varepsilon_0}{2}\int_0^l E(x)^2\mathrm{d}x \tag{2}$$

where $E(x)$ is the distribution of the electric field, ε_0, permittivity in vacuum, ε_{r}, relative permittivity and l length of the sample.

This is the static (low frequency limit), incremental, junction capacitance, and not necessarily the measured C since there are parasitic series and device (parallel) resistances and trap time constants. The results calculated for the carrier densities, n, p and for E, etc. can be used for the explanation of the physical processes involved.

3. The sample

The analysis was carried out for a silicon $P^+N^-N^+$ structure with $1\times10^{11}\,\mathrm{cm}^{-3}$ shallow donors (N^-). The contacts are P^+ ($N_{\mathrm{A}} = 10^{15}\ \mathrm{cm}^{-3}$) between 0 and 30.6 μm and N^+ ($N_{\mathrm{D}} = 10^{15}\ \mathrm{cm}^{-3}$) between 319.6 and 350 μm. The sample is long in the sense that the excess charge distribution is mostly in short lengths near the ends.

The intrinsic carrier concentration at room temperature, n_{i}, is $1.45\times10^{10}\,\mathrm{cm}^{-3}$. The dielectric relaxation time, τ_{D}, at room temperature is about 10^{-9} s so the relaxation criterion is reached for a value of the g–r centre density of $N_{\mathrm{GR}} \sim 10^{15}\,\mathrm{cm}^{-3}$ using $\tau^{-1} = \sigma v_{\mathrm{th}} N_{\mathrm{GR}}$, where v_{th} is the thermal carrier velocity, and a typical value of $10^{-14}\,\mathrm{cm}^2$ is used for the cross-section, σ [11,12], and the centres are at mid gap.

We consider the cases with different types of added traps as the density of generation–recombination (g–r) centres at mid gap is increased from 10^7 to $10^{18}\,\mathrm{cm}^{-3}$. In this model we consider these g–r centres to have no net charge. This gives a very simple separation between the effect of traps, which are charged when unoccupied, and g–r centres. Not much is known about these centres. In the calculations we have simulated a charge on the g–r centres by adding traps near mid gap and there have been no significant differences in the results from those described. This will be seen by the results presented which show little change in the average space charge when deep traps are added. The calculations have also been made for the sample with the addition of deep acceptors (DA) at $E_{\mathrm{T}} = E_{\mathrm{C}} - 0.4$ eV. These traps interact most with their own band. Also for less-deep acceptors (LDA) at $E_{\mathrm{C}} - 0.72$ eV. The energy gap in silicon is 1.12 eV. The distinction between deep and less-deep traps is whether they are, or are not, on the same side of mid gap as the shallow trap of the same type. This is significant because the Fermi energy in a relaxation material is near mid gap. The addition of deep and less deep donors has also been studied.

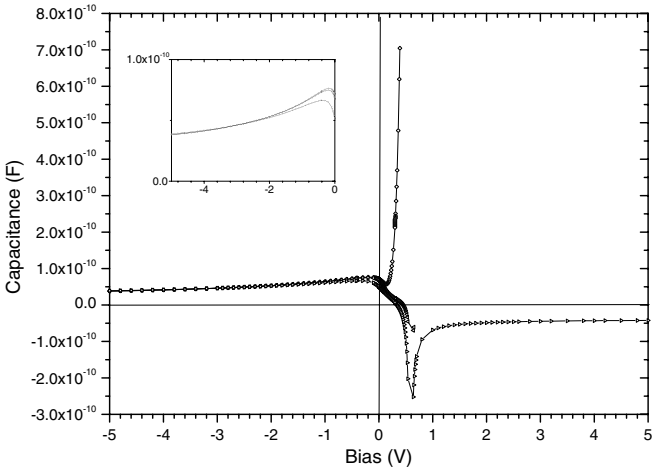

Fig. 1. Calculated C–V characteristics for a PNN junction with no traps for N_{GR} increasing 10^{14}, 10^{15}, 10^{16} cm^{-3}. The curves for the lowest fluence, and those smaller, are approximately superimposed and always positive. The insert is a more detailed reverse curve from 0 to −4.5 V to show the departure from the $V^{-1/2}$ dependence of the capacitance for the same values of N_{GR}.

4. Results and discussion

We will first consider the voltage dependence of the capacitance for the case of no traps and various N_{GR} (Fig. 1). It can be seen that the magnitude at large negative or positive bias is constant at the geometrical capacitance. The reverse bias case is as expected for low N_{GR} and we will take 10^{11} cm^{-3} as a standard value for low N_{GR}. The negative capacitance appears for N_{GR} above about 10^{14} cm^{-3}. There is little change below 10^{14} cm^{-3} and above 10^{16} cm^{-3}. We will take 10^{17} cm^{-3} as our standard value for high N_{GR}.

There is a small decrease of the capacitance in the lifetime case (low N_{GR}) at small forward bias before it increases again. This is due to the spill over of free holes from the P^+ contact to the much less doped n-type central region. When a forward voltage is applied there is a competition between the decreasing space charge density due to the depletion of electrons in the N region and the increasing injected holes from the contact. This small decrease does not exist for a symmetrical junction.

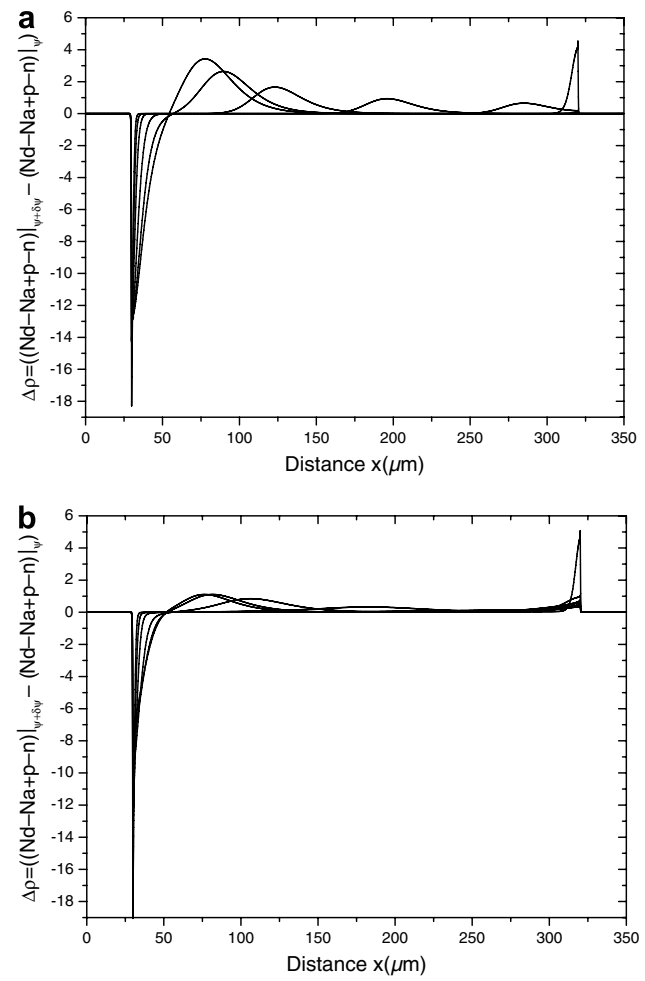

Fig. 2. Delta space charge for reverse bias: (a) low N_{GR}, (b) high N_{GR}. Voltages 0, 0.1, 0.5, 2.0, 5.0, 10.0 V. The positive peaks move to larger distance with increasing voltage.

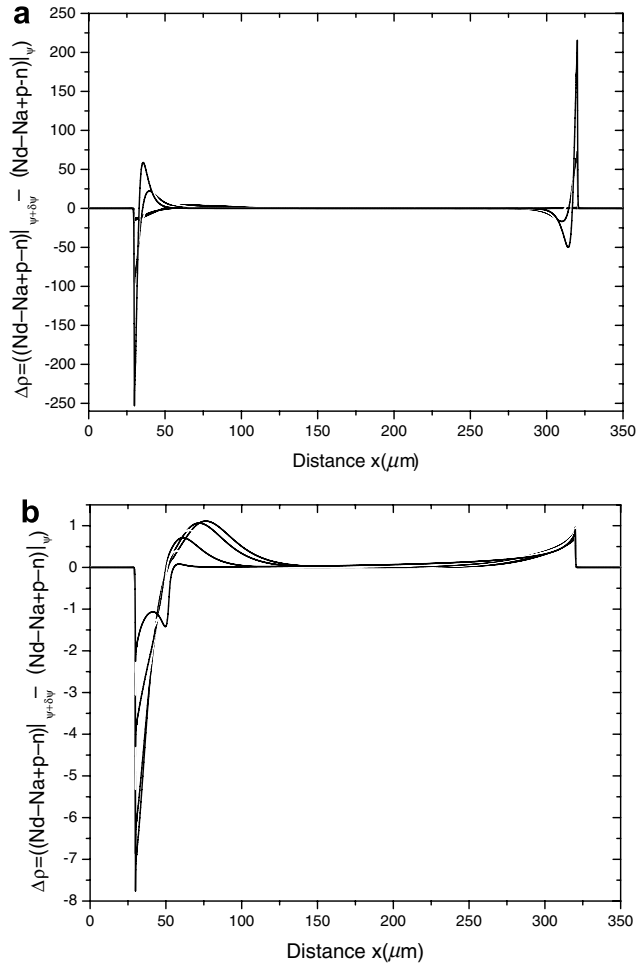

Fig. 3. Delta space charge for forward bias: (a) low N_{GR}, (b) high N_{GR}. Voltages 0, 0.1, 0.26, 0.30 V. The peaks become bigger (a) and smaller (b) monotonically with increasing voltage. Note the differences in scale between (a) and (b) and with Fig. 2.

In order to understand the results we will initially restrict our discussion to the no trap case. The behaviour of delta space charge, the change in the space charge under an increment of voltage of 0.1 V, with low and high N_{GR} in reverse bias is shown in Fig. 2 and in forward bias in Fig. 3.

The reverse bias case for low N_{GR} shows the charge as a dipole, the capacitance, at the edge of the depletion region and near the junction at 30.6 μm. The depletion width increases and reaches full depletion at about 5 V. The negative charge is at the junction. When the central region is fully depleted more of the charge appears at the far contact. Analysis of the components of the space charge suggest that it is due dominantly to free holes to the right of the zero at about 50 μm and ionised acceptors to the right. This is due to the fact that the junction is highly asymmetrical The high N_{GR} case is similar but less defined.

In forward bias and low N_{GR} the distribution is very different with a charge dipole at each contact which increases in amplitude with increasing bias. At large N_{GR} the far contact charge distribution is just due to holes and changes little with bias but the distribution at the junction changes from a dipole to a double peak distribution. The double peak appears at biases higher than the (negative) minimum of the capacitance.

The effect of adding traps to the relaxation material has been studied and can be described generically. There is negligible effect on the C–V results of adding a large (much greater than the shallow donor concentration) concentration of either deep acceptors (DA) or deep donors (DD). This is expected since the quasi-Fermi levels are forced from near their conduction band to near mid gap over much of the relaxation sample and hence the DD and DA traps do not change occupancy. An example of a deep acceptor at $E_T - E_V = 0.72$ eV is shown in Fig. 4 for low (a) and high (b) density of g–r centres.

Adding less deep traps is different. As the quasi Fermi energies move towards mid gap, the less deep donors and acceptors can become ionised and contribute to the static space charge and hence the effective space charge density,

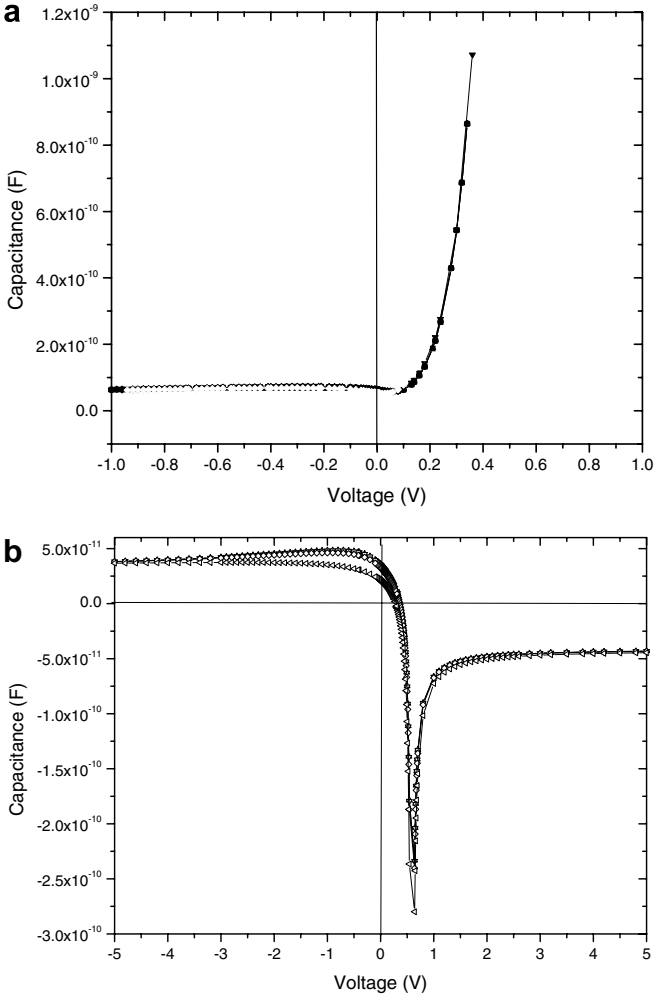

Fig. 4. Calculated C–V characteristics for a PNN junction in the presence of a deep acceptor at $E_T - E_V = 0.72$ eV with N_{TA} increasing from 10^{10}, 10^{11}, 10^{12}, 10^{13} cm^{-3} for (a) low 10^{11} cm^{-3} and (b) high 10^{17} cm^{-3} density of generation–recombination centre.

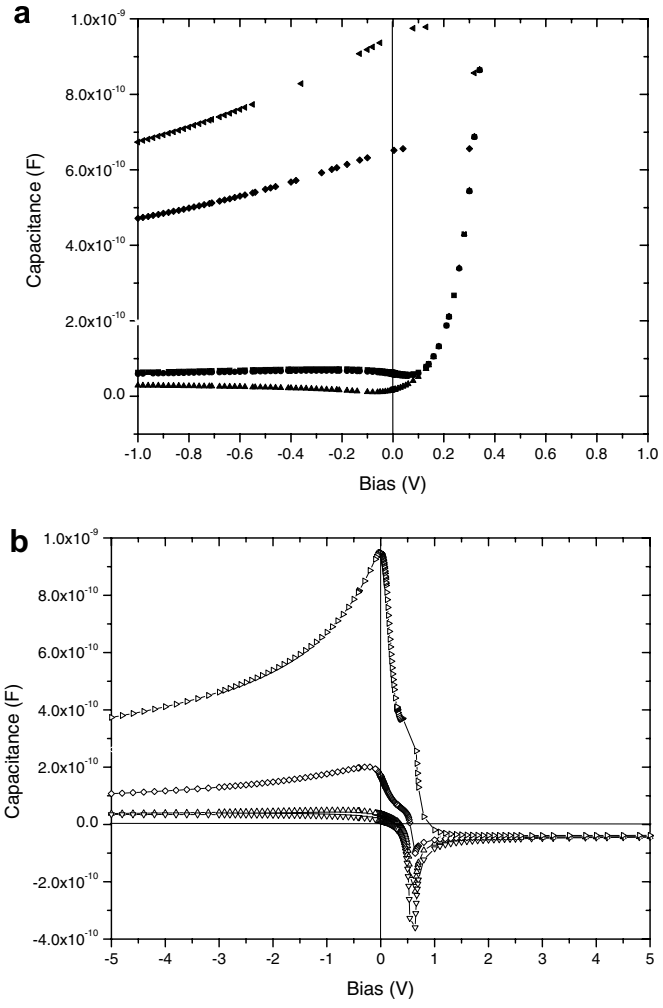

Fig. 5. Calculated C–V characteristics for a PNN junction in the presence of a less deep acceptor at $E_T - E_V = 0.40$ eV with N_{TA} increasing from 10^{10}, 10^{11}, 10^{12}, 10^{13} cm^{-3} for (a) low 10^{11} cm^{-3} and (b) high 10^{17} cm^{-3} density of generation–recombination centre. In each case the capacitance in negative bias initially decreases but then increases as N_{TA} increases through 10^{11} cm^{-3}.

N_{eff}. A large trap concentration removes the negative capacitance and moves the maximum capacitance to small forward bias values. The less deep acceptors compensate the shallow donors so that N_{eff} goes through a minimum as the concentration increases. An example of a deep acceptor at $E_T - E_V = 0.40$ eV is shown in Fig. 5 for low (a) and high (b) density of g–r centres.

5. Conclusions

Modelling of a long PIN diode has shown several capacitive effects which are seen experimentally in material with a high concentration of g–r centres. Reduced and negative capacitance is found in forward bias. A maximum is found at low reverse voltages since the capacitance is 'pulled down' by the negative capacitance. This has an effect on the results obtained for irradiated devices by the $V^{-1/2}$ analysis used to find the trap density and effective trap density, N_{eff}. The capacitive effects may be the best way to distinguish such a diode from an Ohmic resistor. A more detailed description on how this analysis should be modified will be described in a later publication [13].

More complete tutorial descriptions of the I–V and C–V characteristics of irradiated and defected semiconductor diodes are available from the corresponding author.

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