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MODELING THE TRANSIENT RESPONSE OF CHANNEL–SUBSTRATE INTERFACE TRAPS TO GATE VOLTAGE STEPS IN GaAs FETs

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Abstract—The transient response of a hole trap, located in the substrate (buffer) side of the channel–substrate interface in GaAs FETs, to a pulse applied to the gate is accurately modelled. The modelled transient is found to be non-exponential and in excellent agreement with the experimental data. The similarity between the filling and emptying rates of the traps is explained in terms of the very close position of the Fermi level in the substrate (buffer), where the trap is located, to that of the trap level.

1. INTRODUCTION

Deep traps are believed to be responsible for many parasitic effects in GaAs FETs such as the gate lag and drain lag effects in which a slow transient is observed in the drain current following a voltage applied to the gate or the drain[1]. Other effects are the hysteresis loops commonly observed in the I–V characteristics[2], the long term drift in the characteristics of the device[3,4] and the backgating (or sidegating) phenomenon in which a negative voltage applied to the substrate reduces the channel current [5–7]. The transconductance dependence on frequency is also attributed to deep traps[8] as are the low frequency oscillations which sometimes occur under a substrate bias[9]. The effect on the device noise has been related to trapping and detrapping[10–12]. The light sensitivity of the device is another effect of these traps[13].

The most common method used to study deep traps in bulk semiconductors is capacitive Deep Level Transient Spectroscopy (DLTS)[14]. In GaAs FETs the gate capacitance is too small to be measured accurately so the channel conductance mode of DLTS is used instead[15].

A common observation in Conductance DLTS spectra for GaAs FETs is a signature of a large number of hole-like traps. This is surprising since the channel is made of n-type material. Also surprising is the apparent large density of these hole-like traps. The location of traps in GaAs FETs can be (i) at the surface of the ungated regions of the device, (ii) in the active layer or (iii) near the channel–substrate interface or in the substrate itself[16]. These traps have almost identical emptying and filling rates whereas in normal DLTS the filling rates are usually very fast.

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These traps need not only be identified and characterised but also accurately located in the device geometry so that future improvements can be made. The location of these hole-like traps has not been very clear. Earlier studies pointed to the channel–substrate interface[3,4,17,18]. Later studies showed that they might also be related to the ungated area of the device[19–21]. Recently Jin and Jones (1990)[22] used a modified DLTS method to positively locate traps in each of these two regions.

In DLTS, it is usually assumed that the transient in the capacitance or conductance following a step excitation has an exponential time decay. This assumption might be true for some simple structures such as one sided p–n junctions and Schottky barriers where the density of traps is at least a few orders of magnitude smaller than that of free carriers. In devices which have more complicated geometry, such as GaAs FETs, this assumption is usually violated. This may be due to several factors of which the most important are:

(1) In GaAs FETs several close traps are usually observed in a DLTS spectrum[23] so that their responses overlap.
(2) The apparent large density of hole traps[16] which does not allow the use of some approximation.
(3) The different traps are located in different regions of the device[22] so that their responses are different.

Zylberstejn *et al.*[18] have discussed the location of the hole-like traps and concluded that the hole-like traps are very unlikely to be active in the channel itself since the hole quasi-Fermi level has no chance of crossing their energy levels in the channel region. There is a problem in the assumption that hole-like traps are located near the channel–substrate interface due to the fact that there is a response to a voltage

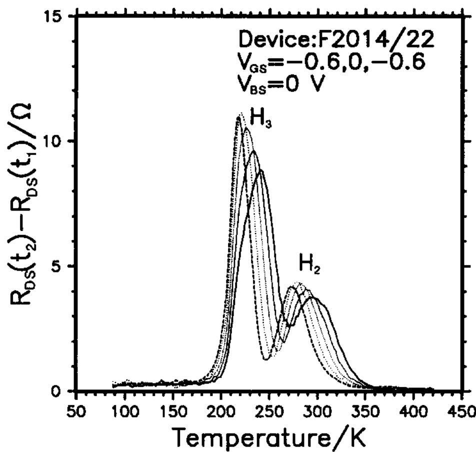

Fig. 1. GDLTS spectrum for F2014/22. The rate windows give $200 < \tau < 12.5$ ms in equal intervals using the usual DLTS rate window formula for the time constant[14].

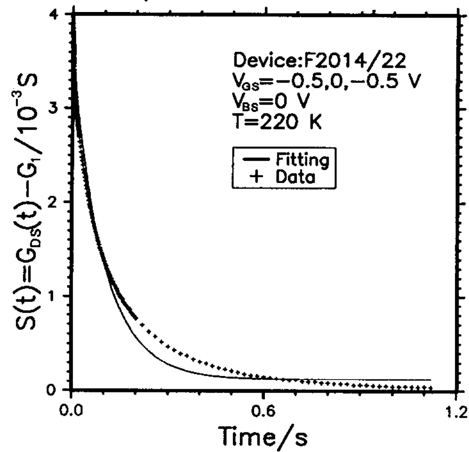

Fig. 3. An example of fitting the experimental data using a bulk trap assumption in the case where $N_T \ll N_D$. The fitting parameters are given in Table 1.

applied to the gate, however small, while the interface itself sees virtually no potential change. They suggested that the ability of a gate voltage to disturb the population of interface hole-like traps is due to the relative displacement of the hole quasi-Fermi levels in the Schottky and channel–substrate interface regions.

This paper is one of a series by the Lancaster group which discusses the properties and methods of analysis of trap effects in GaAs FETs using a wide variety of techniques. In this paper, a quantitative model for the response of an interface trap to a gate voltage step is proposed and verified by applying it to an interface hole-like trap labelled H_3. It will also be shown that the transient following emission from this trap is not a simple exponential and its accurate form will be developed. The long filling time required for this type of hole-like traps, which is comparable to the emission time, is also studied in some detail.

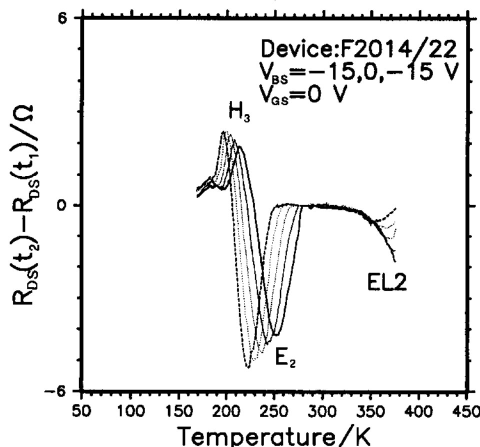

Fig. 2. SDLTS spectrum for F2014/22. The rate windows are the same as in Fig. 1.

2. EXPERIMENTS

The system that measures the DLTS rate window and the isothermal transient in the present experiments and the transient fitting procedure are described elsewhere in detail[23]. The device is biased at a constant drain–source current I_{DS}. A voltage pulse is applied to the gate and the resulting transient in the drain–source voltage $V_{DS}(t)$ due to emission or capture by the trap is measured using an A/D converter. The transient can be studied at a constant temperature by changing the pulse bias levels or the filling time or if a temperature scan is made the transient can be used to produce the conventional DLTS rate window spectrum. The times t_1 and t_2 which define the rate window satisfy the relation $t_2/t_1 = 10$. In this system it is also possible to study the transient $V_{DS}(t)$ following an electric pulse applied to the substrate. Modelling of this transient is presented in a separate publication[24].

The experimental data of the measured transient is fitted to the developed theoretical curve. In the fitting procedure the least square method is used. In this method the best fitting parameters are selected by minimising the sum of the squares of the difference between the fitting curve and the experimental data. This sum is also known as the fitting quality factor, Q.

The specimens used are low noise GaAs FETs type P35-1105 batch F2014, made by Plessey 3–5. The device has a recessed gate structure using doped epitaxial GaAs grown on a Cr doped HB semi-insulating GaAs with an undoped buffer layer. The buffer layer is 3–4 μm thick and the gate is ~0.8 μm long. It is not typical of present commercial devices.

3. RESULTS AND DISCUSSION

3.1. *Location of H_3 using DLTS experiments*

Gate DLTS (GDLTS) and substrate DLTS (SDLTS) were performed on several GaAs FETs

from a batch labelled F2014 by pulsing either the gate or the substrate. The GDLTS spectrum is dominated by two very large hole-like traps (H_3 and H_2) (Fig. 1). The SDLTS spectrum shows H_3 while H_2 is completely absent (Fig. 2). H_3 in SDLTS appears to be at a lower temperature because of the presence of an electron-like trap (E_2) which distorts the spectrum. The fact that H_2 is not excited by a substrate excitation is the first indication that H_2 is not a substrate trap and H_3 is very likely to be a substrate trap (located near the interface). This is in agreement with the findings of Jin and Jones[22] using a modified DLTS method who concluded that H_2 is located at the free surface between the gate and source or drain and H_3 is a substrate trap. There is considerable additional evidence that H_3 is located at the channel-substrate interface rather than throughout the substrate. This includes the bias dependence and amplitude normalisation discussed later.

3.2. Model for the interface trap H_3

The measured transient in the drain–source voltage $V_{DS}(t)$ following a pulse applied to the gate is converted to a conductance transient since the effect of emission from H_3 is to reduce the channel width[22]. This transient will be used to fit the theoretical model for an interface trap developed below. First, it can be shown that, for both interface and bulk traps and whether the change occurs in the gated channel only or in both the gated and ungated channels, the change in the device total conductance ΔG_{DS} is proportional to the channel width change Δa[25], thus:

$$\Delta G_{DS} = C\Delta a, \tag{1}$$

where C is a constant. If the change in the channel width is coming from the channel–substrate interface then $\Delta a = -\Delta a_b$ where a_b is the depletion width spreading from the channel–substrate interface (the minus sign indicates that if the depletion width increases then the channel width decreases). Therefore eqn (1) becomes:

$$\Delta G_{DS} = -C\Delta a_b. \tag{2}$$

Before considering a model for an interface trap, the possibility that H_3 is a bulk trap located in the channel is considered. As quoted in Section 1, Zylberstejn *et al.*[18] have argued (qualitatively) that hole-like traps are very unlikely to be located in the channel bulk. This will be demonstrated quantitatively here. The application of a reverse bias V_{GS} to the Schottky gate creates a depletion region in the channel. Assuming that there is a hole trap in this depletion region which can emit holes within this depleted region then the depletion width can be written as [26]:

$$W \approx \sqrt{\frac{2\epsilon_0\epsilon_s(V_B - V_{GS})}{q(N_D - N_T^-)}}, \tag{3}$$

where ϵ_0 is the free space permitivity, ϵ_s is the semiconductor relative permitivity, V_B is the Schottky built-in voltage, N_D is the channel doping density and N_T^- is the ionised density of the hole trap.

Table 1

τ(ms)	$A(10^{-3}$ S)	$A_0(10^{-3}$ S)	Q
91.18	3.3	0.24	7.02

The time dependence of eqn (3) can be derived from the time dependence of N_T^-, after an emptying pulse, which is given by[23]:

$$N_T^-(t) = N_T\left[1 - \exp\left(-\frac{t}{\tau}\right)\right], \tag{4}$$

where N_T is the total trap density. If $N_T \ll N_D$ then the additional depletion width due to traps should have a simple exponential decay. In this case the conductance transient signal $S(t)$ can be represented by a simple exponential form, since the conductance change is proportional to the channel width change, thus:

$$S(t) = A\exp\left(-\frac{t}{\tau}\right) + A_0, \tag{5}$$

where A is a constant (the conductance transient amplitude) and A_0 is a term which has to be added in the presence of any apparatus drift and possible slow transients[23].

The experimental data of the conductance transient are fitted to an equation of this form and is shown in Fig. 3. The fitting parameters are presented in Table 1. The fitting is not good.

In the other case where N_T is not very small compared to N_D, then the approximation made in eqn (5) is not valid. The experimental data are then fitted to an equation of the form:

$$S(t) = A_0 - A\sqrt{\frac{1}{1 - \frac{N_T}{N_D}[1 - \exp(-t/\tau)]}}, \tag{6}$$

where A is the conductance transient amplitude and A_0 is a term which has to be added in the presence of an apparatus drift and possible slow transients. This is basically the same idea as that of Okushi and Tokumaru[27] in which the DLTS signal is defined as the square of the capacitance and the method is referred to as C^2-DLTS. The fitting of the experimental data to eqn (6) is shown in Fig. 4 and the fitting parameters are presented in Table 2. Again this fitting is not good enough. In addition to the fitting being not good the value of N_T/N_D evaluated from the fitting is ~0.0013 which is not acceptable since the percentage of the transient to the total signal is observed to be at least 20% (the evaluated values means that the transient amplitude is only 0.13% of the total signal). Several values for N_T/N_D

Table 2

τ(ms)	$A(10^{-3}$ S)	$A_0(10^{-3}$ S)	N_T/N_D	Q
91.1	5105.9	5109.4	0.0013	7.1

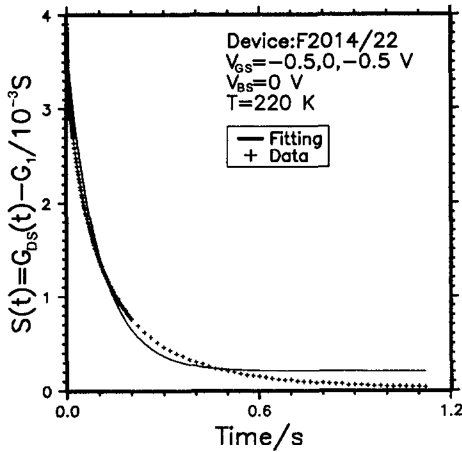

Fig. 4. An example of fitting the experimental data using a bulk trap assumption in the case where N_T is not $\ll N_D$. The fitting parameters are given in Table 2.

$(0.1, \ldots, 0.4)$ were assumed and the fitting was even worse. Therefore H_3 is very unlikely to be a bulk trap located in the channel.

Now the modeling of the transients due to emission and capture is developed assuming that H_3 is an interface trap. First we need to understand what are the mechanisms by which the population of interface traps can be affected by a voltage applied to the gate while the channel–substrate interface itself sees no applied voltage. We have already referred to the qualitative model suggested by Zylberstejn *et al.* (1979) in Section 1. For simplicity we make the following assumption. Since a voltage applied to the gate is found to modify the population of traps located near the channel–substrate interface then we assume that a potential drop exists at this interface. This potential drop implies the existence of a space charge region and this is the right condition for traps to change their population. This potential drop should be proportional to $(V_B - V_{GS})$, but this proportionality is not required to be known since it will be included in one of the fitting parameters as will be shown.

Table 3

τ(ms)	$A(10^{-3}$ S)	$A_0(10^{-3}$ S)	Q
183.489	3.834	3.889	0.365

It is clear in this case that the trap is in the substrate side of the channel–substrate interface. Therefore the depletion width in the channel is given by (assuming that $N_T \ll N_D$):

$$a_b(t) \approx \sqrt{\frac{2\epsilon_o \epsilon_s V_{eff}}{q N_D^2}[N_A + N_T^-(t)]}, \tag{7}$$

where N_A is the free carrier density in the substrate and V_{eff} is the voltage drop in the space charge region at the channel–substrate interface. Therefore the time dependence of the conductance change following emission from H_3 can be written as (since it is proportional to the change in the channel width):

$$\Delta G_{DS}(t) = -A\sqrt{\frac{N_A}{N_T} + 1 - \exp(-t/\tau)}$$
$$\approx -A\sqrt{1 - \exp(-t/\tau)}, \tag{8}$$

where A is a constant. In this equation $N_A \ll N_T$ in the substrate and the data used in the fitting correspond to $t > 0$ so that the approximation made is acceptable. The DLTS signal $[S(t) \propto \Delta G_{DS}(t)]$ can then be written as:

$$S(t) = A_0 - A\sqrt{1 - \exp(-t/\tau)} \tag{9}$$

where A is the conductance transient amplitude and A_0 is a term which has to be added in the presence of any apparatus drift and possible slow transients. The experimental data are then fitted using this equation. An example of this fitting using one decay is shown in Fig. 5. The fitting parameters are presented in Table 3. This fitting looks much better than the two

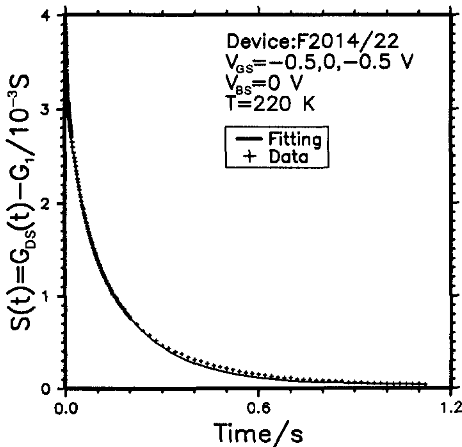

Fig. 5. An example of fitting the experimental data using the interface trap assumption. The fitting parameters are given in Table 3.

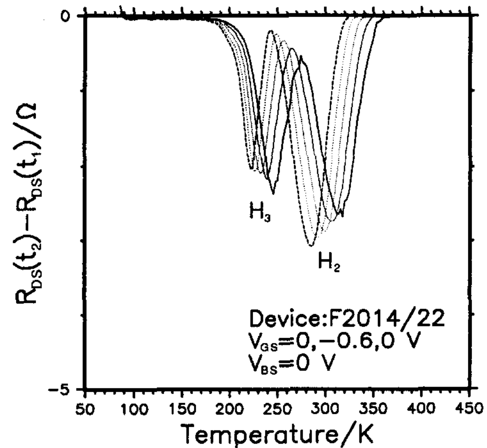

Fig. 6. Reverse GDLTS spectrum for F2014/22 to show the symmetry in emptying and filling rates for H_3 (compare with Fig. 1). The rate windows are the same as in Fig. 1.

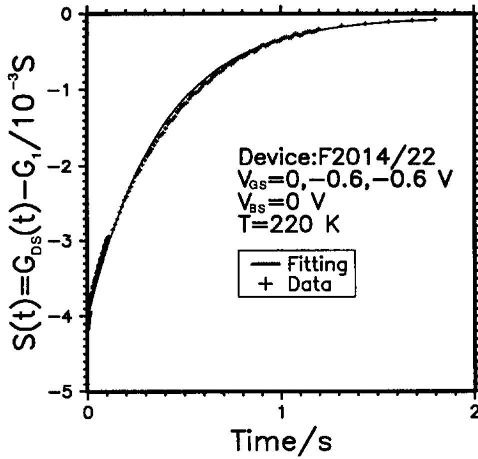

Fig. 7. An example of fitting the reverse transient (capture) to an interface trap assumption. The fitting parameters are given in Table 4.

previous ones (Figs 3 and 4) and Q is smaller compared with Q in Tables 1 and 2.

The equation for capture dominated transients differs from the emission case only in the time dependence of the charge change. The importance of modeling these transients arises from the observation that when the gate pulse polarity is reversed the signature of H_3 is also observed (Fig. 6). In Fig. 6, the spectrum is referred to as RGDLTS (Reverse Gate DLTS). In RGDLTS the capture process is measured instead of emission[28]. Comparison of Figs 1 and 6 shows that both traps H_3 and H_2 have approximately symmetrical emptying and filling rates. This phenomenon has received little attention and will be studied here for the trap H_3 in detail.

In the capture process the captured charge (or the filled trap portion), after a filling pulse, is given by [25]:

$$N_T^- = N_T \exp\left(-\frac{t}{\tau}\right). \tag{10}$$

Therefore in the capture process the transient signal has the form:

$$S_c(t) = B_0 - B\sqrt{\exp\left(-\frac{t}{\tau_c}\right)}, \tag{11}$$

where B is the capture transient amplitude, B_0 (like A_0) is a term which has to be added in the presence of any apparatus drift and possible slow transients and τ_c is used here to indicate that it might be different from τ used for emission [compare with eqn (9)]. An example of this fitting is shown in Fig. 7 for F2014/22 of which the RGDLTS spectrum shows only one trap at $T = 220$ K. The fitting parameters are presented in Table 4.

Table 4

τ_c(ms)	$B(10^{-3}$ S)	$B_0(10^{-3}$ S)	Q
254.450	4.061	0.041	0.21

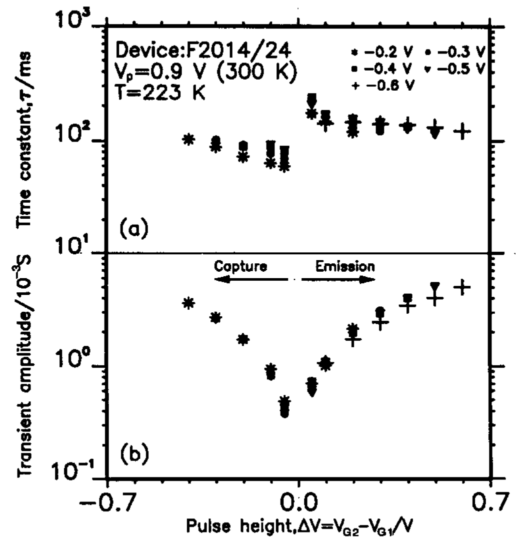

Fig. 8. The time constants (a) and amplitudes (b) of H_3 evaluated by fitting the experimental data to an interface trap assumption using the device F2014/24 ($V_p \approx 0.9$ V) at different V_{G1}'s (different symbols).

3.3. *The bias dependence of H_3*

The bias dependence is studied by measuring the transient in the drain–source conductance $G_{DS}(t)$ following a change in the gate voltage V_{GS} from V_{G2} to V_{G1} (V_{G1} is the voltage at which the transient is measured). Both cases where $V_{G1} > V_{G2}$ and $V_{G1} < V_{G2}$ are studied since H_3 is symmetrical in emptying and filling rates (compare Fig. 6 with Fig. 1).

At a constant temperature, $T = 233$ K, the voltage at which the measurement is taken, V_{G1}, is kept constant and the pulse height $\Delta V = V_{G2} - V_{G1}$ is changed from positive to negative values by changing V_{G2} from larger to smaller values than V_{G1}. This experiment is repeated at several fixed V_{G1}'s. The results do not depend much on the value of V_{G1}. The transient time constants and amplitudes evaluated from fitting the experimental data at different biases are presented in Fig. 8 for F2014/24. This device has exactly the same DLTS spectrum as F2014/22[25].

The bias dependence of the time constant can be summarized as follows:

(1) When $\Delta V > 0$ [emission in Fig. 8(a)] the time constant is almost constant for large pulse heights. When the pulse height approaches zero, the time constant increases.
(2) When the pulse height is negative [capture in Fig. 8(a)] then the time constant is generally comparable to the emission time constant (symmetrical). This is unusual since in a semiconductor the filling rate is very much faster than the emptying rate. Also it is apparent that the capture time constant decreases with decreasing pulse height magnitude.

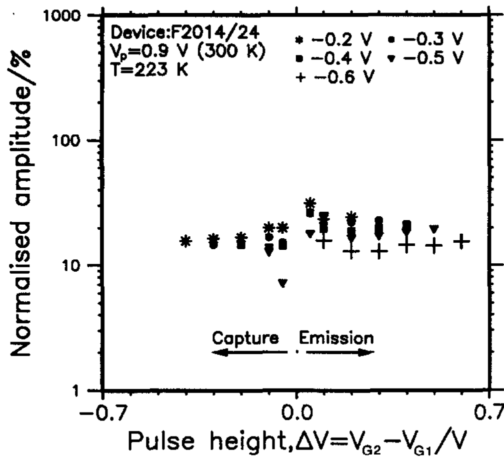

Fig. 9. The normalised amplitudes $A\%$ at different V_{G1}'s for F2014/24.

There are two features which need discussion, the basic symmetry of the time constant with the sign of ΔV and the details of the departure from this overall pattern in the capture case.

Let us first discuss the basic symmetry in filling and emptying rates. The possibility that the emission and capture are taking place in the vicinity of the depletion edge, where there is a tail of free carriers, is the cause of the symmetry in emptying and filling rates can be easily ruled out since then it is expected that the capture rate will be faster as the pulse height increases in magnitude. The observation is that the capture time constant τ_c increases rather than decreases as $|\Delta V|$ increases. Also the possible temperature dependence of the capture cross section can be ruled out since it will have the same temperature effect on both rates. In normal DLTS the emission rate has an additional temperature dependence through the activation energy. Therefore the ratio of two rates is expected to be thermally activated. This is not the case since it was observed that the rates have almost similar temperature dependence (compare Figs 1 and 6).

The most likely case to explain the symmetry in emptying and filling rates is the fact that the Fermi level in the substrate, where H_3 is located, is very close to the energy level of H_3. The emission time constant is given by:

$$\tau_e = [\sigma\langle v_{th}\rangle N_V]^{-1}\exp\left(\frac{E_T - E_V}{kT}\right) \quad (12)$$

where $\langle v_{th}\rangle$ is the average thermal velocity of holes, σ is the capture cross section and N_V is the density of states in the valence band. The free hole density is given by:

$$p = N_V \exp\left(-\frac{E_F - E_V}{kT}\right). \quad (13)$$

In undoped (buffer) or SI GaAs the position of the Fermi level E_F is controlled by the dominant trap (H_3 in the present case) since the free carrier density is orders of magnitude smaller than the trap density. Assuming that $E_F = E_T \pm \epsilon$ where ϵ is a very small energy separation between the Fermi and trap levels then the capture time constant is given by:

$$\tau_c = [\sigma\langle v_{th}\rangle p]^{-1}$$

$$= [\sigma\langle v_{th}\rangle N_V]^{-1}\exp\left(\frac{E_T \pm \epsilon - E_V}{kT}\right). \quad (14)$$

From the above two equations one can obtain the ratio of the two time constants as

$$\frac{\tau_c}{\tau_e} = \exp\left(\frac{\pm\epsilon}{kT}\right). \quad (15)$$

Since ϵ/kT is small then the above three equations mean that the two time constants are comparable and thermally activated through $(E_T - E_V)$ in nearly the same way. Actually, $\epsilon = \Delta E(\text{emission}) - \Delta E(\text{capture}) \approx 0.02$ eV (as will be shown at the end of this section, Fig. 10). In this case $\tau_c \approx 0.4\tau_e$. This is experimentally observed for a large range of ΔV.

Now let us look at the details of the symmetry in the capture time constant. For emission the time constant increases as the pulse height approaches zero. This increase may be due to some unknown systematic errors since it is expected that the time constant is expected to decrease to $\sim(e_p + c_p p_1)^{-1} = (2e_p)^{-1}$ at $\Delta V = 0$. As $|\Delta V|$ decreases in the capture case we observe that the capture time constant decreases. A possible explanation of this asymmetry is that the free hole density in the neutral region decreases with increasing

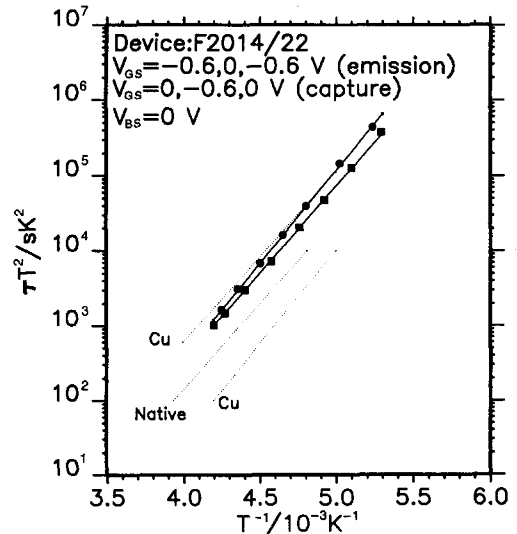

Fig. 10. The Arrhenius plot of the time constants obtained by fitting the transients at several fixed temperatures using eqn (9) for positive pulse height (emission, circles) and using equation (11) for negative pulse heights (capture, squares). The straight lines are the best fits. The dotted lines are some of the hole traps reported in the literature for [32,33] and another native defect[34]. In the bias notation the transient is acquired during the third bias value.

distance from the initial depletion edge towards the channel–substrate interface since it decreases from its peak value, at the depletion edge, by means of diffusion which may take a very long time in SI GaAs[29,30]. So the wider the previously depleted region the smaller is the diffused hole density. Since the capture time constant is inversely proportional to the hole density then the smaller is the latter the longer is the former. Unfortunately this cannot be confirmed in the present work since we used devices and not materials. Also we have very little knowledge about the SI GaAs used as a substrate. Add to all this the well known complicated nature of SI GaAs[31].

3.4. *Amplitude normalisation for the bias dependence of H_3*

The volume of the neutral channel created by the ionised trap can be normalised to the total volume depleted during the excitation. This can be represented by the percentage ratio of the decay amplitude, A (in conductance units) to the total change in the conductance due to the excitation $\Delta G = G_2 - G_1$. That is:

$$A\% = \frac{A(S)}{G_2 - G_1} \times 100. \tag{16}$$

This normalisation is shown in Fig. 9. It can be seen that compared with the raw data of Fig. 8(b) the normalisation produces fairly uniform results. Also the normalised amplitude decreases with increasing reverse bias (V_{G1}). This is expected from an interface trap since the amplitude should be proportional to $\sqrt{N_T}$ which decreases away from the interface, at large $|V_{G1}|$. We have also found that if the conductance transient amplitude is normalised to the applied voltage then the normalised amplitude is practically independent of the applied gate voltage[25].

3.5. *Characterisation of H_3*

The parameters of the trap can be evaluated very accurately by optimising the experimental conditions by using a large positive pulse height with a long filling time so that the trap is completely filled (or emptied) before allowing it to empty (or fill). This experiment is carried out using the device F2014/22 using both positive and negative pulse heights. The bias was -0.6, 0, -0.6 V for emission (positive pulse height) and 0, -0.6, 0 V for capture (negative pulse height) to show that capture is thermally activated in almost the same way as emission for this trap. The conductance transient is fitted to eqn (9) for emission and to eqn (11) for capture at several fixed temperatures and the results are presented in Fig. 10 which represents the Arrhenius plot of the corrected time constant vs $1/T$ using eqns (12) and (14). Also presented in Fig. 10 are some of the closest bulk hole traps to H_3 which are reported in the literature. Two of them are related to the presence of copper[32,33] and the other is attributed to a native defect (Ikuta *et al.*[34], $E_A = 0.45$ eV). Since our devices are not doped with Cu then H_3 is very likely to be a native defect or perhaps a characteristic of the channel–buffer interface. This identification is enhanced by the fact that other devices with a thinner buffer layer show a very small H_3[25]. The activation energies evaluted from these two Arrhenius plots are 0.467 ± 0.006 eV from the emission data and 0.443 ± 0.003 eV from the capture data. The temperature at which $\tau = 200$ ms is 218 ± 1 K. The difference between the two activation energies 0.024 eV corresponds to the separation of the trap and Fermi energies discussed earlier. A detailed study of the properties of H_3 using several additional techniques such as excess noise, g_M dispersion in Lancaster so that their results can be compared will be presented elsewhere[35].

4. CONCLUSION

It was shown that the transient due to H_3 is best fitted to an interface trap assumption and a quantitative model for this is proposed. This model shows that the transient due to interface traps in GaAs FETs is not a simple exponential and it is expected that this will introduce errors in the evaluation of the trap parameters. The normalised trap amplitude using the interface assumption was shown to be almost independent of the excitation amplitude ΔV and decreases with increasing reverse bias which is expected from an interface trap. It was also shown that the basic symmetry in emptying and filling rates for H_3 is due to the fact that the Fermi-level position in the substrate, where the trap is located, is pinned near the trap level.

Modeling of the transient following a pulse applied to the substrate is not considered here since the devices used are not suitable because of the appearance of an electron trap larger than H_3 in SDLTS (E_2 in Fig. 2). This modeling will be carried out using more suitable devices for another hole trap and will be presented in a subsequent paper.

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