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والبحث العلمي والعلاقات الخارجية

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Simulation bidimensionnelle de l'effet des pièges profonds dans le substrat sur les caractéristiques des Transistors à Effet de Champ en Arséniure de Gallium (GaAs FETs)

(Two Dimensional Simulation of Deep Level Substrate Effect on the Characteristics of the GaAs Field Effect Transistor (GaAs FETs))

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Abstract

In this thesis, the reduction of the conductance of GaAs FETs by a negative voltage applied to the substrate, termed backgating or sidegating, was numerically modeled to determine which type of traps is responsible of this phenomenon. Drift diffusion Modelling was carried out for several sets of deep levels in the substrate. It has been observed that deep acceptors are mainly responsible for backgating, independently of the shallow level type in the substrate. In this case, there is no threshold. However, when deep donors are present in the substrate, backgating is again reduced but with a threshold. The presence of a buffer layer between the channel and the semi-insulating substrate also helps reducing backgating.

A two dimensional-hydrodynamic model was carried out to predict the performance of short-gate length power III–V field effect transistors. The model is based on the conservation equations, deduced from the Boltzmann transport equation and solved in their whole form. This model is also well suited to study the effect of substrate deep levels on the device. The results of hydrodynamic model (physical model) were compared to those of the fully distributed model (electrical model), especially, as for high frequency operating. In fact, at high frequencies, the dimensions of the electrodes of microwave transistors such as FETs become comparable to the wavelength, highlighting the parasitic effect of wave propagation. Thus, this effect needs to be accurately evaluated in the device model to assure a reliable design.

In the electrical model, the device width was then divided into an infinity number of segments, while each segment was considered as a combination of three coupled lines and a conventional FET equivalent circuit. By solving a set of multi-conductor transmission line equations using the Finite-Difference Time-Domain (FDTD) technique, an accurate and efficient transistor modeling approach was proposed.

Furthermore, the two dimensional hydrodynamic model had been shown to provide a valuable insight into the operation devices and confirm in many cases the measurements. Thus, the HDM model was used to study the effect of the gate length and its the recess depth on the recessed gate MESFET and pHEMT. It was found that, the performance of these devices is improuved by shrinking the gate length and deepening the recess. The effect of increasing the delta doped density on the pHEMT performance was also studied. It is a way to improve the transfer efficiency of electrons from the delta-doped AlGaAs layer to the InGaAs channel. For the deep levels, it was found that deep acceptors improve the transistor performance while deep donors degraded it.

Index Terms: GaAs FETs, Backgating, deep traps, Hydrodynamic model, FDTD, time domain, wave effects.

Résumé

Dans cette thèse, la réduction de la conductance des transistors GaAs FETs par une tension négative appliquée au substrat (effet backgating ou sidegating) a été modélisée numériquement dans le but de préciser quel est le type de piège responsable de ce phénomène. La modélisation dérive-diffusion est effectuée pour plusieurs ensembles de niveaux profonds dans le substrat. Il a été observé que les accepteurs profonds sont principalement responsables du backgating et ce, indépendamment du type de niveau peu profond dans le substrat. Dans ce cas, il n'existe pas de seuil. Lorsque les niveaux donneurs profonds sont présents dans le substrat, on observe que cet effet est réduit avec une tension de seui. La présence d'une couche tampon entre le canal et le substrat semi-isolant contribue également à réduire l'effet backgating.

Le modèle hydrodynamique bidimensionnel est réalisé pour prédire les performances des transistors de puissance III-V à grille courte. Le modèle est basé sur les équations de conservation, déduites de l'équation de transport de Boltzmann, et résolues dans leur forme entière. Ce modèle est également bien adapté pour étudier les effets des niveaux profonds de substrat sur le dispositif. Les résultats du modèle hydrodynamique (modèle physique) ont été comparés à celui du modèle entièrement-distribué (modèle électrique), en particulier, dans le cas de fonctionnement en hautes fréquences où les dimensions des électrodes des transistors comme les FET deviennent comparables à la longueur d'onde, mettant en évidence l'effet parasite de la propagation des ondes. Ainsi, cet effet doit être évalué avec précision afin d'assurer une conception fiable.

Dans le modèle électrique, les électrodes des transistors ont été divisées en un nombre infini de segments, chaque segment étant considéré comme une combinaison de trois lignes de transmission couplées et d'un circuit équivalent FET classique. Les équations différentielles résultantes ont été résolues en utilisant la méthode des différences finies dans le domaine temporel, une approche temporelle précise et efficace de modélisation du transistor.

En outre, nous avons démontré l'aptitude du modèle hydrodynamique bidimensionnel de fournir des indications précieuses sur les caractéristiques des composants, indications confirmées par les mesures. Ainsi, le modèle HDM a été utilisé pour étudier l'effet de la longueur de la grille et la profondeur de son recess sur le MESFET à grille creusée et le pHEMT. Il a été constaté que les performances sont améliorées en réduisant la longueur de la grille et l'augmentation de son approfondissement. L'effet de l'augmentation de la densité de la couche delta–doped a été aussi étudié. En effet, ca améliore l'efficacité du transfert des électrons de la couche AlGaAs au canal InGaAs. Pour les niveaux profonds, il a été constaté que les accepteurs profonds améliorent les performances des transistors tandis que les donateurs profonds les dégradent.

Mots Clés: GaAs FETs, Backgating, pièges profonds, modèle Hydrodynamique, FDTD, domaine temporal, effets d'onde.

ملخص:

في هذه الرسالة تمت دراسة (باستعمال النمذجة الرقمية)إنخفاض ناقليه الترانزستور ذوالتأثيرالحقلي غاليوم أرسيند (GaAs FETs) بتطبيق جهد سالب على المسند و المعرّف ب Backgating أو Sidegating من أجل تعيين أي نوع من المستويات العميقة المسؤولة عن هذه الظاهرة.

تم استعمال نموذج جر – إنتشار لعدة مجموعات من المستويات العميقة الموجودة في المسند. لقد لوحظ أنّ المستويات الأخذة العميقة هي المسؤولة الأساسية عن ظاهرة backgating و بشكل مستقل عن نوع المستويات الأقل عمقا في المسند. في هذه الحالة لا يوجد عتبة الجهد. في وجود المستويات المانحة العميقة في المسند, ظاهرة backgating تتناقص مع وجود عتبة الجهد. وجود طبقة شبه ذاتية بين القناة و المسند نصف العازل يساعد أيضا في التقليل من ظاهرة backgating.

تم وضع نموذج ثنائي الأبعاد الهيدروديناميكي من أجل التنبأ بتصرف الترانزستورات ذوالتأثيرالحقلي المبنية على أنصاف النواقل V-III ذات طول البوابة القصير. هذا النموذج يعتمد على معادلات الحفظ و المستنتجة من معادلات النقل لبولتزمان Boltzmann, حيث تحل في شكلها الكامل. هذا النموذج أيضا مناسب تماما لدراسة تأثير المستويات العميقة الموجودة في المسند على الترانزستور.

تمت مقارنة نتائج النموذج الهيدروديناميكي (النموذج الفيزيائي) لتلك النتائج المتحصلة من نموذج الموزعة الكليا (النموذج الكهربائي) خاصة عند التشغيل في التواترات العالية. في الواقع, من أجل التواترات العالية, أبعاد الأقطاب للترانزستورات الميكروموجية مثل الترانزستورات ذوالتأثيرالحقلي تصبح مقاربة لطول الموجة مما يحدث تأثير التشويش للموجة المنتشرة. و لهذا, هذا التأثير يحتاج إلى تقييم دقيق في نموذج الترانزستور لضمان تصميم موثوق به.

في النموذج الكهربائي تمّ تقسيم عرض الترانزستور إلى عدد لا متناهي من القطع, في حين إعتبرنا كل قطعة من المجموعة كمساهمة ثلاث خطوط إرسال مقرونة و دائرة مكافئة للترانزستور ذوالتأثيرالحقلي كلاسيكية. لحل مجموعة المعادلات التفاضلية الناتجة, تمّ إستعمال تقنية الفروق المحدودة في المجال الزمني (FDTD) و التي تتميز بدقّة زمنية و كفاءة في نمذجة الترانزستور. علاوة على ذلك, تم البرهنة على قدرة النموذج الهيدروديناميكي ثنائي الأبعاد في توفير معلومات قيّمة حول عمل الترانزستور و تم تأكيده بقياسات في حالات عدّة.

من أجل ذالك تمت دراسة تأثيرا لأبعاد التكنولوجية لترانزستور مثل طول البوابة وعمقها. وقد وجد أن تصغير طول البوابة وتعميقها يحسن من أداء الترانزستورات. وكذلك تمت دراسة تأثير زيادة كثافة دلتا-مطعمة على أداء pHEMT. في الواقع، هي وسيلة لتحسين كفاءة ناقلية الإلكترونات من طبقة AlGaAs إلى القناة InGaAs. تمت كذالك دراسة تأثير المستويات العميقة في المسند، وقد وجد أن الأخذة العميقة تحسن من الأداء الترانزستور والعكس في حالة المستويات المانحة العميقة.

الكلمات الدلالية: ترانزستور تأثير حقل ـ ناقلية – النموذج الهيدروديناميكي - تقنية الفروق المحدودة في المجال الزمني - خطوط إرسال

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Dedication

I dedicate this work to my loved Father, my Praiseworthy two mothers, to the nicest person Boussaha Abdeldjalil (late), to Dr Sengouga Nouredine for his support and assistance and to Dr Mustapha Cherif-Eddine Yagoub for guiding me with respect and patience.

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List of Acronyms

2DEG	Two dimensional (2D) electron gas
Al	Aluminium
As_{Ga}	The defect if an arsenic atom is on a gallium lattice site
BTE	Boltzmann Transport Equation
CAD	Computer Aided Design
CPU	Central Processing Unit
Cr	Chromium
DDT	Drift-Diffusion Transport
DX	Deep Donors States
EL	Electron Traps
EL2	The deep-donor trap
FET	Field Effect Transistor
FDTD	The Finite Difference Time Domain
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GHz	Giga Hertz
HBT	Heterojunction Bipolar Transistor
HB	Horizontal Bridgman Process
HEMT	High Electron Mobility Transistor
HDM	Hydrodynamic Model
HL	Hole Traps
HP	Hewlett Packard
InP	Indium Phosphide
JAC	Jacobian Matrix
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LNA	Low Noise Amplifier
LEC	Liquid Encapsulated Czochralski

LTG	low temperature grown
LPE	Liquid-Phase Epitaxy
MESFET	Metal Semiconductor Field Effect Transistor
MBE	Molecular-Beam Epitaxy
MC	Monte-Carlo
MMIC	Monolithic Microwave Integrated Circuits
MOVPE	Metallo-Organic Vapor-Phase Epitaxy
NF	Noise Figure
NEC	Nippon Electronic Corporation
PDEs	Partial Differential Equations
RF	Radio Frequency
S	Sulfur
Si	Silicon
SiC	Silicon Carbide
Si_3N_4	Silicon Nitride
SiO_2	Silicon dioxide
SI GaAs	Semi-Insulating Gallium Arsenide
TL	Transmission Line
TEM	Transverse ElectroMagnetic

List of Symbols

a	The hydrostatic potential
A_0	Curtice model parameter
A_1, A_2, A_3	Curtice model parameter
α	Curtice model parameter
α_Γ	The ratio of Γ valley carrier population to the carrier concentration
α_L	The ratio of L valley carrier population to the carrier concentration
α_X	X valley carrier populations to the carrier concentration
α_n	3rd valley transition factor
α_r	allowed error
b	The shear deformation potential
B	Magnetic field
β	Curtice model parameter
Beta	Power in the standard analytic field-dependent mobility model
BV_{gd}	Breakdown voltages
C_{ds}	The drain-to-source capacitance of the FET
C_{gd}	The gate-to-drain capacitance of the FET
C_{gs}	The gate-to-source capacitance of the FET
$C_{n(p)}$	The trap capture coefficient for electrons (holes)
C_p	The pad capacitance
C_s	The 2DEG capacitance per unit area
C_{pds}	The parasitic drain-to-source capacitance of the FET (C_{pd})
C_{pgs}	The parasitic gate-to-source capacitance of the FET (C_{pg})
D^0	The neutral- substitutional donors
D^+	The four- coordinate substitutional donors
D_{gd}	Gate-to-Drain diode
D_{gs}	Gate-to-Source diode
Δd	Distance of the centroid of the 2DEG distribution from the AlGaAs/GaAs
ΔE_c	The conduction band offset $\Delta E_c = V_h$
Δe_r	The relative difference in lattice constant
D_n, D_p	The diffusion coefficients
d_n	The doped layer thickness

$\Delta_{\Gamma L},\ \Delta_{\Gamma X}$	The minimum energy necessary to excite an electron to an upper conduction band
δn_s	The ratio of the 2DEG charge change
E	The electric field
E_A	ionization acceptors energy
E_c	The conductance band energy
E_{cr}	The critical electric field
E_D	Ionized donors energy
E_f	The Fermi level energy
E_H	The conduction band heterojunction discontinuity
E_{gs}	The heavy hole band-gap of strained $In_yGa_{1-y}As$
E_i	The intrinsic Fermi level
E_T	The energy level of the trap
E_v	The valence band energy
$£_s$	Semiconductor permittivity
ε_0	Permittivity of free space
ε_0	The average energy at zero field
ε_r	The relative permittivity
η	The modulation efficiency
f	The frequency
F_c	Curtice parameter
F_{min}	Minimum noise figure
f_{max}	Maximum oscillation frequency
f_t	The cut-off- frequency
$\emptyset_b$	Schottky barrier height
G	The generation rate
G_a	The amplifier Gain
G	The conductance of the planar MESFET
G_A, G_D	Degeneracy factors for the conduction and the valence bands
G_m	Channel transconductance
γ	Curtice model parameter
γ_m	Power in the negative differential mobility model
G_{ds}	Drain to source conductance
g_{ds}	The output conductance of the field effect transistor

g_m	The transconductance of the field effect transistor
g'_m	The extrinsic transconductance
$\hbar = \frac{h}{2®}$	Plank constant
H	Height of the gate strip
h_{ch}	Channel thickness
h_{dep}	Depletion width
I_{ds0}	The DC component of the drain-to-source current
I_{ds}	The radio-frequency component of the drain-to-source current (I_{ds}=I_d).
I_{dss}	Zero-gate saturation drain current
I_{sub}	Substrate current
I_{ch}	Channel current
J	Current density
J_n, J_p	The electron and hole current densities
K_B	Boltzmann's constant ($1.38*10^{-16}$ /K)
λ	Curtice model parameter
λ_K	The k^{th} bound-state energy level
L_D	Debye length
L_{dd}	The drain inductance of the field effect transistor (L_{dd} =L_d)
l_g	Gate length of the field effect transistor
L_{gg}	The gate inductance of the field effect transistor (L_{gg} = L_g)
L_{ss}	The source inductance of the field effect transistor (L_{ss} = L_s)
l_{sg}	The source-to-gate length
l_{gd}	The gate-to-drain length
m_0	Effective electron mass at the rest (m_0 = m_e)
m_c	effective mass at conduction band energy
M_{gd}	Mutual inductances between drain and gate
M_{gs}	Mutual inductances between source and gate
M_{ds}	Mutual inductances between source and drain
μ	Mobility of the free carrier (electron)
μ_p	Free space permeability ($12.56*10^{-6}$ H/m)
μ_n ,μ_p	The mobilities for the electron and hole
μ_{fp}	the free space permeability

n	Free electron density
n_i	The intrinsic density
N_A^-	Ionized acceptor doping density
N_D	Doping density of the channel,
N_D^+	Ionized donor doping density
n_{free}	Free electrons in the donor layer
n_{bound}	Bound carrier density in the donor layer of the pHEMT
n_{sm}	The maximum 2DEG density
N_{c2D}	Constant density of states for a given effective mass and temperature
p	Free hole density
P	The equivalent hydrostatic pressure
p_s	The number of parallel strips into which the total gate-width is divided
φ	Electrostatic potential
P_{out}	The output power density
AE	The power-added efficiency
q	Electron charge ($1.60*10^{-19}$ C)
$\overrightarrow{Q_1}$	The carrier heat flow
Q_{tot}	The total charge
Q_{gs}	The gate-to-source stored charge
Q_{gd}	The gate-to-drain stored charge
R_c	Ohmic contact resistance
R_d	The drain resistance of the field effect transistor
R_{ds}	The output resistance of the field effect transistor
R_{gg}	The gate resistance of the field effect transistor ($R_{gg} = R_{gg}$)
R_i	The channel resistance of the field effect transistor
ρ	The resistivity
R_{ss}	The gate resistance of the field effect transistor ($R_{ss} = R_s$)
σ	Electrical conductivity
T	Temperature in degrees Celsius
T_e	Electron temperature (K)
T_D^+	Ionized donor trap impurities
T_A^-	Ionized Acceptor trap impurities
T_L	The lattice temperature

τ	The transconductance delay
τ_ε	Energy relaxation time
τ_v	Velocity time relaxation
τ_p	Momentum relaxation time (s)
τ_w	Energy relaxation time (s)
U	The net recombination rate
$U_{n,p}$	The net generation-recombination rates of electron, hole carriers
U_{tot}	The total potential energy of electron
v	Carrier velocity
V_{bi}	Built-in potential of the Schottky gate
$V_{breakdown}$	Breakdown voltage
V_c	Channel potential
v_d	The drift velocity
V_{ds}	The DC drain-to-source voltage of the field effect transistor
V_{ds0}	Drain-to-source model at model evaluation point
V_{gs}	The DC gate-to-source voltage of the field effect transistor
$V_{ns,}$	The electron saturation velocity
v_{pinch}	Pinch-off voltage
v_{ps}	The hole saturation velocity
v_s	Saturation velocity (v_s=v_{sat})
V_{dd}	The operating voltage
V_{knee}	knee voltage
V_{th}	Threshold voltage
w_{Av}	Angular velocity(w_{Av}= ω)
w_{dev}	The device width
Y	The admittance matrix
Z	The impedance matrix
ζ_K	The k^{th} bound-state wave function

Introduction

Motivation

The glaring evolution of an extensive range of microwave and millimeter-wave communication systems is due to the fact that the technology of microwave integrated circuits has continuously grew through successive steps. First of all, the GaAs MESFETs were the most commonly used active devices and many key design techniques were pioneered. Then, as second step in advanced technology, the heterojunction devices have been introduced and rapidly improved. This enabled the circuits to operate over 100GHz [Golio; 1991, Mass; 2003].

Currently, because of the maturation of the HEMT technology, Monolithic Microwave Integrated Circuit (MMICs) operating beyond 100 GHz are now emerging from research to the commercial production [Sheng;2006, Golio; 2008].

Due to the high performance electronics that are evolving with a large number of closely packed passive and active structures, several levels of transmission lines and discontinuities operating at high speeds and frequencies are needed. Also, by decreasing the device size and increasing the operating frequency, devices and circuits need to a continually progress of accurate techniques for modelling and simulation [Schwierz and Liou; 2003, Guillouard; 1997, Liou and Schwierz; 2003].

Moreover, the growing interest for prior design methods has driven the research effort toward a possibly complete physical-based approach. In fact, with today's powerful computing capabilities, numerical simulations based on physical modelling can be used to predict and provide better understanding of device behavior. This approach becomes significantly appreciated to understand the physical phenomena appearing in real electron devices.

Indeed, from the point of view of physical modelling, high voltage gain and operating frequencies, which can be achieved by using sub-micrometer-gate transistor lengths, require full models. Conventionally, physical modelling of semiconductor devices employs a solution of Poisson's equation to update the electric field inside the device which, in principle, presents no conceptual difficulty. However, interesting physical phenomena arise from the manner in which charge fluctuations and current responses are coupled to the fields. When semiconductor devices are operating at high frequencies, the semiconductor transport physics and consequently the device modelling problem become more involved. In such cases, quasi-static semiconductor device models fail to accurately represent the effects of the physical

phenomena where the carriers interact with the propagating electromagnetic wave along the device [Alsunaidi et al; 1996].

Accurate device physical modelling is at least based on either two-dimensional (2D) hydrodynamic models or particle Monte-Carlo (MC) models. The Monte-Carlo model is the most accurate but it requires huge CPU resources. Therefore, the hydrodynamic model may represent a reasonable compromise between accuracy and computational requirements. The hydrodynamic equations are obtained from the Boltzmann equation by the method of moments [Rousseau et al; 2003].

On the other hand, the integrated circuit design encounters the severe problem of dealing with non-negligible electromagnetic effects like undesired radiation and parasitic coupling between circuit elements. Such complex effects require a full-wave approach to accurately analyze them. This implies solving Maxwell's equations and taking into account the interaction between parasitic electromagnetic waves and circuit elements comprehensively. Since this interaction can affect the overall system performance, the entire system needs to be characterized as a whole package by a full-wave analysis incorporating all devices, particularly transistors like MESFETs and HEMTs, which are the core of modern communication systems.

Hence, an accurate modelling approach of such electromagnetic interaction must be taken into account, especially when the gate dimension is on the order of the wavelength. When the device dimensions become comparable to the wavelength, the input active transmission line, e.g., the gate electrode, has a different reactance from the output transmission line, e.g., the drain electrode. Therefore, they exhibit different phase velocities for the input and output signals. So, by increasing the frequency or device dimensions, the phase cancellation due to the phase velocity mismatching will affect the performance of the device. Thus, the wave propagation effect will influence the electrical performance of the device, and therefore, should be accurately considered in high frequency device modelling [Asadi; 2011].

Full-wave analysis and global modeling approach can be used to accurately consider this wave propagation effect along the device structure. But, this type of analysis is time consuming and needs a huge CPU time. Although, some efficient numerical methods have been recently proposed for simulation time reduction, this analysis approach still needs more attention for suitable implementation in simulation software.

The transverse electromagnetic (TEM) wave propagation was investigated on the three electrodes of the device (gate, source, drain), where their lengths were divided into infinite segments. Thus, the transistor was considered as a combination of three coupled lines

(representing the three terminals) and a conventional equivalent circuit of a GaAs MESFET (representing the intrinsic part of the device). So, as one of the most efficient discretization techniques, the transmission line method (TL) was selected to analyze each infinitesimal segment of the proposed model [Achar and Nakhla; 2001, Dounavis et al; 2002].

Then, the Finite Difference Time Domain (FDTD) method was preferred to numerically obtain the model element values. This method is widely used in solving various kinds of electromagnetic problems, wherein lossy, nonlinear, and inhomogeneous media and transient problem can be considered [Asadi and Yagoub; 2010; Tafove; 1996, Sadiku; 1992].

Thus, the scattering parameters of a sub micrometer-gate FET transistor were obtained by applying this modeling technique. The results were successfully compared with those obtained by the physical model.

Contribution overview

The major contributions of this work expected from the successful fulfillment of the research objectives are listed below:

1 An efficient physical model including Maxwell's equations was proposed and applied to field effect transistors (including deep level effects). Based on the physical geometry and the physical process that characterize the device, the physical model requires a description on the carrier transport physics and the associated geometrical and material properties of the transistor. The physical modelling obtained device electrical behavior from basic parameters such as device dimensions and material characteristics. This is accomplished by solving a set of equations that describe the motion of charge carriers through the device. These equations typically include the Poisson, current continuity, drift-diffusion, energy and momentum conservation equations [Jingyi; 2002, Mercury; 2004, Sze; 2007].

2 A novel and accurate small-signal modeling procedure for microwave FETs as three active coupled transmission lines is presented; this linear distributed model considers the effect of wave propagation along the device electrodes. In this modeling technique, the active multi-conductor transmission line equations are obtained, which satisfy the TEM wave propagation along the FET electrodes. This modeling procedure was applied to FETs by solving the equations using Finite-Difference Time-Domain (FDTD) technique [Gaoua et al; 2010, Asadi and Yagoub; 2010(a), Asadi and Yagoub; 2010(b), Yagoub et al; 2009, Gaoua et al; 2009].

3 A proposed physical/electrical distributed time-domain FET model including wave-propagation effects and trap effects was successfully validated. It can be successfully used in FET-based circuit design and optimization up to millimeter-wave frequencies.

Thesis Outline

In this dissertation, an efficient physical modelling of GaAs Field Effect Transistors (FET) is presented and its equivalent electrical parameters extracted. Then, it is demonstrated through successful comparison with measurements.

Therefore, the work is going to be divided into a general introduction, four chapters, and a conclusion.

General introduction describes the motivation behind FETs modelling methods. Then, chapter I gives an overview of GaAs based MESFETs and HEMTs with analytical description of the device operation.

Chapter II describes the hydrodynamic model (physical model), which introduces the two hydrodynamic FET model by solving the Boltzmann transport equations and the single electron gas approach. Next, a presentation of deep trap effects and their nature in different varieties of GaAs based materials is performed. Then, and as the material parameters are also undergo a variation due to the mole fraction of aluminium and indium in the structure, a given set of equations are investigated according to these conditions.

Chapter III deals with the fundamental concept of a GaAs MESFET. The basic equations which involve its operation have been described in this chapter. Although the nonlinear modelling is crucial for the performance prediction of microwave circuits, the small signal modelling methodology is also investigated. Then, an accurate electrical modelling procedure is presented for FETs and applied to a FET by solving the equations based on three active coupled transmission lines using the Finite-Difference Time-Domain (FDTD) technique.

Chapter IV gathers the results and the corresponding interpretations. First of all, the Backgating effect in GaAs MESFET is studied as function to the density and nature of deep levels and the presence of the buffer layer. Then, the ability of the hydrodynamic model (physical model) to obtain accurate response of the device under different bias conditions is discussed. The fully distributed modelling (electrical model) is also evaluated for the GaAs FET to simulate I-V characteristics and S-parameters under the two conditions with and without including the wave propagation effect. This work concludes with a general conclusion and a list of future perspectives to further enhance this work.

Chapter I
Field Effect Transistors

I.1 Introduction

The GaAs MESFET transistor is considered as a key component in the microwave technology. It allows a new sighting for the device in many applications such as high performance MMIC technology, RF amplifiers and digital GaAs ICs.

The famous idea given by Schottky which introduced the concept of Schottky barrier FET [Schottky; 1938] was handled by Mead in 1966 as first prototype for the fabrication of Metal Semiconductor Field Effect Transistor (MESFET) [Mead; 1966]. Then, the first FET using a Gallium Arsenide (GaAs) epitaxial layer on a semi-insulating GaAs substrate was fabricated by Hooper in 1967 [Hooper and Lehrer;1967] and a proved exceptional high frequency performance was reached. Further developments in GaAs FET's were followed to offer a very low noise and high frequency capabilities. Through the improvement of the GaAs material quality, a manifested step was brought by Turner who attained for 1 μm gate length GaAs FETs a maximum frequency up to 50 GHz [Turner et al; 1971]. Then a large contribution was attributed to the GaAs devices to achieve low noise [Liechiet al, 1972] and high power FETs [Fukuta et al; 1973]. Beside these performances, the GaAs MESFET offered better electrical performance properties over its silicon counterpart.

GaAs devices have been mainly used in microwave integrated circuits [Ladbrooke; 1991, Golio; 1991, Bose; 2001]. GaAs MESFETs provided excellent noise and gain performance at microwave frequencies [Sedra and Smith; 2003].

In the early in the eighties, GaAs MESFETs were runners-up in the design of high-speed digital systems as well as in analog ICs applications, such as in satellite and fiber-optic communication systems. But due to the relative lack of maturity in technology, there was a special constraint limiting the GaAs MESFET use to a weak ratio of industrial integration.

Afterward, a fast progress in GaAs MESFETs manufacturing took off to be a rival device to other components like MOSFET. Indeed, the excellent microwave performance of the GaAs MESFET yields it to become a great attractive active device in hybrid and monolithic microwave integrated circuits (HMIC and MMIC) design [Jingyi; 2002] beside the heterostructure field effect transistor [Feng et al; 1990]. As they reached a high maximum frequency of oscillations and an interesting cutoff frequency, they became the workhorse of

GaAs technology and tended to cover a large band of applications. However the GaAs based heterojunction devices including high electron mobility transistor (HEMT) and heterojunction bipolar transistor (HBT) provide several advantages as the record of frequency reaching 400 GHz and lower noise figure for the HEMT compared to the MESFET, as well as the high transconductance and power density for the GaAs-HBT.

The InP based transistors (HBTs, HEMTs), successfully developed with reduced costs, became a rival to those of GaAs-based HEMT MMICs, including GaAs-based metamorphic HEMT technology, with superior performance. The important intend to supersede the GaAs transistors which governs the high power amplifier market became an eccentricity, today. Whereas the GaAs MESFET is still dominate for a high frequency and an increased power claim, emerging materials such as SiC and GaN, wide bandgap semiconductors, get attractive attention due to their higher breakdown voltage, higher thermal conductivity, and higher electron velocity [Golio;2001].

Due to their electrical properties such as high electron mobility, peak drift velocity and high electron velocity at low field, GaAs transistors have a high switch speed resulting in a high cutoff frequency. The large transconductance and the low ON resistance are two other major characteristics of this transistor. The manufacture and the high resistivity of Semi-Insulating GaAs substrate support the simple structure of the MESFET and hold its technology out to reduce parasitic capacitance. Whereas Si, SiGe RF and high speed ICs are forecasting to be triumph RF devices for large wireless applications below 5 GHz [Jingyi;2002], the GaAs devices persist to dominate the recent industry for Multi-Band/Multi-Mode Cellular, Bluetooth and Wireless LAN applications. Agilent Technologies, formerly HP, developed products with a three-inch line for both GaAs and InP based FET for test equipment. In 2005, they realized a reduced gate length as 0.25 µm-GaAs FETs, 0.125 µm-GaAs pHEMTs, 2 µm-InGaP HBTs, and recently 1 µm-GaAs/Sb/InP DHBTs [Godin et al; 2005].

I.2 Properties of Material for MESFETs and HEMTs

I.2.1 GaAs Material

The light electron effective mass in GaAs (0.067 m_e) compared to that in Si (0.98 m_e longitudinal and 0.19 m_e transverse) leads to higher electron mobility in GaAs which is approximately 8500 cm^2/Vs at room temperature compared to Si (1500 cm^2/Vs). This provides a higher electron velocity. Under normal operating conditions, the electric fields are higher than the peak velocity field, which gives the GaAs the notable advantage especially for the short channel devices. Another consequence of the light mass for the GaAs electrons is

that they can undergo overshoot and ballistic transport [Shur and Eastman; 1979]. Since the electron transit time becomes equal to (or smaller than) the electron energy or even the momentum relaxation time, this boosts the electron velocity higher than the steady-state values [Golio; 1991].

The semi-insulating material is an important GaAs property which serves as substrate for MESFET or other devices fabrication. Thus, the GaAs materials offer the manufacturing ability of the MESFET and integrated circuits by direct implantation onto the semi-insulating GaAs substrate.

The direct band gap of the GaAs and related semiconducting is another advantageous property, widely used in optoelectronic applications. Hence, electronic and photonic devices can be integrated on the same chip for use in optical interconnects or in optoelectronic circuits. This characteristic leads to a high recombination rate, improving radiation hardness. GaAs based devices can survive over 100 megarads of ionizing radiation [Roosild; 1990]. Also because of the small intrinsic carrier concentration and high breakdown field make the GaAs a good material for power devices.

Table I.1: Comparison of the material properties of some semiconductors used in MESFET technology [Golio; 2001]. [*] [Heiblum et al; 1985], [**] [Levi et al; 1985]

Property	Si	GaAs	α-SiC(6H)	GaN
Energy gap (eV)	1.12	1.42	2.9	3.4
Lattice constant (a) A°	5.43107	5.6533	3.081	3.189
Lattice constant (c), A°	-	-	15.117	5.185
Density (g/cm^3)	2.329	5.3176	3.211	6.1
Dielectric constant	11.7	12.9	9.66($\perp$) 10.03($\parallel$)	9.5 [*, **]
Electron mobility (cm^2/Vs)	1450	8500	330	1200
Hole mobility (cm^2/Vs)	500	400	60	<30
Saturation velocity (m/s)	10^5	1.2×10^5	$2\text{-}2.5\times10^5$	$2\text{-}2.5\times10^5$
Electron effective mass ratio	0.92/0.19	0.067	0.25/1.5	0.22
Light hole mass ratio	0.16	0.076	0.33	0.7
Optical phonon energy (eV)	0.063	0.035	0.104	0.092
Thermal conductivity (W/cm°C)	1.31	0.46	4.9	1.5

I.2.2 $Al_xGa_{1-x}As$ alloys

The accuracy of a physical modelling methodology for a semiconductor device is governed by the quality of the physical information available. There has been a considerable amount of research [Adachi; 1985, Guigni and Tansley; 1992, Adachi; 1982, Kuo et al; 1985, Marzin et al; 1985, Park and Bernnan; 1989; Alamkan et al; 1990, Arent et al; 1989, Niki et al; 1989] directed over the last decade concerning the characterization of material parameters for a variety of heterojunctions.

The material parameters for the $Al_xGa_{1-x}As$ are based on the work of Adachi [Adachi; 1985]. The variation of bandgap E_g (eV), effective mass m^*, and dielectric constant ε_r as a function of Aluminum mole fraction x at room temperature are described by:

For $x \leq 0.45$

$$E_g = 1.424 + 1.25x + 0.143x^2 \quad \text{(I.1)}$$

$$m^* = (0.067 + 0.083x)m_0 \quad \text{(I.2)}$$

$$\varepsilon_r = 13.18 - 3.12x \quad \text{(I.3)}$$

The term m_0 is the mass of an electron at rest. A ratio of 65/35 [Guigni and Tansley; 1992] has been used for the band-edge-discontinuities (fraction of band-gap-difference in the conduction and valence bands), and the variation of conduction band-discontinuity for $Al_xGa_{1-x}As$ as a function of Aluminum mole fraction is given by:

$$V_h = 0.65(1.25x + 0.143x^2) \quad \text{(I.4)}$$

I.2.3 $In_{1-x}Ga_xAs_yP_{1-y}$ alloys

The $In_{1-x}Ga_xAs_yP_{1-y}$ compounds form crystals with the zinc blende arrangement. The lattice matching relations between the compositions x and y can be expressed as [Adachi, 1985]:

On InP substrate $$x \cong \frac{0.1894y}{0.4184 - 0.013y} (0 \leq y \leq 1) \quad \text{(I.5)}$$

On GaAs substrate $$x \cong \frac{1+y}{2.08} (0 \leq y \leq 1) \quad \text{(I.6)}$$

The lowest band gap E_0 for y=0 is

$$E_0 = 0.36 + 0.505x + 0.555x^2 \quad \text{(I.7)}$$

$$m^* = 0.080 - 0.039y \quad \text{(I.8)}$$

$$\varepsilon_r = 12.40 + 1.5y \quad \text{(I.9)}$$

In the case of the $Al_xGa_{1-x}As/In_yGa_{1-y}As/GaAs$ heterojunction, the strain dependent material parameters have been incorporated in the charge-control model [Singh and Snowden; 1999, Adachi; 1982, Kuo et al; 1985, Marzin et al; 1985, Park and Bernnan; 1989] and are given by the following form by [Alamkan et al; 1990]

$$E_{gs} = E_g - 2a\frac{C_{11}-C_{12}}{C_{11}}\Delta e_r + b\frac{C_{11}-2C_{12}}{C_{11}}\Delta e_r \quad \text{(I.10)}$$

$$m^* = m_0^* \cdot \frac{E_g + 2a[(C_{11}-C_{12})/C_{11}]}{E_g}\Delta e_r \quad \text{(I.11)}$$

$$\varepsilon_{rs} = \varepsilon_r e^{(-1.73\times10^{-11})P} \quad \text{(I.12)}$$

$$E_g = 1.424 + 1.25x - 1.501y + 0.143x^2 + 0.436y^2 \quad \text{(I.13)}$$

$$m_0^* = (0.067 + 0.083x - 0.076y)m_0 \quad \text{(I.14)}$$

$$\varepsilon_r = 13.18 - 3.12x - 1.6y \quad \text{(I.15)}$$

The variation of conduction band-discontinuity as function of the aluminium and indium contents given by

$$V_h = \Delta E_c = 0.7E_{gs} + 0.65(1.087.x + 0.438.x^2) \quad \text{(I.16)}$$

where

$C_{11} = (11.88 - 3.55y)10^{10}$ $\qquad$ $C_{12} = (5.37 - 0.84y)10^{10}$

$a = -0.84 - 2.4y$, $b = -1.7 - 0.1y$, $P = -\frac{2}{3}\Delta e_r(C_{11} + C_{12})/C_{11}$, and $\Delta e_r = \frac{0.405y}{5.6533+0.405y}$.

where C_{ij} are the elastic stiffness, a is the hydrostatic potential, and b is the shear deformation potential. E_{gs} is the heavy hole band-gap of strained $In_yGa_{1-y}As$, Δe_r is the relative difference in lattice constant and P is the equivalent hydrostatic pressure, while x and y are aluminium and indium content.

Arent [Arent et al; 1989] reported band-edge-discontinuities of $Al_xGa_{1-x}As/In_yGa_{1-y}As$ heterojunction varying from around 60/40 to 70/30 as y is varied from 0 to 0.3 with x set at 0.2. The ratio of conduction-band-discontinuity to the band-gap difference for strained layer pseudomorphic $In_yGa_{1-y}As/GaAs$ heterojunction is taken as 0.65 [Niki et al; 1989].

The material parameters such as permittivity and effective mass are functions of local energy-band structure and are position dependent quantities to account for the change in material across a heterojunction.

I.3 The GaAs MESFET technology

Most GaAs MESFETs for digital and sometimes in microwave applications are fabricated by ion implantation. The GaAs MESFET fabrication is a sequence process. Firstly, the semi insulating GaAs substrate is coated with a thin Silicon Nitride (Si_3N_4), and then a selective implantation defines the active channel region. The ohmic contacts (drain and source) are realized adjacent to the channel, by heavily and deeper dopant implant. This is realized by a self-aligned process represented in Figure I.1. The gate is covered by silicide (typically tungsten slicide) as a mask before implanting the ohmic contacts. Nevertheless, this method

mainly reduces the parasitic resistances; the gate leakage current is increased leading to the carrier injection into the substrate due to the n^+ implant [Eastman and Shur; 1979]. Afterwards, a subsequent annealing process is carried out. Finally, an insulator shelter is deposited on the GaAs surface.

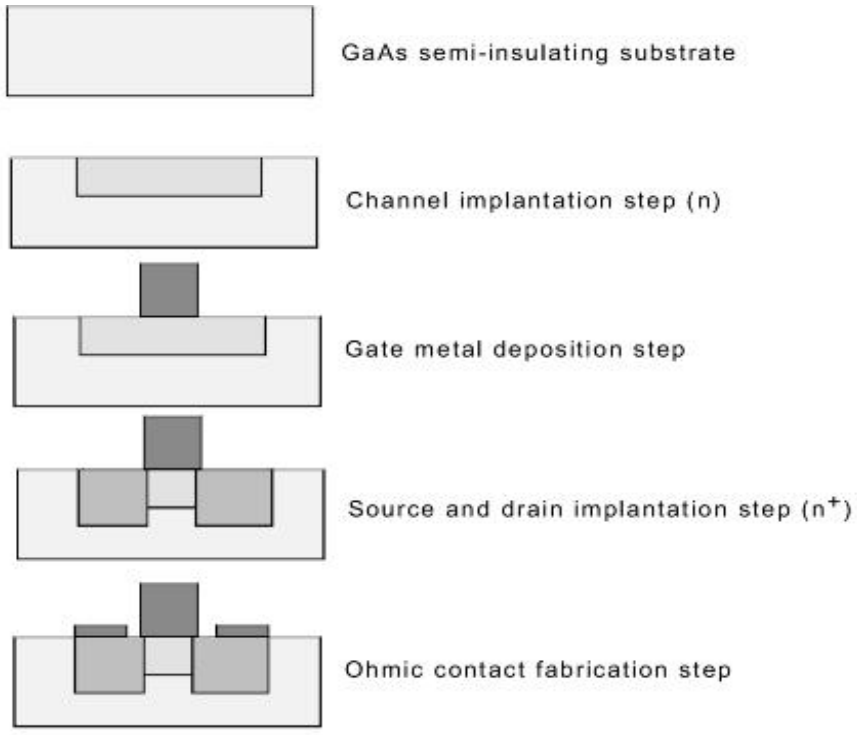


Figure I.1: Fabrication steps for self-aligned GaAs MESFET [Higgins et al; 1978, Welch and Eden; 1977].

For high performance electronic devices, and especially in microwave applications, the molecular-beam epitaxy is another standard technique for fabrication of GaAs MESFETs due to the control of the thickness and the impurity incorporation. In particular, this method is very useful for ultra short channel (0.25µm) low noise GaAs MESFET [Bandy et al; 1979]. An undoped GaAs buffer layer is used to separate the active channel from the substrate. The reduced active layer thickness heavily doped with silicon (n-type channel) leads to reduced series resistances. The formation of mesas is followed up by the liftoff technique using evaporated Au/Ge/Ni/Au in order to form the contact areas. The photolithographic process used to recess the channel layer and the gate metallization and overlay of Ti/W/Au are then deposited [Omori et al; 1989]. The top n^+ doping spread film from the source to the drain contacts reduces the series resistances [Golio; 2001]. The recessed gate position, depth and

geometric shape can improve the electric field distribution and the device breakdown [Omori et al; 1989, Ohata et al; 1980].

In power devices, the recessed gate is closer to the source than to the drain which may reduce the source parasitic resistance and enhances the drain-source breakdown voltage by allowing additional expansion space for the high-field region at the drain side of the gate. The mushroom gate (T-Shape) is also a way to reduce the gate series resistance without increasing the gate length, which determines the device cutoff frequency. The MESFET passivation by SiO_2 and Si_3N_4 films affects mainly the surface states and the surface depletion layer. The strain induced by the passivating dielectrics causes piezoelectric effects and tensile stress of the substrate [Chen et al; 1987]. Finally, it is worth to know that the wide band gap semiconductors, such as GaN and SiC are serious competitor with GaAs for applications in power electronic devices [Golio; 2001, Stanislaw; 2001].

I-4 GaAs MESFET operation

The most simple field effect transistor (FET) is the GaAs MESFET. It is a three terminal carrier device, which consists of two ohmic contacts (n^+: Source and Drain) separated by a Schottky barrier Gate contact. The single charge carriers (electrons) flow in the conducting channel formed between the source and the drain terminals. Under the gate, a generated depletion region thickness is controlled by the gate bias, thus, modulates the channel conductivity. This makes the MESFET as a voltage controlled resistor. Compared to the Metal Oxide Semiconductor Field Effect Transistor (MOSFET), where the silicon dioxide layer separates the gate from the active device, the GaAs compound semiconductor, does not have a stable oxide. A cross sectional view of two types of GaAs MESFET structures fabricated by (a) the epitaxial and (b) the ion-implantation technique are shown in Figure I.2. Basically, the GaAs MESFET structure consists of an GaAs active layer (channel) with a high n-dopant density $\approx 10^{17}\,cm^{-3}$, deposited on a high-resistivity buffer layer, which is grown on the undoped or p-doped (Cr) Semi-Insulating substrate, characterized by a typical high resistivity ($\rho \geq 10^7 \Omega.cm$). The buffer layer is added to prevent the out-diffusion of residual impurities from the substrate into the active layer.

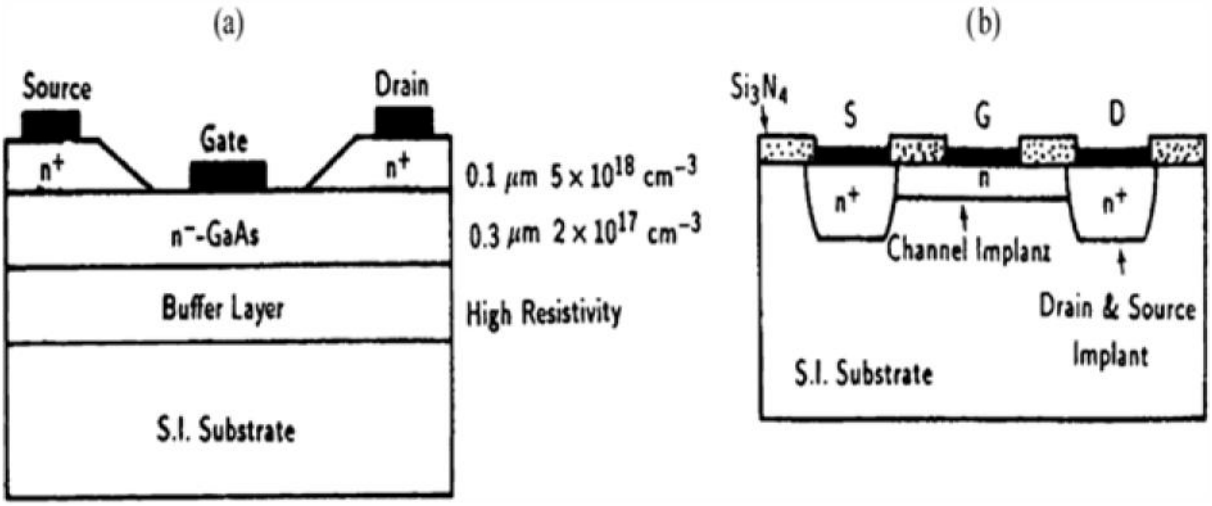


Figure I.2:Two widespeared GaAs MESFET methods (a) epitaxial and (b) ion implantation [Sheng; 2006].

The gate-channel junction behaves like a p^+n junction, and because of the built in voltage due to this junction, a depletion region is naturally formed. According to the built in voltage the device operates in the two forms presented by Figure I.3. In Normally-on (Depletion mode or D-MESFET), a depletion region does not cover all the channel, thus lets a finite conducting cross section to permit the electron flow even at zero gate bias. Under a sufficient negative voltage applied between the gate and the source a drain current cutoff may occur because of the depletion region widens such that it "pinches off" the channel. This is the pinch-off voltage.

On the other hand, Normally-off (Enhancement mode or E-MESFET), the depletion region is wide enough to pinch off the channel even without applying any bias. The threshold voltage at which the channel becomes conductive is positive (forward bias). The low open-up bias of Schottky-gate restricts the gate oscillation voltage, which constitutes the drawback of this operation mode. Thus, most GaAs MESFET are of the first type (D-MESFET).

In the main stream MESFET devices, the source is regularly grounded, whereas the drain is biased by a forward voltage. A schematic of the depletion region below the gate and under a finite drain voltage is shown in Figure I.4. Due to the additional reverse bias through the channel-gate junction supplied at the drain voltage, the depletion region is wider at the drain side. As the drain bias increases, the conducting area is again constricted mainly close to the drain until the saturation of the electrons velocity leading to saturate the current flow over the channel.

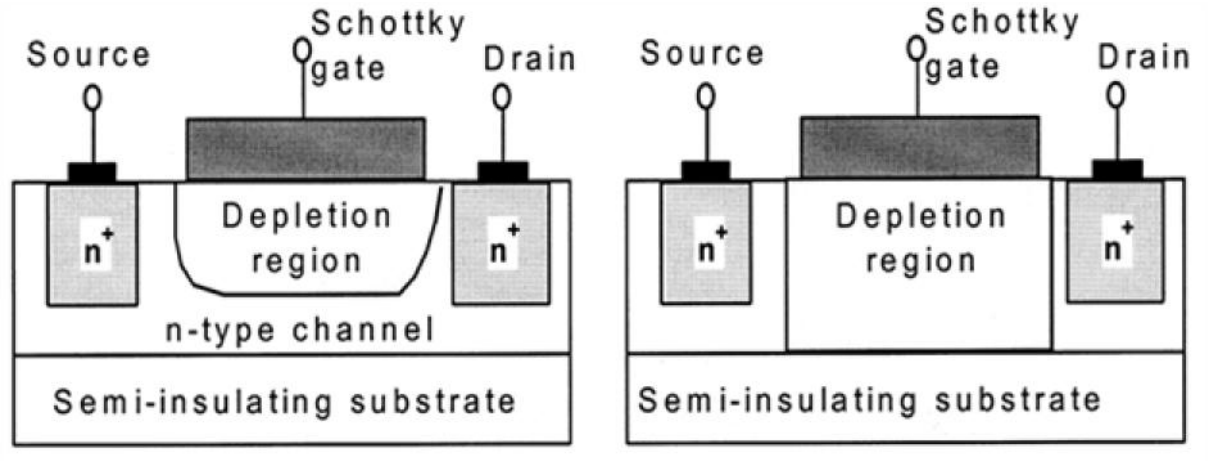


Figure I.3: Normally-on (a) and normally-off (b) MESFETs at zero gate bias [Yasuto; 2012].

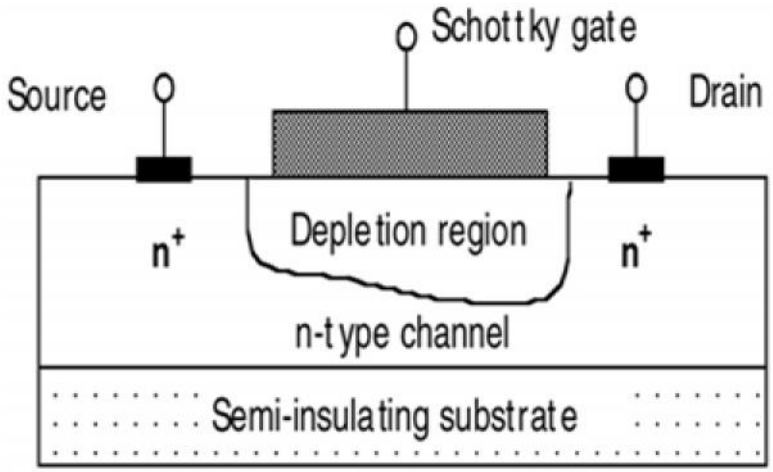


Figure I.4: Depletion region in MESFET with positive drain bias [Yasuto; 2012].

I.5 High electron mobility transistors

I.5.1 Introduction

The concept of modulation doping was first introduced in 1978 [Dingle et al, 1978] providing an attractive means of spatially separating the ionized donor atoms from the current-carrying electrons. The electrostatics of the heterojunction leads to the formation of a triangular well at the interface which confines the electrons in a two-dimensional electron gas (2DEG) [Golio; 2001]. Thus, the removal of the two-dimensional electrons gas 2DEG from the ionized donors mainly reduces the deleterious action of ionized impurity scattering. So, the free carrier concentration can be increased significantly without compromising the mobility.

The high-electron Mobility Transistor HEMT also called the Modulation Doped Field Effect Transistor (MODFET) which use the 2DEG as the current conducting channel have proved to

be excellent candidates for the main device in microwave and millimeter-wave analog and high speed digital applications [Golio; 2001]. Their rapid evolution has been due to the important advances in growth methods such as the Metal-Organic Chemical Vapor Deposition (MOCVD) and Molecular Beam Epitaxy (MBE). Advances in device processing techniques such as electron beam lithography have enabled the fabrication of feasible HEMTs with gate lengths down to 50 nm. A typical structure of a HEMT is shown in Figure I.5.

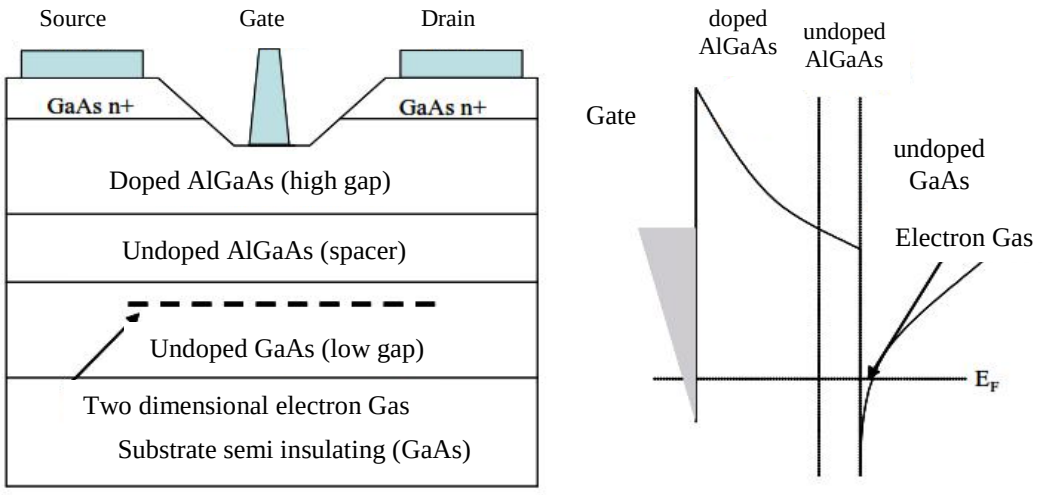


Figure I.5: The device structure of ordinary HEMT and the associated band energy diagram [Khlil; 2005].

The AlGaAs/GaAs material technology was the first HEMT demonstrated in1981 [Delagebeaudeuf and Linh; 1982] and considerable performance improvements over the GaAs MESFET at microwave frequencies were shown. Nevertheless, for millimeter frequencies operation, the high frequency achievement was not enough. The choice of the material system put in the highlight the possibility of manufacturing different kinds of HEMTs for microwave and millimeter-wave circuit applications, such as the AlGaAs/InGaAs pseudomorphic HEMT on a GaAs substrate [GaAs pHEMT] and the AlInAs/GaInAs HEMT on InP substrate [InP HEMT]

Previously, the HEMTs were not widely used, restricted to military and space-based electronic technology due to their high cost. Thereafter, the growth of wireless and optical fiber-based communication systems has opened up new and large applications especially those requiring high frequency, low noise and high gain.

I.5.2.1 Analytical description of HEMT operation

I.5.2.1 Linear charge control model

The current control mechanism in the HEMT controls the 2DEG density at the interface of heterojunction by the gate voltage. Figure I.6 shows the band diagram along the AlGaAs /GaAs interface. In equilibrium, a 2DEG region is formed at the AlGaAs/GaAs interface due to the conductance band discontinuities. A positive voltage applied to the gate increases the density of this 2DEG while a negative voltage reduces it.

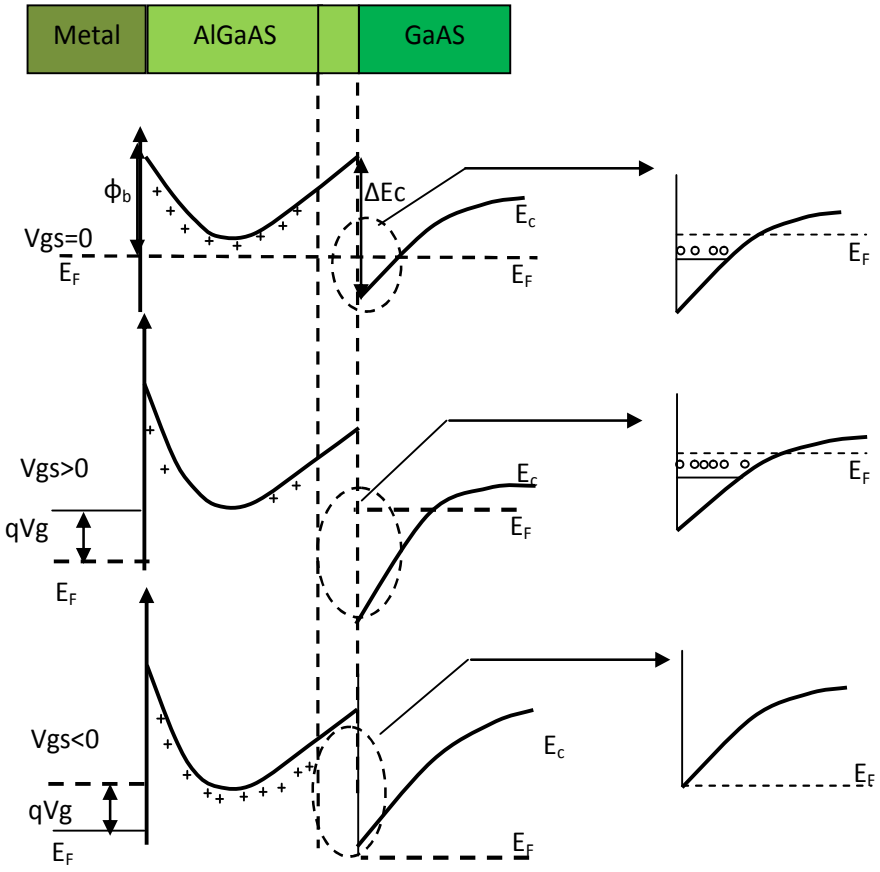


Figure I.6: Equilibrium and gate bias modulated conduction band diagram and 2DEG density of an AlGaAs/GaAs HEMT [Wang; 2008].

Delagebeaudeuf [Delagebeaudeuf and Linh; 1982] proposed a charge control model for the HEMT based on Poisson equation and given by the expression (I.17). At the interface of the AlGaAs/GaAs heterojuction, the potential has a triangular well shape, where the energy levels and the maximum (n_{sm}) 2DEG density can be evaluated from the Schrödinger equation in the triangular well and Poisson equation in AlGaAs donor layers [Drummond et al; 1986].

For $0 < n_s < n_{sm}$, the 2DEG carrier concentration n_s versus the gate bias V_{gs} can be expressed as [Delagebeaudeuf and Linh; 1982]:

$$n_s = \frac{C_s}{q}\left(V_{gs} - V_{th}\right) \tag{I.17}$$

where C_s is the 2DEG capacitance per unit area and is given by the following expression:

$$C_s = \frac{\varepsilon_s}{d_n + d_i + \Delta d} \tag{I.18}$$

ε_s is the permittivity of the AlGaAs material. Here Δd is the distance of the centroid of the 2DEG distribution from the AlGaAs/GaAs interface and is typically of the order of 80 Å for ~ 10^{12} cm^{-2}. d_i is the thickness of the undoped AlGaAs spacer. V_{th} the threshold voltage, is expressed as follows:

$$V_{th} = \emptyset_b - \frac{qN_d.d_n^2}{2\varepsilon_s} - \frac{\Delta E_c + E_F}{q} \tag{I.19}$$

$\emptyset_b$, N_d, and d_n are the Schottky barrier height on the donor layer, the doping density and the doped layer thickness, respectively. E_F is the Fermi level with respect to the conduction band edge in the channel layer and ΔE_c is the conduction band offset between the barrier and the channel. In the 2DEG, with respect to the bottom of the conduction band E_F dependence on its density is given by [Golio; 2001].

$$E_F = E_{F0}(T) + an_s \tag{I.20}$$

where E_{FO}(300K) = 0eV, E_{FO}(77K) = 0.025 eV, $a = 0.125 \times 10^{-16}$ V/m^2.

At room temperature, apart from the 2DEG charge density n_s, the gate voltage also modulates the free electrons n_{free} and the bound carrier density n_{bound} in the donor layer.

I.5.2.2 Modulation efficiency

Since the bound carrier density (n_{bound}) is modulated by the gate voltage which affect the carrier (electrons) conducting in the channel n_{free}, it produces a frequency dependence displacement current through the gate terminal [Foisy et al, 1988]. Nguyen [Nguyen et al; 1992] demonstrated that the charge modulation is a limiting mechanism in high frequencies. One of the interesting figures of merit of frequency performances of the HEMT is its cutoff-frequency (f_t). It is resulted to the modulation efficiency which is the ability of the gate voltage to modulate the drain current, thus, the cutoff frequency f_t can be expressed by [Foisy et al; 1988]:

$$f_t = \frac{v_{sat}}{2\pi l_g}\eta \tag{I.21}$$

η is the modulation efficiency which can express the ratio of the 2DEG charge change (δn_s) to that of the total charge Q_{tot}:

$$\eta = \frac{\delta q(n_s)/\delta V_{gs}}{\delta q(n_s+n_{bounds}+n_{free})/\delta V_{gs}} = \frac{C_s}{C_{tot}} \tag{I.22}$$

where v_{sat} is the saturation velocity and $C_{gs} = C_{tot}.l_g$ (l_g is the gate length).

The high frequency performance of HEMTs also leads to higher transconductance (g_m) thus, is also manifested in the transconductance expression given by:

$$g_m = \frac{\delta I_{ds}}{\delta V_{gs}} = \frac{\delta q(v_{sat}n_s)}{\delta V_{gs}} = q v_{sat}\frac{\delta n_s}{\delta V_{gs}} \tag{I.23}$$

$$g_m = 2\pi C_{gs} f_t = 2\pi C_{gs}\frac{v_{sat}}{2\pi l_g}\eta \tag{I.24}$$

I.5.2.3 Current-Voltage (I-V) models for HEMTs

By assuming linear charge control, gradual channel approximation, and a 2-piece linear velocity-field model, the expression for the saturated drain current I_{dss} in the HEMT is given by [Delagebeaudeuf and Linh; 1982]:

$$I_{dss} = C_s v_{sat}\left[\sqrt{(E_{cr}l_g)^2 + (V_{gs} - V_c(0) - V_{th})^2} - E_{cr}l_g\right] \tag{I.25}$$

E_{cr} is the critical electric field at which the electrons reach their saturation velocity and $V_c(0)$ is the channel potential at the source end of the gate.

For the HEMTs with long gate lengths, and before the onset of the donor charge modulation, this expression for the saturated drain current is valid and the intrinsic transconductance of the HEMT is obtained by differentiating the drain current with respect to the gate voltage and given as

$$g_{m0} = C_s v_{sat}\frac{V_{gs}-V_c(0)-V_{th}}{\sqrt{(V_{gs}-V_c(0)-V_{th})^2+(E_{cr}l_g)^2}} \tag{I.26}$$

In return, when the gate length of the HEMT is short, the electric field in the channel is considerably greater in magnitude than the critical electric field E_{cr}. Thus, if the entire channel operates in saturated velocity mode, the term (V_g–$V_c(0)$ – V_{th}) >> $E_{cr}.l_g$. Then, using equations

I.17, I.25 and I.26, the transconductance and the saturated drain current are reduced to the following expressions:

$$I_{dss} = qn_s v_{sat} \tag{I.27}$$

$$g_m = C_s v_{sat} \tag{I.28}$$

These formulas provide poor indication for the device design, so it is useful to take into account the equation I.17 where the 2DEG density depends on the gate bias; n_s is the fundamental parameter. By substitution in the expressions of I_{ds} and V_{gs}, we obtain the following expressions [Nguyen et al; 1992].

$$I_{dss} = qv_{sat} n_s \left(\sqrt{1 + \left(\frac{n_c}{n_s}\right)^2} - \frac{n_c}{n_s} \right) \tag{I.29}$$

$$g_m = C_s v_{sat} \frac{1}{\sqrt{1+\left(\frac{n_c}{n_s}\right)^2}} \tag{I.30}$$

where $n_c = \left(\frac{E_c C_s lg}{q}\right)$ and $0 < n_s < n_{sm.}$. By dividing both sides of equation I.30 by $(C_s v_{sat})$ the modulation efficiency is given by:

$$\eta = \frac{1}{\sqrt{1+\left(\frac{n_c}{n_s}\right)^2}} \tag{I.31}$$

Thus, the last three expressions ensure that maximizing the current, the transconductance and the modulation efficiency require maximizing the 2DEG density n_s.

I.5.3 Material systems for HEMTs

Extensive researches have been achieved in HEMT development and; the diversity of appropriate material systems for a particular devise application has been sounded out. Therefore, Table I.2 illustrates the relationship between the device parameters and the material parameters [Golio; 2001].

For the various constituent layers of the HEMT, namely the high bandgap donor and buffer layers, and the 2DEG channel. Figure I.7 shows a schematic diagram of a HEMT, illustrating the material requirements from each component layer.

Table I.2: The Device type and material parameters [Golio; 2001].

Device Type	Device Parameters	Material Parameters	
		2DEG Channel Layer	Barrier /Buffer Layer
Short Gate Length Devices	High Electron Velocity	High Electron Velocity High Electron Mobility	
Power Devices	High Aspect Ratio High Current Density Low Gate Leakage High Breakdown Voltage Low Output Conductance Good Charge Control Low Frequency Dispersion	High 2DEG Density High Breakdown Field High Modulation Efficiency	High Schottky Barrier High Breakdown Field High Quality Buffer
Low Noise Devices	Low R_s High Electron Velocity	High 2DEG density High Electron Velocity High Electron Mobility	
Digital Devices	Low Gate Leakage Current High Current Drive	High 2DEG Density	High Schottky Barrier

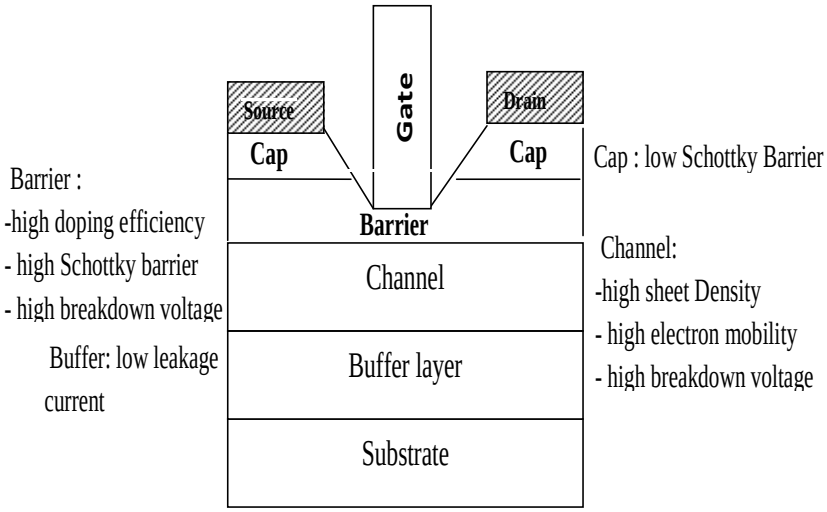


Figure I.7: Material requirements for HEMT devices [Golio; 2001].

The AlGaAs/GaAs HEMT demonstrated significant improvement in low noise and power performance over GaAs MESFET due to superior electronic transport properties of the 2DEG at the AlGaAs/GaAs interface and better scaling properties. However, the limited band discontinuity at the AlGaAs/GaAs interface limits the 2DEG density. Other undesirable effects, such as formation of a parasitic MESFET in the donor layer and real space transfer of electrons from the channel to donor, are prevalent.

One way to increase band discontinuity is to increase the Al composition in AlGaAs. However, the presence of deep level centers (DX centers) associated with Si donors in AlGaAs prevents the use of high Al composition AlGaAs donor layers to increase the band discontinuity and also limits doping efficiency.

Problems relating to low band discontinuity can also be solved by reducing the bandgap of the channel, and by using a material that has higher electron mobility and electron saturation velocity. The first step in this direction was taken by the implementation of an AlGaAs/InGaAs pseudomorphic HEMT (GaAs pHEMT) [Ketterson, 1986]. In an AlGaAs/InGaAs pHEMT the electron channel consists of a thin layer of narrow bandgap InGaAs that is lattice mismatched to GaAs by 2%. The thickness of the InGaAs channel is thin enough (~200 Å) so that the mismatch strain is accommodated coherently in the quantum well, resulting in a dislocation free "pseudomorphic" material. However the indium content in the InGaAs channel can be increased only up to 25%. Beyond this limit the introduction of dislocations due to high lattice mismatch degrades the electronic properties of the channel. The maximum Al composition that can be used in the barrier is 25% and the maximum indium composition that can be used in the channel is 25% [Ketterson; 1986].

Using the $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ material system lattice matched to InP can simultaneously solve the limitations of the high bandgap barrier material and the lower bandgap channel material. The AlInAs/GaInAs HEMT (InP HEMT) has demonstrated excellent low-noise and power performance that extends well into the millimeter-wave range. The GaInAs channel has high electron mobility (> 10,000 cm /Vs at 300°K), high electron saturation velocity (2.6×10^7 cm/s) and higher inter-valley (Γ-L) energy separation. The higher conduction band offset at the AlInAs/GaInAs interface (ΔE_c = 0.5 eV) and the higher doping efficiency of AlInAs (compared to AlGaAs) results in a 2DEG density that is twice that of the AlGaAs/InGaAs material system. Higher doping efficiency of AlInAs also enables efficient vertical scaling of short gate length HEMTs. The combination of high 2DEG density and electron mobility in the channel results in low source resistance, which is necessary to achieve high transconductance. However, the low bandgap of the InGaAs channel results in low breakdown voltage due to high impact ionization rates.

Table I.3 summarizes the material properties of the three main material systems used for the fabrication of HEMTs. The emergence of growth techniques like MOCVD and MBE has enabled a new class of phosphorus based material systems for fabrication of HEMTs.

Table I.3: Material Parameters of the three main materials used in manufacturing of the HEMT AlGaAs/GaAs, AlGaAs/InGaAs, and AlInAs/GaInAs material systems [Golio; 2001].

Material Parameter	AlGaAs/GaAs	AlGaAs/InGaAs	AlInAs/GaInAs
ΔEc (eV)	0.22	0.42	0.51
Maximum donor doping(cm^{-3})	5×10^{18}	5×10^{18}	1×10^{19}
Sheet charge density (cm^{-2})	1×10^{12}	1.5×10^{12}	3×10^{12}
Mobility (cm^2/Vs)	8000	6000	12,000
Peak Electron Velocity (cm/s)	2×10^7		2×10^7
Γ-L valley separation (eV)	0.33		0.5
Schottky Barrier (eV)	1.0	1.0	0.45

On the GaAs substrate, the GaInP/InGaAs has emerged as an alternative to the AlGaAs/InGaAs material system. GaInP has a higher bandgap than AlGaAs and hence enables high 2DEG densities due to the increased conduction band discontinuity (ΔE_c) at the GaInP/InGaAs interface. As GaInP has no aluminum it is less susceptible to environmental oxidation. The availability of high selectivity etchants for GaAs and GaInP simplifies device processing. However, the high conduction band discontinuity is achieved only for disordered GaInP, which has a bandgap of 1.9 eV. Using graded GaInP barrier layers and an $In_{0.22}Ga_{0.78}As$ channel, 2DEG density as high as 5×10^{12} cm^{-2} and a mobility of 6000 cm^2/Vs was demonstrated [Pereiaslavets; 1996].

On InP substrates, the InP/InGaAs material system can be used in place of the AlInAs/GaInAs material system. The presence of deep levels and traps in AlInAs degrades the low frequency noise performance of AlInAs/GaInAs HEMT. Replacing the AlInAs barrier by InP or pseudomorphic InGaP can solve this problem. One disadvantage of using the InP-based barrier is the reduced band discontinuity (0.25 eV compared to 0.5 eV for AlInAs/GaInAs) at the InP/InGaAs interface. This reduces 2DEG density at the interface and modulation efficiency. Increasing the indium content up to 75% in the InGaAs channel can increase the band discontinuity at the InP/InGaAs interface. The poor Schottky characteristics on InP necessitate the use of higher bandgap InGaP barrier layers or depleted p-type InP layers. A 2DEG density of 3.5×10^{12} cm^{-2} and mobility of 11,400 cm^2/Vs was demonstrated in an InP/InAs/InP double heterostructure [Mesquida-Kusters; 1997].

Despite the large number of material systems available for fabrication of HEMTs, the GaAs pHEMT implemented in the $Al_xGa_{1-x}As/In_yGa_{1-y}As$ ($x \sim 0.25$; $y \sim 0.22$) material system and

the InP HEMT implemented in the $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ material system have emerged as industry vehicles for implementation of millimeter-wave analog and ultra high-speed digital circuits.

I.5.3.1 AlGaAs/(In)GaAs/GaAs (GaAs pHEMT)

Firstly demonstrated by Ketterson [Ketterson; 1985], the AlGaAs/InGaAs pHEMT exhibits significant performance improvement over AlGaAs/GaAs HEMT. The high dc transconductance (270 mS/mm) [Ketterson; 1986], and maximum drain current density (290 mA/mm) were observed for the 1µm gate length and 3 µm channel thickness. Shrinking the gate length gives more interesting performance as for 0.2 µm ($In_{0.25}Ga_{0.75}As$ channel) devices, the cutoff frequency f_t was about 120 GHz [Nguyen; 1988] and for 0.1µm devices an f_{max} of 270 GHz [Chao;1989].

Using the GaAs pHEMT as premier FET for implementing microwave and millimeter-wave power amplifiers takes effort to reach high output power density. Since high current density and consequently, higher 2DEG are required performances for the device structures, increasing the 2DEG density in single heterojunction AlGaAs/InGaAs is limited to 2.3×10^{12} cm^{-2}. Thus, a double heterojunction (DH) presents a solution to increase it. In order to introduce the carries of the DH devices in the channel (InGaAs), atomic planar doping method is used to dope both layers (AlGaAs) sides of the channel with silicon to increase the electron transfer efficiency. Thus, reaching a charge density of 3.5×10^{12} cm^{-2} and a mobility of 5000 cm^2/Vs leads to higher current drive and power handling capability. Figure I.8 shows the layer structure of a typical millimeter wave power GaAs pHEMT. In some cases, a doped InGaAs channel is also used to increase the 2DEG density [Smith; 1989, Streit, 1991].

To increase the drain efficiency, voltage gain, and power added efficiency (PAE), the breakdown voltage has to be higher, which involves intensive approaches. The breakdown mechanism of a GaAs pHEMT can be either at the surface in the gate-drain of the device or in the channel (due to impact ionization). Among the approaches used to increase the breakdown voltage of a GaAs HEMT, the planar doping of AlGaAs barriers serve to keep a high breakdown voltage. Knowing that the AlGaAs barrier is generally not doped, using a low temperature grown (LTG) GaAs buffer below the channel creates another possibility to increase the breakdown voltage. In consequence of this approach, a 45% increase in channel breakdown voltage with a 12% increase in output power was achieved [Actis; 1995]. Accommodating the electric field in the gate-drain depletion layer by utilizing a double recessed gate is also a means of increasing the breakdown voltage. The electric field reduction

close to the gate by surface states in the exposed recess region is able to increase the breakdown voltage [Huang; 1993].

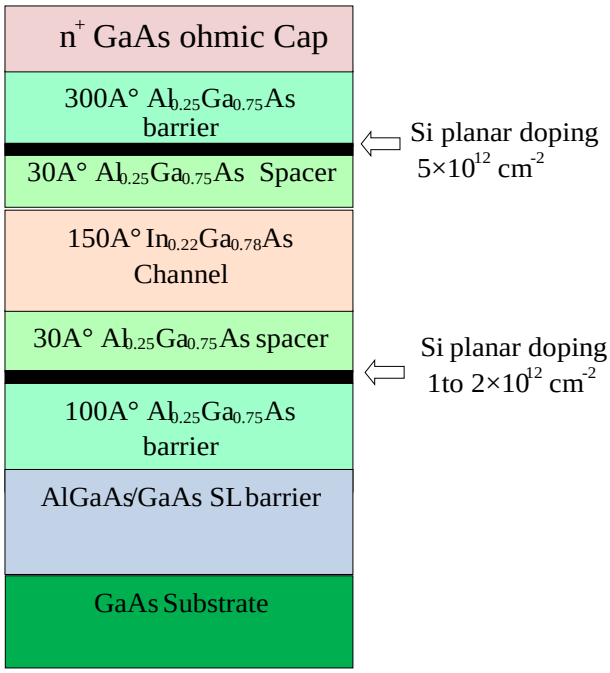


Figure I.8: The Power GaAs pHEMT [Golio; 2001].

I.6 Comparative study of HEMT, pHEMT and MESFET

GaAs-based devices and circuits have a well-defined place in commercial and defense applications as evidenced by their use in a variety of products and systems. Applications extend from the low-frequency spectrum of several hundred MHz to the millimeter wave range. The choice of a device is influenced by its maturity in terms of manufacturing but also by other criteria, which are related to fundamental operation mechanisms and determine the performance. Although MESFETs have for long been considered as most mature components, HEMT technology made significant advances because of the extensive understanding of both III-V and Si manufacturing approaches. From the basic considerations regarding the properties of HEMTs/pHEMTs and MESFETs and the relative merits of each technology, a brief comparative study will be done in this section.

I.6.1 Low-noise applications

For low-noise amplifier applications, the pHEMT is believed to be the best choice followed up by the MESFET. Since at high frequencies, the principal source of noise in FETs thermal-diffusion type (mainly related to power dissipation in the internal device resistances). This leads to random variations in carrier speed in channel and hence carried over to current variations and thus, noise. At lower frequencies, generation/recombination processes become dominant. General dependencies of F_{min} on device parameters can be obtained from Fukui's equation [Fukui; 1979] as follow:

$$F_{min} \approx 1 + .2\sqrt{K_f}\left(\frac{2\pi f}{g_m} C_{gs}\right)\sqrt{g_m\left(R_g + R_s\right)} \qquad \text{(I.32)}$$

where f is the frequency of operation and K_f a fitting factor originally derived experimentally for GaAs MESFETs and found to be ≈ 2.5 [Fukui; 1979].

Of particular importance is the presence of capacitive coupling between the gate and the channel, which results in the overall noise being determined by subtracting part of the gate noise from the drain noise. This is a unique property of FETs, which leads to very low-noise performance. Best noise performance is obtained by minimizing the source access resistance and maximizing the current gain cutoff frequency, f_t. This necessitates to design the device for maximum transconductance g_m and minimum gate capacitance C_{gs}, conditions that can, to some extend, also be controlled by proper bias choice.

The equation can be also used for a qualitative discussion of the noise of HEMTs minimum noise, $F_{min,}$ [Lugli et al; 1996], obtained under ~I_{dss} /10 conditions. There is, however, a difference in the bias range necessary for this purpose in MESFETs and HEMTs; HEMTs appear to have a broader range of I_{ds} values than MESFETs over which F_{min} is achieved. This provides a larger margin in LNA circuit design. Since high gain is in general desired for amplifiers, and bias for F_{min} does not often coincide with bias for maximum gain, a trade-off is often made in gain *vs*. noise. This turns out to be less severe in HEMTs due to their broader range of bias for F_{min}. Large gain also requires device designs with a heterojunction or other type of buffer below the channel to minimize carrier injection and reduce the output conductance. An analysis of noise characteristics also shows that pHEMTs offer smaller bias sensitivity of noise performance than MESFETs. Figure I.9 summarizes the noise performance of various device types as a function of frequency.

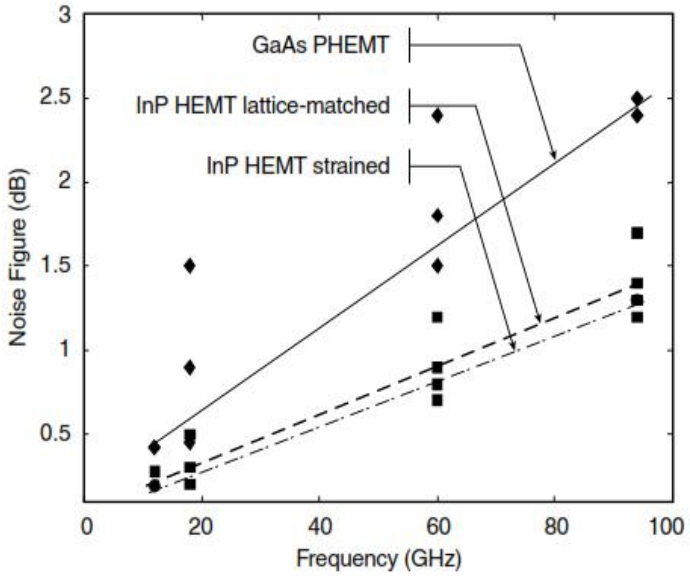


Figure I.9: Noise performance of GaAs- and InP-based HEMTs as a function of frequency [Pavlidis; 1999, Itoh et al; 2001].

Table I.4 summarizes the HEMT applications for various frequency bands. As shown by this table, the uses of the GaAs pHEMT overcame in all broad band applications.

Table I.4: HEMT applications for various frequency bands [Golio; 2008]

Frequency	Military/Space	Commercial	Device Technology
850 MHz–1.9 GHz		Wireless Low noise	Low noise –GaAs pHEMT Power – GaAs pHEMT
12 GHz (Ku-Band)	Phased array radar	Direct broadcast satellite	Low noise – GaAs pHEMT Power – GaAs pHEMT
20 GHz (K-Band)	Satellite downlinks		
27–35 GHz (Ka-Band)	Missile seekers	LMDS - Local multipoint distribution system	Low noise – GaAs pHEMT Power – GaAs pHEMT
44 GHz (Q-Band)	SATCOM ground terminals	MVDS - Multipoint video distribution system	Low noise – InP HEMT Power – GaAs pHEMT
60 GHz (V-Band)	Satellite crosslinks	Wireless LAN	Low noise –InP HEMT Power –GaAs pHEMT/InP HEMT
77 GHz	Collision avoidance radar		Low noise –InP HEMT Power –GaAs pHEMT/InP HEMT
94 GHz (W-Band)	FMCW radar		Low noise –InP HEMT Power –InP HEMT
100–140 GHz	Radio astronomy		Low noise –InP HEMT
Digital 10 Gb/s		Fiber-optic communication	GaAs pHEMT
Digital 40 Gb/s		Fiber-optic communication	InP HEMT

I.6.2 Microwave Power Applications

The GaAs pHEMT and the InP HEMT are the two major competing technologies for microwave and millimeter-wave power amplifiers. The relation between output power density $P_{out,}$ and power-added efficiency, *PAE*, and device parameters is given by the following expressions:

$$P_{out} = \frac{1}{8}(I_{max})(BV_{gd} - V_{knee}) \tag{I.33}$$

$$PAE = \alpha\left[\frac{V_{dd}-V_{knee}}{V_{dd}}\right]\left(1-\frac{1}{G_a}\right) \tag{I.34}$$

In equation I.34, α is 1/2 for Class A operation and $\pi/4$ for Class B operation. Figure I.10 compares the P_{out} and *PAE* of GaAs pHEMTs and InP HEMTs as a function of operating frequency. It can be seen that GaAs pHEMTs have a higher power density than InP HEMTs. This is due to higher breakdown voltages, BV_{gd}, in GaAs pHEMTs that enables higher operating voltage, V_{dd}. The InP HEMT operating voltage is limited by the low breakdown voltage, hence the power output is low. However, InP HEMTs have comparable power output at millimeter-wave frequencies. This is enabled by the low knee voltage, $V_{knee,}$ and high current drive, I_{max}. On the other hand, due to their low knee voltage and high gain, G_a, InP HEMTs have higher gain and *PAE* at frequencies exceeding 60 GHz. The potential of InP HEMTs as millimeter-wave power devices is evident in the fact that comparable power performance can be achieved at drain biases 2 to 3 V lower than those for GaAs pHEMTs. Hence a high voltage InP HEMT technology should be able to outperform the GaAs pHEMT for power applications at all frequencies.

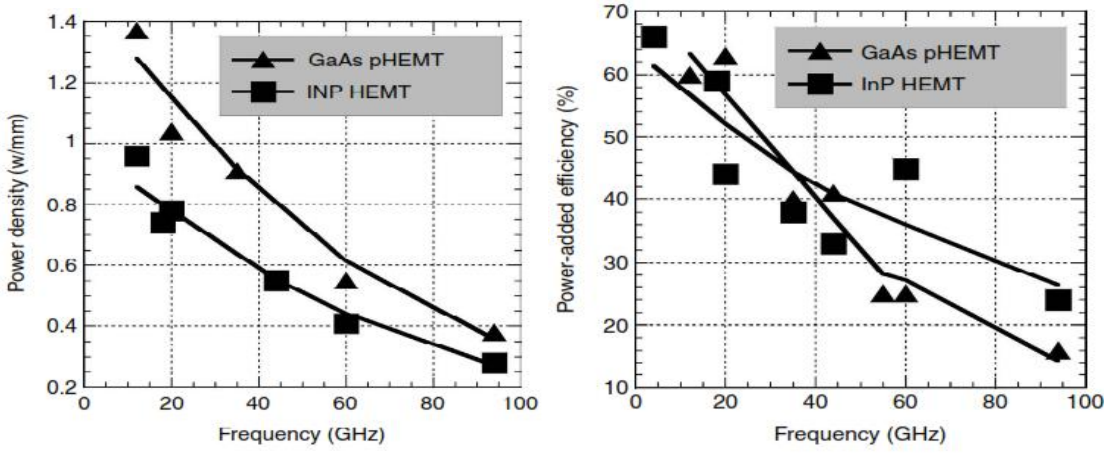


Figure I.10: Comparison of output power density and power-added-efficiency of GaAs pHEMTs and InP HEMTs as a function of frequency [Golio; 2008].

From the technological point view, the use of heterojunctions opens new possibilities in optimizing device performance. AlGaAs/GaAs HEMTs allow higher frequency of operation than MESFETs. These devices are, however, limited in terms of sheet carrier n_s (10^{12} cm^{-3}) and thus, in terms of current and power, due to their small conduction band discontinuity ΔE_c. Despite this limitation, 100 W of power have been obtained at 2.1 GHz using a 86.4 mm gate HEMT [Goto; 1998] Improved performance can be obtained by adding heterojunction channels or increasing ΔE_c. The first leads to higher overall n_s, without compromising in breakdown since the doping of individual channels remains the same. The second can be realized using the so-called pseudomorphic pHEMT approach where the GaAs channel is replaced by $In_xGa_{1-x}As$. The pHEMTs have n_s values of at least (4×10^{12} cm^{-3}) and therefore currents exceeding 1A/mm can be achieved. A power exceeding 2.8 W (34.5 dBm) and power added efficiency of 23 to 26% has been obtained over 42 to 46 GHz frequency range using a 0.15 µm gate device [Aust et al; 2005]. Further n_s and thus I_{ds} improvement can be obtained by fabricating HEMTs on InP substrates. This technology offers the additional advantage of higher thermal conductivity for InP substrates. InP substrates and the related technology is, however, less mature than GaAs. Most popular among all devices for power applications is the pHEMT. In order to have further improvements in pHEMT performance, it can be envisaged to use double and asymmetric recess. Figure I.11 summarizes the power performance of pHEMTs, MESFETs and HBTs.

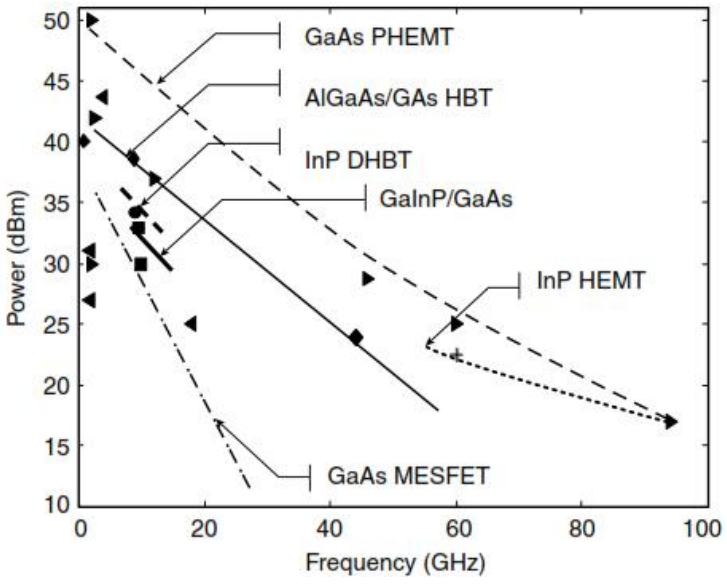


Figure I.11: Power performance of HEMTs, MESFETs and HBTs as a function of frequency [Pavlidis; 1999, Itoh et al; 2001].

I.7 Summary

In this chapter, an overview of GaAs based MESFETs and HEMTs material and their parameters expressions were given. The GaAs MESFET operation was first described then the HEMT functionality principle was detailed in its analytical description. The HEMT structure was constructed in lattice matched GaAs-based AlGaAs system, then, additional material systems including pseudomorphic HEMT have also been described to achieve higher operating frequencies and lower noise. First, the 2DEG charge density can be controlled by applying an appropriate bias voltage. Thereafter, the cutoff frequency, the transconductance, and the current-voltage expressions related to the 2DEG were given. Then, the material systems for the HEMTs were given to reveal the relationship between the device and the material parameters. From both technological and application points of view, a brief comparative study has been achieved concerning the MESFET, HEMT and (GaAs.*vs.*InP) pHEMT. Millimeter-wave power modules have been demonstrated using GaAs pHEMT devices. The superior device performance of GaAs pHEMTs is being used to improve the performance of power amplifiers. Consequently and for the raisons given above, and since we limited our study to frequencies less than 60 GHz, the GaAs MESFETs and GaAs based pHEMT will be chosen as sample devices.

Chapter II

Physical Modelling of Field Effect Transistors

II.1 Introduction

Research in the field of GaAs High Electron Mobility Transistors (HEMTs) for microwave systems has increased dramatically in the recent years [Kärnfelt et al; 2006]. Improved performance requires an extensive physical and electrical modelling to accurately predict the device response. Physical modelling is a useful tool to optimize the device structure and to tailor the FET characteristics for specific applications and curtail the manufacture cost. Thus, physical modelling has become an unavoidable step [Curtice; 1989].

The main limitations of FET devices and the effects of the channel parameters upon circuit performance can be indeed assessed from a physical point of view. In fact, modelling of the I-V transistor characteristics can be affected by many physical parameters [McNally and Daniels; 2001]. Three of the most significant hurdles are: (i) velocity overshoots which occur when the electrons found themselves in high electric field region which can cause the current to saturate earlier; (ii) effective threshold voltage displacement which is a particular problem at short gate lengths and as the gate-source voltage increases; and (iii) non-zero drain conductance which again comes into consideration when the device gate length is short [Streetman and Banarjee; 2000]. Thus, it is important to understand the physical mechanisms underpinning short-channel microwave FET operation.

Moreover, the high operating frequencies of computing and telecommunication equipment [Tsai et al; 2000]; as well as growing interest for priori design methods have driven the research effort towards a possibly complete, and accurate physical-based modelling approach. In fact, taking into account the charge transport physics for electrons and holes and their time-domain behavior, these models require two or three- dimensional internal models of the FET [Curtice; 2010].

The major interest of the physical modelling of microwave and millimeter wave circuits is to focus more on the device physics rather than on the circuit functionality. It is based on the simulation of Maxwell's semiconductor transport equations. At high frequencies, the period of the propagating wave is small enough to be comparable to the electron relaxation time and the electrons require a finite time to adjust their velocities under the fields' variations. In this situation, electron transport is seriously and directly affected by the wave propagation inside the transistor [Alsunaidi et al; 1996, Sohel Imtiaz and El-Ghazaly; 1998]. Furthermore, due to

the continuous scaling into the deep submicron regime [Feng and Hintz; 1988], neither internal nor external characteristics of state-of-the-art FETs can be properly represented by the conventional drift-diffusion transport (DDT) model. For example, the drift-diffusion method does not reproduce velocity overshoot and often overestimates the impact ionization generation rates [Shestakov et al; 2008]. This is because the DD Model does not take account of some effects such as the momentum and energy relaxation times of the electron gas that are close to the picosecond range.

On the other hand, the hydrodynamic model can take the above mentioned phenomena into account, giving better results than the DDM. The hydrodynamic model involves the solution of four coupled nonlinear partial differential equations (PDEs) as will be detailed later. The full accounting of the changing fields inside the device is possible.

II.2 Two Dimensional Hydrodynamic FET Model

II.2.1 Model Description

The physical model used in this work is a hydrodynamic approach based on the conservation equations derived from the Boltzmann transport equation. The fundamental semiconductor equations can be divided into two main groups namely, electromagnetic and charge transport. The first group requires only Poisson's Equation for low frequency simulation, since the terms in the remaining electromagnetic equations are negligibly small. Poisson's equation relates the local electrostatic potential to the charge distribution throughout the device. As the operational frequency rises to microwave frequencies, the displacement current, which will be defined later, becomes important; hence this term is included in all time-domain simulations.

Carrier transport is described using the Boltzmann Transport Equation (BTE). An explicit solution of the BTE uses the moments method, which splits the BTE into a system of conservation equations. The first three conservation equations relate to particle, momentum, and energy. Full description of these methods is presented in Appendix A.

For DC operation: particle, momentum, and energy conservation equations are solved self-consistently with Poisson's equation. These are supplemented by displacement current when the device is operated in time-domain mode. The secondary equations describing the dependent variables including Schrodinger's equation, carrier population statistics, impurity ionization, carrier mobility, and energy relaxation effects are taken into account by this model.

II.2.2 Poisson' equation

The Poisson's equation is derived from Maxwell's equations and correlates the electrostatic potential to the charge distribution as [Sze; 1981, Simlinger et al; 1997]:

$$\nabla(\varepsilon_0\varepsilon_r\nabla\varphi) + q(N_D^+ - N_A^- + p - n + T_D^+ - T_A^-) = 0 \quad \text{(II.1)}$$

where q is the elementary charge, $\varepsilon_0, \varepsilon_r$ are the free space and relative permittivity, respectively, φ is the electrostatic potential, n and p are the electron and hole density respectively, N_D^+, N_A^- are the ionized donor and acceptor dopant, respectively, while T_D^+ and T_A^- are the ionized trap densities. Thus, the electric field ($\vec{E}$) can be deduced from:

$$\vec{E} = -\nabla\vec{\varphi} \quad \text{(II.2)}$$

Poisson's equation is solved first to acquire the initial guess on the potential profile throughout the device.

II.2.3 Carrier statistics

Once the potential profile is obtained, the free carrier densities can be evaluated. The total free charge concentration in the device is calculated by performing an integral over energy of the density of states *g(E)* with probability of occupation *f(E)* where *E* is energy [Sze; 1981, Markowich et al; 1990].

$$n = \int_0^\infty g(E).f(E)dE \quad \text{(II.3)}$$

The probability of occupation is described using either Boltzmann or Fermi-Dirac statistics given by equations II.4 and II.5 [Sze; 1981, Markowich et al]:

Boltzmann:

$$f(E) = \exp\left\{\frac{(E_F - E)}{K_B T}\right\} \quad \text{(II.4)}$$

Fermi-Dirac:

$$f(E) = 1/\left(1 + \exp\left\{\frac{(E - E_F)}{K_B T_L}\right\}\right) \quad \text{(II.5)}$$

where E_F is the electron Fermi Level, K_B is the Boltzmann constant and T_L is the lattice temperature.

In the limit when $E\text{-}E_F >> k_B T_L$ the Fermi-Dirac expression reduces to the Boltzmann statistics. The density of states can be expressed using the effective mass approximation [Sze; 1981].

$$g(E) = \frac{4\pi(2m_c)^{3/2}}{h^3}.\sqrt{E - E_F} \quad \text{(II.6)}$$

where m_c is the free carrier (conduction band) effective mass and h is Plank's constant. As the device scale length approaches or falls below 50 nm the classical description can become inaccurate and quantum mechanics may be necessary to accurately model the charge [Mercury; 2004].

Since the density of states becomes dependent upon the energy band structure and the material can no longer be considered isotropic, the calculation of the quantized density of states relies upon a solution of the Schrodinger equation as [Lundstrom; 2000, Mercury; 2004]:

$$\nabla\left(\frac{1}{m_c}\nabla\zeta_k\right) + U_{tot}\zeta_K = \lambda_K\zeta_K \quad \text{(II.7)}$$

where ζ_K and λ_K are the k^{th} bound state, wave function and energy level respectively. U_{tot} is the total potential energy of electron $U_{tot} = q\varphi + E_H$ and E_H is the conduction band heterojunction discontinuity given by the difference in electron affinities. Thus, the quantized density of states has the form [Mercury; 2004, Madou; 2011]:

$$g(E)_{quantum} = \begin{cases} \left.\frac{4\pi m_c|\zeta_K|^2}{h^2}\right|_{E=\lambda_K} \\ \left. 0\right|_{E\neq\lambda_K} \end{cases} \quad \text{(II.8)}$$

Using Fermi-Dirac statistics, the discrete nature of the quantized density of states reduces the integral over energy (equation II.3), to a sum over bound-state energies:

$$n = N_{c2D}\sum_{K=1}^{K_{max}}|\zeta_K|^2 log\,(1 + exp\,(\frac{E_F - \lambda_K}{K_BT}) \quad \text{(II.9)}$$

N_{c2D} is a constant density of states for a given effective mass and temperature

$$N_{c2D} = 2(\frac{2\pi m_c K_B T}{h^2}) \quad \text{(II.10)}$$

The ionized impurity density is calculated using Fermi-Dirac statistics including the dopant ionization energy, E_D and E_A, together with appropriate degeneracy factors G_D and G_A for the conduction and the valence bands, respectively,

$$N_d^+ = N_d/(1 + G_D exp\left\{\frac{(E_c - E_D - E_F)}{K_BT}\right\}) \quad \text{(II.11)}$$

$$N_A^- = N_a/(1 + G_A exp\left\{\frac{(E_F - E_v - E_A)}{K_BT}\right\}) \quad \text{(II.12)}$$

where E_c and E_v are the conductance and the valence band energy respectively.

II.2.4 Hydrodynamic transport equations

Using only the current continuity equations in classical modelling of carrier transport in the device is no longer accurate when the device scale lengths drop into the ultra-submicron regime. The alternative hydrodynamic approach is therefore adopted where the carrier, momentum, and energy balance equations are solved self-consistently with Poisson's equation [Sandborn; 1989, Caughey and Thomas; 1967, Littlejohn; 1977, Buturla and Cotrell; 1980, Katayama; 1989, Lombardi et al; 1988, Klaassen; 1992(a), Klaassen; 1992(b), Zhou; 1992, Zhou; 1996, Cassi and Ricco; 1990, Wada et al; 1981].

Firstly, the three moments of the Boltzmann Transport Equation (BTE) are given. The conservation equations can be derived for the i^{th} valley in the semiconductor as follows:

- **The particle equation**

$$\frac{\partial n_i}{\partial t} + \nabla(n_i \vec{v}_i) = \left(\frac{\partial n_i}{\partial t}\right)_{coll} \tag{II.13}$$

- **The momentum balance equation**

For negligible charge carrier generation and recombination

$$\frac{\partial \vec{v}_i}{\partial t} + \vec{v}_i \nabla \vec{v}_i + \frac{q\vec{\mathcal{E}}}{m_i} + \frac{1}{m_i n_i} \nabla(n_i K_B T_i) = -\left(\frac{\partial \vec{v}_i}{\partial t}\right)_{coll} \tag{II.14}$$

- **The energy balance equation**

$$\frac{\partial w_i}{\partial t} + \vec{v}_i \nabla w_i + q\vec{v}_i \mathcal{E} + \frac{1}{n_i} \nabla(n_i \vec{v}_i K_B T_i) + \nabla(\vec{q}_i) = \left(\frac{\partial w_i}{\partial t}\right)_{coll} \tag{II.15}$$

Here $w_i = \frac{3}{2} K_B T_i + \frac{1}{2} m_i v^2$ and $\vec{q}_i = -k_i T_i$. n_i, $\vec{v}$ and w, are the electron concentration, average velocity and average energy, respectively. *Q* is the heat flow and *coll* is abbreviation of collision.

The single electron gas approach can accurately simplify these equations [Sandborn et al; 1989], where the individual valley parameters are averaged to produce an equivalent single-valley semiconductor. Thus, reducing the number of equations to be simultaneously solved by a factor of 3 and resulting in an excellent compromise between speed and accuracy.

The following expressions form the average material parameters:

$$n = n_\Gamma + n_L + n_X \tag{II.16}$$

$$\bar{v} = \alpha_\Gamma v_\Gamma + \alpha_L v_L + \alpha_X v_X \tag{II.17}$$

$$\bar{m}_c = \alpha_\Gamma m_\Gamma + \alpha_L m_L + \alpha_X m_X \quad \text{(II.18)}$$

$$\bar{w} = \alpha_\Gamma w_\Gamma + \alpha_L (w_L + \Delta_{\Gamma L}) + \alpha_X (w_X + \Delta_{\Gamma X}) \quad \text{(II.19)}$$

$\alpha_\Gamma + \alpha_L + \alpha_X = 1$, where α_Γ, α_L and α_X denote the ratio of *Γ*, *L* and *X* valley carrier populations to the carrier concentration, respectively; so the sum of these ratios is necessarily one. $\Delta_{\Gamma L}$ and $\Delta_{\Gamma X}$ are the minimum energy necessary to excite an electron to an upper conduction band . Moreover, by omitting the carrier heat and kinetic energy terms, the Boltzmann's transport equations can be simplified to the following equations [Mercury; 2004]:

$$\frac{\partial n}{\partial t} + \nabla(n\vec{v}) = 0 \quad \text{(II.20)}$$

$$\frac{\partial \vec{v}}{\partial t} + \vec{v}\nabla\vec{v} + \frac{q\vec{E}}{m_c} + \frac{2}{3m_c n}\nabla(nw) = -\frac{\vec{v}}{\tau_p} \quad \text{(II.21)}$$

$$\frac{\partial w}{\partial t} + q\vec{v}\vec{E} + \frac{2}{3n}\nabla(n\vec{v}w) = -\frac{w - w_0}{\tau_w} \quad \text{(II.22)}$$

τ_p and τ_w are the momentum and energy relaxation times, respectively. The parameters τ_p, τ_w, and $\vec{v}$ (function of the applied electrical field, doping and lattice temperature) are derived from three-valley ensemble Monte-Carlo simulations [Jacobini and Reggiani; 1983].

From the energy balance equation and when the third term of equation II.22 is expanded, the term $\nabla(n\vec{v})$ drop down to zero value, hence one can get:

$$\frac{2}{3n}\nabla(n\vec{v}w) = \frac{2\vec{v}}{3}\nabla w + \frac{2w\nabla(n\vec{v})}{3n} \quad \text{(II.23)}$$

As the second term in equation II.23 is negligible, this one can be simplified to the following expression which takes into account the steady state case:

$$\frac{5\nabla\omega}{3} = q\vec{E} - \frac{w - w_0}{\vec{v}\tau_w} \quad \text{(II.24)}$$

In the time-domain Radio Frequency simulation, the total conduction current is formed from the sum of the DC transport and displacement currents.

$$\vec{J}(t) = -qn(t)\vec{v}(t) + \varepsilon_0\varepsilon_r\frac{\partial\vec{E}(t)}{\partial t} \quad \text{(II.25-a)}$$

$$\vec{J}(t) = -qn(t)\mu_n\vec{E}(t) + \varepsilon_0\varepsilon_r\frac{\partial\vec{E}(t)}{\partial t} \quad \text{(II.25-b)}$$

where μ_n is the electron mobility which will be defined in next section. If the time derivatives in energy and momentum equations are developed, Equations II.21 and II.22 can be written as:

$$\frac{\partial w}{\partial t} = -\vec{v}\vec{\nabla} - \frac{1}{n}[w\,\nabla(n\vec{v}) - \vec{v}\vec{\nabla}(nw)] - \frac{w-w_0}{\tau_w} \qquad \text{(II.26)}$$

$$\frac{\partial(m_c v_l)}{\partial t} = -qE_l - \frac{qK_BT}{n}\frac{\partial n}{\partial l} - \vec{v}\vec{\nabla}(m_c v_l) - \frac{m_c v_l}{\tau_p} \qquad \text{(II.27)}$$

with $l \in (x,y)$ for a 2D simulation. For a 2D simulation along the length of the device (*x*-axis) and the depth of the device (*y*-axis), the *x* and *y* components of the momentum are given by the following set of equations:

$$\frac{\partial(m_c v_x)}{\partial t} = -qE_x - \frac{qK_BT}{n}\frac{\partial n}{\partial x} - v_x\frac{\partial(m_c v_x)}{\partial x} - v_y\frac{\partial(m_c v_x)}{\partial y} - \frac{m_c v_x}{\tau_p} \qquad \text{(II.28)}$$

$$\frac{\partial(m_c v_y)}{\partial t} = -qE_y - \frac{qK_BT}{n}\frac{\partial n}{\partial y} - v_x\frac{\partial(m_c v_y)}{\partial x} - v_y\frac{\partial(m_c v_y)}{\partial y} - \frac{m_c v_y}{\tau_p} \qquad \text{(II.29)}$$

As these equations are strongly coupled, they must be solved together. The momentum relaxation time τ_p is related to the mobility as given by [Grasser et al; 2003]:

$$\mu_n = \frac{q\tau_p}{m_c} \qquad \text{(II.30)}$$

II.2.5 Carrier mobility

The mobility can be defined in terms of electric field to maintain its energy dependence. Among the different mobility models, the models which describe the carrier mobility as a function of the electric field using specified material dependent parameters are the field dependent and the negative differential models.

II.2.5.1 Standard field-dependent mobility

The famous formula for the standard field dependent mobility was first given by [Caughey and Thomas; 1967] as follow:

$$\mu(E) = \mu_0 \frac{1}{\left[1+\left(\frac{\mu_0 E}{v_{sat}}\right)^{Beta}\right]^{Beta^{-1}}} \qquad \text{(II.31)}$$

For GaAs layer, the electron mobility under low electrical field (*E*) is μ_0 =8000cm^2/V.s and the saturated drift velocity $v_{sat} = 1 \times 10^7 \text{cm/s}$; the constant *Beta* usually equals one.

II.2.5.2 Negative differential mobility

The analytic negative differential mobility model has the common format with an additional term, αE included to describe the high-field *L-X* valley transport given by [Littlejohn; 1977, Lombardi et al; 1988, Mercury; 2004]:

$$\mu(E) = \frac{\mu_0 + \frac{v_{sat}}{2.E}\left(\frac{2+\alpha E}{1+\alpha E}\right)\left(\frac{E}{E_{cr}}\right)^{\gamma}}{1+\left(\frac{E}{E_{cr}}\right)^{\gamma}} \qquad \text{(II.32)}$$

where E_{cr} is the critical field and γ is a constant usually equals to four. The parameters values of the this equations can be set for each material layer and also according to the Indium content in the InGaAs or Aluminum or infraction in AlGaAs as given as example in Table II.1.

Table II.1: The parameters values used for the Negative Differential Field Dependent Mobility Model for the GaAs, $Al_{0.25}Ga_{0.75}As$ and $In_{0.55}Ga_{0.45}As$ [Mercury; 2004].

Parameter	GaAs	$Al_{0.25}Ga_{0.75}As$	$In_{0.55}Ga_{0.45}As$	Dimension
μ_0	7238	3218	13560	$cm^2/V/s$
v_{sat}	1.141×10^{7}	3.28×10^{6}	8.603×10^{6}	cm/s
α	1.525×10^{-5}	-1.20×10^{-6}	8.134×10^{-5}	cm/V
E_{cr}	4194	4769	4098	V/cm
γ	4	4	4	-

II.2.6 Boundary physics

Mercury is a commercial simulator that solves the physical equations describing carrier population and transport throughout the device domain

- Ohmic Contacts

  Mercury [Mercury; 2004] designs both the source and drain contacts as ohmic. It takes the simpler approach of modelling the intrinsic device and contacting the source and drain metal through circuit elements. The intrinsic device is connected to its contacts using the structure shown in Figure II.1.

The output contact characteristics at the reference nodes include the intrinsic lumped circuit elements. In the DC-IV simulation, the internal potentials are explicitly included in the output quantities using the expressions below:

$$V_s = V_{s\,node} + I_s R_S \quad \text{(II.33)}$$

$$V_{gs} = V_{gs\,node} + I_g R_G \quad \text{(II.34)}$$

$$V_{d\,node} = V_d + I_d R_D \quad \text{(II.35)}$$

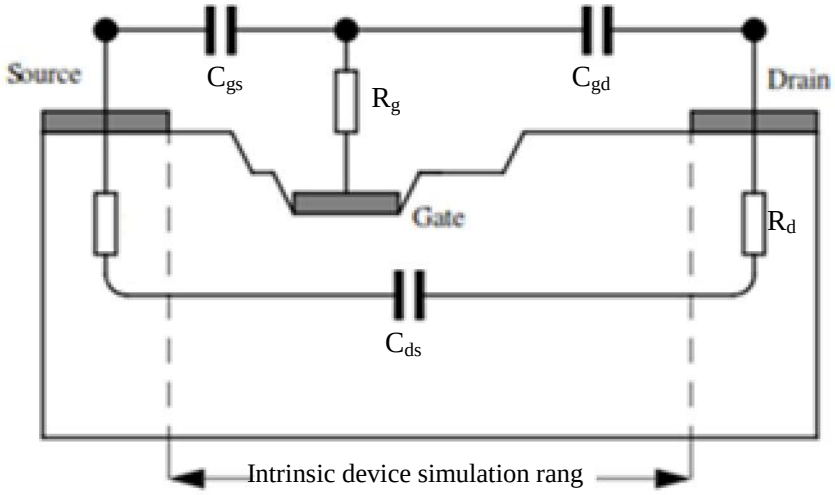


Figure II.1: Diagram of intrinsic device structure illustrating layout of circuit elements [Mercury; 2004].

where V_s, V_{gs} and V_d are the internal potentials. R_S, R_g, and R_d are the ohmic resistances, which values can be evaluated by the physical relation that bounds the resistivity R_{HO}; the total contact resistance will be calculated as a function of the contact length and the number of parallel contact fingers. The capacitances C_{gd}, C_{gs} and C_{ds} can be set such as input data.

- Schottky contact

The gate is defined as a Schottky contact where the contact work function is V_{bi}.

II.2.7 Numerical solution procedures

Semiconductor device operation is modeled by one to four coupled non-linear partial differential equations (PDEs). Mercury produces the numerical solutions of these equations by calculating the values of the unknowns on a mesh of point [Rose and Bank; 1981,

Anderson; 1965, Raffertyet al; 1985, Varga; 1962, Gear; 1971, Lambert; 1973, Polsky and Rimshans; 1986, Lundstrom and Shuelke; 1983, Kernighan and Ritchie; 1978, Pejcinovic et al; 1984, Gossens et al; 1994]. An internal discretization procedure converts the original continuous model to a discrete non-linear algebraic system that has approximately the same behavior. The set of PDEs, the mesh, and the discretization procedure determine the non-linear algebraic problem.

The non-linear algebraic system is solved using an iterative procedure that refines successive estimates of the solution. Iteration continues until the corrections are small enough to satisfy convergence criteria. Corrections are calculated by solving linearized versions of the problem while the linear sub-problems are solved using direct or interactive techniques.

The numerical method used is the current driven simulation. This technique operates by injecting a current source into the device and calculating the corresponding potential drop V_{ds}. This technique takes smaller voltage steps where the gradient in the current is changing rapidly and larger voltage steps where the current is insensitive to the applied voltage.

II.2.7.1 Meshes

The meshes are automatically generated and their density can change according to the tolerance used in the mesh generation algorithm. This can be done separately for solving Poisson's equation in the *y*-direction and for solving the transport equations in the *x*-direction. The key points to calculate Poisson's equation are the surface of the device, the interface between all layers, the bottom of the device, and some points dictated by the doping such as the peak of a Gaussian doping profile. For the channel simulation, it would be defining the starting and ending points of the device, the limits of the gate, and any point where the surface topography changes.

The uniform step of initial meshes and the minimum number of steps are defined automatically. The mesh is generated by taking the uniform step between any two adjacent key points. If this results in less than the minimum number of points between the two key points, then the minimum number of points is evenly spaced between the key points.

Once the initial mesh is created it can be used for calculation. After calculations, it can investigate the shape of some important dependent variables calculated on the grid (for example, the carrier density or the potential profile). The simulator can also refine the grid by making it dense in regions where the dependent parameter has large derivatives. By choosing a refined grid, the linear interpolation of the dependent parameter is sufficiently close to the correct value. We can start with the first three terms of the Taylor expansion:

$$f(x+d) = f(x) + d.\frac{\partial f(x)}{\partial x} + \frac{d^2}{2} \cdot \frac{\partial^2 f(x)}{\partial x^2} \quad \text{(II.36)}$$

For a linear interpolation to model the function *f(x)* where the third term must be smaller than the allowed error (defined by the parameter α_r).

$$\frac{d^2}{2} \cdot \frac{\partial^2 f(x)}{\partial x^2} \leq \alpha_r . f(x) \quad \text{(II.37)}$$

This lead to a step d given by:

$$d \leq \sqrt{\frac{2.\alpha_r . f(x)}{\partial^2 f(x)/\partial x^2}} \quad \text{(II.38)}$$

In addition to α_r, three other parameters are defined: a maximum step size, a minimum number of steps, and an absolute minimum step size. The maximum step size should be larger than the uniform step size used for the initial mesh. Otherwise, it will be impossible for the refined mesh to be less dense than the initial mesh. The minimum number of steps refers to the minimum number of points needed between two adjacent key points. The absolute minimum step size is to prevent having too many points appearing in the refined grid.

II.2.7.2 Newton method

Newton method is used to solve the non-linear equations generated by the physical device relationships. Each iteration of the Newton method solves a linearized version of the entire nonlinear algebraic system. The iterations will normally converge quickly (in about three to eight iterations) as long as the initial guess is sufficiently close to the final solution.

II.2.7.3 The current driven DC I-V simulation

Mixed current/voltage boundary conditions are used during the DC I-V simulation. Firstly, the gate bias and source current are injected. Then, the corresponding gate and drain currents, and the drain bias are calculated. To get a single bias point solution, the gate and drain biases are specified. An automatic algorithm searches the input (source) currents for the solution. This requires an iterative procedure which somehow reduces the gains in efficiency. But if a DC I-V sweep is performed, the simulator can be left in "current-driven" mode and no iteration will be necessary. An automatic DC I-V generation algorithm increases the efficiency of the simulation, since it takes larger bias/current steps in the linear regions of device operation and smaller steps in areas of non-linear response, particularly near the "knee" of the I-V curves and at the breakdown.

II.3 The drift diffusion model

Some simplifying assumptions have been made on the previous equations, leading to two variants of the hydrodynamic model, the energy-balance model and the drift-diffusion model. In this section, we present the equations of the latter model. Indeed, if the nonlinear convection term is neglected ($v.\nabla v$) (second order term) in the momentum conservation equation (II.21), the system of energy balance equations is obtained. The drift-diffusion equations are deduced from the latter model, assuming in addition that the electron temperature does not vary and is equal to that of the semiconductor crystal lattice $T_e = T_o$. Thus, the gradient of T_e is zero, the conservation energy equation disappears.

The drift–diffusion transport approach includes a drift current along the electric field and a diffusion current that flows along carrier density gradients. In a spatially homogenous system, it reduces to Ohm's law for low electric fields. However, such models assume that the time and space scales of the problem are such that there is, at all times. It assumes that the microscopic distribution of momentum and energy over the charge carriers at any location and time inside the device is equal to that which one would find in a large sample with a dc field equal to the local instantaneous field [Grondin et al; 1999].

II.3.1 Model Description

The drift diffusion model of transport in semiconductors is governed by three sets of differential equations.

First, the one-dimensional (*y*-direction in our case) Poisson's equation relating potential with charge densities:

$$\frac{d^2 \cdot}{dy^2} = -\frac{q}{\pounds}\left(p - n + N_D - N_A + (1 - f_D)N_{TD} - f_A N_{TA}\right) \qquad \text{(II.39)}$$

where $\cdot$ is the potential, $\varepsilon = \varepsilon_0 \varepsilon_r$ is the dielectric constant of GaAs; n and p are the free electron and hole densities, ($N_D - N_A$) is the effective doping distribution, N_{TD} is the deep donor density, N_{TA} is the deep acceptor density and $f_{D(A)}$ is the occupation probability of the deep donor (or acceptor) given by the Shockley-Read-Hall (SRH) statistics as [Shockley and Read; 1952, Hall; 1952]:

$$f = \frac{C_n n + C_p n_i e^{-\left(\frac{E_T - E_i}{K_B T}\right)}}{C_n\left(n + n_i e^{\left(\frac{E_T - E_i}{K_B T}\right)}\right) + C_p\left(p + n_i e^{-\left(\frac{E_T - E_i}{K_B T}\right)}\right)} \qquad \text{(II.40)}$$

In the above equation, E_T is the energy level of the trap, E_i is the intrinsic Fermi level, $C_{n(p)}$ is the trap capture coefficient for electrons (holes), n_i is the intrinsic density, k_B is the Boltzmann constant, and T is the absolute temperature.

Second, the electron and hole conservation laws can be written as:

$$\frac{1}{q} \cdot \frac{dJ_n}{dx} + G - U = 0 \qquad \text{(II.41)}$$

$$\frac{1}{q}\frac{dJ_p}{dx} - G + U = 0 \qquad \text{(II.42)}$$

where G is the generation rate and U is the net recombination rate. Recombination in GaAs can be direct (from band to band) or via recombination centres located in the energy gap. The first can be neglected if there are high densities of recombination centres. The second mechanism is given by the Shockley-Read-Hall model [Shockley; 1952] for a single species of recombination centres as:

$$U = \frac{np - n_i^2}{\tau_p\left(n + n_i e^{\left(\frac{E_T - E_i}{K_B T}\right)}\right) + \tau_n\left(p + n_i e^{-\left(\frac{E_T - E_i}{K_B T}\right)}\right)} \qquad \text{(II.43)}$$

where τ_n and τ_p are the minority carrier lifetimes given by:

$$\tau_n = \frac{1}{C_n N_T} \quad \text{and} \quad \tau_p = \frac{1}{C_p N_T}$$

Since we have considered two deep levels then the net recombination rate is the sum of the two rates.

The generation rate is usually made of several types. Another generation mechanism is the impact ionisation generation rate, which may be important for high electric field and current conditions. It is given by [Shur; 1987],

$$G = \alpha(E).\frac{|J_n| + |J_p|}{q} \qquad \text{(II.44)}$$

where $\alpha(E)$ is the field dependent impact ionization coefficient; it is equal to $\alpha_\infty \exp\left(-\frac{E_i}{E}\right)^2$, with $\alpha_\infty = 3.5.10^5$ cm^{-3} and E_i= 550 kV/cm.

Although the electric field is high and can reach 200 kV/cm for a substrate bias of 200 V, the currents J_n and J_p are very small $\approx 10^{-10}$ Acm^{-2} in reverse bias. This gives a generation rate of the order of $G \approx 10^{11}$ s^{-1}cm^{-3} which is negligible compared to U which can be as high as 10^{17}s^{-1}cm^{-3} and with τ_n and $\tau_p$as low as 10^{-10} s in GaAs with the presence of high density of traps and or recombination centers.

Third, the electron and hole currents are given by:

$$J_n = -\mu_n\left(qn\frac{d\cdot}{dx} - K_B T\frac{dn}{dx}\right) \qquad \text{(II.45)}$$

$$J_p = -\mu_p\left(qp\frac{d\cdot}{dx} + K_B T\frac{dp}{dx}\right) \qquad \text{(II.46)}$$

where μ_n and μ_p are the electron and hole mobility whose dependence on the electric field E is taken into account by the following empirical relation [Horio et al;1991].:

$$\mu_n = \mu_{no}\frac{1+\left(\frac{v_{ns}}{\mu_{n0}E}\right)\left(\frac{E}{E_0}\right)^4}{1+\left(\frac{E}{E_0}\right)^4}\ ,\ \mu_p = \mu_{p0}\frac{1}{1+\mu_{p0}\frac{E}{v_{ps}}} \qquad \text{(II.47)}$$

with μ_{n0} = 4500 cm^{2}V^{-1}s^{-1} is the low field electron mobility, μ_{p0} = 400 cm^{2}V^{-1}s^{-1} is the low field hole mobility, v_{ns}=8.5x10^6 cm.s^{-1} is the electron saturation velocity, v_{ps}=10^7 cms^{-1} is the hole saturation velocity, and E_0= 4000 Vcm^{-1} is the peak electric field.

II.3.2 Numerical resolution

Numerical simulations were carried out using the package Kurata [kurata; 1982]. The three differential equations (IV.1), (IV.3) and (IV.4) together with equations (IV.5)-(IV.8) were numerically solved for the three unknowns: ψ, n and p, as well as appropriate boundary conditions. These quantities are defined such as the electrical neutrality holds at the ohmic contact for the space charge while for the potential is zero and the applied voltage at the ends of the channel and the substrate respectively. These give six boundary conditions which are:

At the channel end:

$$n(1) = N_D \,,\; p(1) = \frac{n_i^2}{N_D} \tag{II.48}$$

At the substrate end:

$$\begin{cases} n(L) = \dfrac{\left(M \times N_T^M + N_{DS} - N_{AS}\right) + \sqrt{\left(N_{AS} - N_{DS} - M \times N_T^M\right)^2 + 4n_i^2}}{2} \\ p(L) = \dfrac{\left(N_{AS} - N_{DS} - M \times N_T^M\right) + \sqrt{\left(N_{AS} - N_{DS} - M \times N_T^M\right)^2 + 4n_i^2}}{2} \end{cases} \tag{II.49}$$

$$\cdot(1) = 0, \qquad \cdot(\mathrm{L}) = V_{app} \tag{II.50}$$

Here, M indicates the trap charge,– for a deep acceptor and + for a deep donors, N_{DS} and N_{AS} are the densities of the shallow donors and acceptors in the substrate, respectively, and V_{app} is the applied voltage to thesubstrate.

Obviously the quantities, J_n, J_n and U involve nonlinear functions which can be linearized by Taylor expansion neglecting higher order terms. According to Scharfetter and Gummel [Scharfetter and Gummel; 1969], the current equations are rewritten in integral forms by assuming a constant current between adjacent points and a linear variation of the electrostatic potential.

II.4 Deep level effects on GaAs MESFETs and HEMTs

Extensive researches have been achieved on the analysis of deep centers (deep levels) in GaAs. Knowing that the issue remains most relevant to GaAs microelectronics, many methods for the characterization of deep centers are focusing on the nature of deep centers in the bulk-grown and epitaxial forms of GaAs, whether ion-implanted or undoped.

It is particularly often to encounter disagreement between the predicted and the actual performance of a GaAs devices or integrated circuits (IC). This is partly due to the fact that usual approaches do not considering deep centers that tend to form in GaAs during different process steps.

Deep centers in a material as well as carrier traps, recombination centers, or scattering centers, can strongly alter the electronic properties of the material and ultimately the device performance. This factor takes importance as the industry progresses to smaller feature sizes and to multilayered structures. They are inherent in the bulk of semi-insulating substrates, in high-resistivity buffer layers, and in undoped portions of heterostructures.

II.4.1 The Nature of deep centers in different varieties of Gallium-Arsenide

The large number of types of deep centers in GaAs is due to the semiconductor being a compound. In bulk single crystals, deep centers mostly arise from non-stoïchiometry [Mil'vidskii and Osvenskii; 1984].

In epitaxial layers, the concentration of such defects should be much smaller, since epitaxy is performed at far lower temperatures than bulk growth. A large proportion of defects in epitaxial layers is produced by the substrate, they also arise due to the stress induced by growth and cooling [Mil'vidskii and Osvenskii; 1985]. During the epitaxy, the substrate acts as a source of impurities and point defects that diffuse into the layer. More than 30 types of deep centers have been identified in GaAs, with energy levels divided almost equally between the upper and the lower half of the band gap.

Table II.2 lists the activation energies and capture cross sections for different types of electron or hole deep-level traps while indicating the corresponding growth methods of bulk or epitaxial material. The GaAs traps [Martinet al; 1977, Mitonneau et al; 1977], known by the symbols EL and HL for electron and hole traps, respectively, have become accepted notation and for the traps denoted otherwise were discovered later. Table II.2 reports that traps in epitaxial material are less diversified than in bulk one.

The concentration of electron traps is estimated at 10^{12}–10^{14} cm^{-3} in epitaxial material when bulk crystals tend to have four or more deep levels in the upper half of the band gap [Katayama et al;1987]. The trap concentration in bulk crystals is one or two orders of magnitude larger than those of the same traps in epitaxial layers.

Table II.2: Deep-level traps in bulk-grown or epitaxial GaAs [Khuchua et al; 2003]. The acronyms LEC, HB, LPE, MBE, MOVPE, and VPE state for: Liquid Encapsulated Czochralski, Horizontal Bridgman Process, Liquid-Phase Epitaxy, Molecular-Beam Epitaxy, Metallo-Organic Vapor-Phase Epitaxy, and Vapor-Phase Epitaxy, respectively.

Trap	E_a(eV)	σ(cm^2)	Process	Source
EL1	0.78	1×10^{-14}	LEC	[Martin et al; 1977]
EL2	0.82	$(0.8\text{-}1.7)\times10^{-13}$	VPE, MOVPE, LEC, HB	[Martin et al; 1977]
EL3	0.57	$(0.8\text{-}1.7)\times10^{-13}$	VPE, LEC, HB	[Martin et al; 1977]
EL4	0.51	1.0×10^{-12}	MBE, MOVPE, LEC	[Martin et al; 1977]
EL5	0.42	$(0.5\text{-}2)\times10^{-13}$	VPE, LEC, HB	[Martin et al; 1977]
EL6	0.35	1.3×10^{-13}	VPE, LEC, HB, MOVPE	[Martin et al; 1977]
EL7	0.3	7.2×10^{-15}	MBE	[Martin et al; 1977]
EL8	0.27	7.7×10^{-15}	VPE	[Martin et al; 1977]
EL9	0.225	6.8×10^{-15}	VPE, HB	[Martin et al; 1977]
EL10	0.18	3.2×10^{-15}	VPE, MBE, HB	[Martin et al; 1977]
EL11	0.17	3.0×10^{-16}	VPE	[Martin et al; 1977]
EL12	0.78	4.9×10^{-13}	VPE, LEC	[Martin et al; 1977]
EL14	0.215	2.3×10^{-15}	LEC, HB	[Martin et al; 1977]
EL16	0.37	4.0×10^{-18}	VPE	[Martin et al; 1977]
EL17	0.21	$(0.7\text{-}1)\times10^{-12}$	LEC, HB	[Auret et al;1986, Ghezzi et al; 1986]
EA2	0.52	5.0×10^{-16}	LEC	[Ghezzi et al; 1986]
EA7	0.14	1.0×10^{-15}	LEC	[Ghezzi et al; 1986]
EC2,E0, EC3	0.49	$(5\text{-}9)\times10^{-15}$	VPE, MOVPE, HB	[Fang et al; 1987, Partin et al; 1974]
HL1	0.94	3.7×10^{-14}	VPE, LEC, HB	[Mitonneau et al; 1977]
HL2	0.73	1.9×10^{-14}	LPE	[Mitonneau et al; 1977]
HL3	0.59	3.0×10^{-15}	VPE, LEC, HB	[Mitonneau et al; 1977]
HL4	0.42	3.0×10^{-15}	VPE, LEC, HB	[Mitonneau et al; 1977]
HL5	0.41	9.0×10^{-14}	LPE	[Mitonneau et al; 1977]
HL6	0.32	5.5×10^{-14}	VPE, MOVPE	[Mitonneau et al; 1977]
HL7	0.35	6.4×10^{-15}	MBE, MOVPE	[Mitonneau et al; 1977]
HL8	0.52	3.5×10^{-16}	MBE	[Mitonneau et al; 1977]
HL9	0.69	1.0×10^{-15}	VPE, LPE	[Mitonneau et al; 1977]
HL10	0.83	1.7×10^{-15}	VPE	[Mitonneau et al; 1977]
HL11	0.35	1.4×10^{-15}	LEC	[Mitonneau et al; 1977]
HL12	0.27	1.3×10^{-15}	LPE	[Mitonneau et al; 1977]
H06	0.13	2.0×10^{-15}	MOVPE	[Ghezzi et al; 1986]

Both kinds of material have two to four levels in the lower half of the gap band. Among the types listed in Table II.2, the EL2 trap is eventually examined to the highest extent [Martin and Makram-Ebeid; 1986, Guillot; 1998, Meyer; 1988]. It is due to the fact that this trap governs the semi-insulating properties of undoped gallium arsenide devices. The EL2 trap is found in both bulk and epitaxial material (except for LPE and MBE layers). Its distinguishing

feature is the existence of a metastable state. The concentration of EL2 traps is determined by the As-to-Ga flux ratio and the growth rate.

The traps have also been found to arise under plastic deformation, neutron irradiation, and ion implantation. The EL2 trap consists of an As_{Ga} defect and an interstitial arsenic atom, as established by ESR and electron– nuclear double resonance.

Until recently, the EL6 center had been regarded as a major recombination center in GaAs [Fang et al; 1987, Steinegger; 2002]. The influence has been ascertained of the conditions of growth and surface treatment on EL6 concentration. In addition, the centers have been found to arise under plastic deformation, neutron irradiation, and ion implantation. If the annealing temperature is above 400°C, the decrease in EL6 concentration has been found to be accompanied by the increase in EL2 concentration. In other researches, EL6 had been identified as an isolated As_{Ga} defect, but this conclusion is not in accord with the fact that the annealing of EL2 traps does not increase EL6 concentration. The EL6 center was also identified as the V_{Ga}–V_{As} divacancy [Fang et al; 1987].

Some types of electron trap have been attributed to the presence of impurities. The EL1 center has been observed in Cr-doped specimens [Martin et al; 1977]. The EL11 center has been identified as a complex including structural imperfections and an impurity [Blood. and Yarris; 1984]. The 0.48eV center is associated with the presence of nickel [Brehme and Pickenhein; 1986, Partin et al; 1974].

The hole traps HL1, HL3, HL4, HL6, HL10, and HL12 are attributed to impurities [Mitonneau et al; 1977, Prints and Getalov; 1980]. Because any of the VPE layers of GaAs show HL6 or HL10 traps, they are ascribed to unwanted impurities. The HL3, HL4, and HL12 traps are due to iron, copper, or zinc, respectively. The HL2, HL8, and HL9 traps are associated with structural imperfections [Mitonneau et al; 1977].

II.4.2 The deep level in HEMTs

A deep understanding of the trapping mechanism in HEMTs is a necessary step for developing accurate device models for HEMT characterization. Trapping phenomena mainly limit the device performance. Examples of anomalous behavior include the collapse of I-V characteristics, decrease in both maximum transconductance and gate-voltage swing, shift in pinch-off voltage, and generation-recombination noise. There has been a significant amount of research directed towards understanding the basic physics of deep levels in doped AlGaAs layers [Chadi and Chang; 1988(a), Chadi and Chang; 1989, Mooney; 1987, Morgan; 1986] and Semi insulating (SI) substrate [Martin et al; 1977, Mitonneau et al; 1977, Barton and

Snowden; 1990, Chadi and Chang; 1988 (b)], but less efforts have been devoted to incorporating trapping mechanisms in the device models. Fermi-level pinning due to DX centers in HEMTs has been analyzed [Mizuta; 1989] based on a two dimensional drift diffusion model. They demonstrated that maximum transconductance of AlGaAs/GaAs is lowered by DX centers and Fermi-level pinning phenomena disappear in pseudomorphic HEMTs.

By including the DX center mechanism [Shawk et al; 1990] and assuming that all donors are electrically active as DX centers, [Tachikawa et al; 1985] confirmed that DX centers are also present in n-type GaAs and become the ground state when the pressure exceeds 20 kbar. This result provides strong evidence that DX properties are associated with isolated donors. A measurement work [Mooney; 1987] has further shown that there is a strong variation of trapping kinetics with a change in alloy composition of $Al_xGa_{1-x}As$ and the DX center concentration increases when the pressure is applied to the low mole fraction AlGaAs.

II.4.2.1 The DX center model

In $Al_xGa_{1-x}As$, donor-related deep states are commonly referred to as the DX centers, which introduce several undesirable effects for HEMT operation. The most important outcome of extensive experimental and theoretical studies on the electronic properties of $Al_xGa_{1-x}As$, is that, independently of alloy composition, each donor gives rise to two types of electronic states, a shallow and delocalized effective-mass level associated with the normal substitutional site configuration, and a more localized level, labelled DX centers arising from a lattice distortion at or near the donor [Chadi and Chang; 1988(a)].

The charge-control model presented in this work is extended to model the steady-state DX center related phenomena for microwave devices and circuit operation based on the work of Chadi and Chang [Chadi and Chang; 1988(a), Chadi and Chang; 1989] and experimental results for DX centers reported in [Mooney et al; 1987].The DX center is a highly localized and negatively charged center [Chadi and Chang; 1988(a)] resulting from the equation:

$$2D^0 \rightarrow D^+ + DX^- \qquad \text{(II.51)}$$

where D^0 and D^+ are the neutral and four-fold coordinate substitutional donors. The DX^0 and DX^+ states are completely unstable with respect to D^0 and D^+, respectively. For a donor that gives rise to shallow and deep states, the total donor concentration N_D ($N_D = N_d$) is given by:

$$N_d \rightarrow N_d^+ + N_{ds}^0 + N_{dX}^0 - N_{dX}^- \qquad \text{(II.52)}$$

where N_{ds}^{0} is the concentration of neutral donors in shallow states, and N_{dX}^{0} and N_{dX}^{-} are the respective concentrations of donors with electrons in neutral and negatively charged DX states.

There is a sharp increase in the concentration of deep-donor levels in $Al_xGa_{1-x}As$ [Chadi and Chang; 1988 (a), Chadi and Chang; 1989, Mooney et al; 1987] from10^{-3} times the Si-dopant concentration at $x = 0.2$ to a maximum at $x = 0.4$ equals to the Si concentration. This steep rise occurs in the composition range x=0.27 ± 0.35 [Singh and Snowden; 1999]. The emission activation energy for DX center is > 0.4 eV, independent of Aluminum mole fraction of the AlGaAs layer. However, the activation energy for capture varies strongly with the Aluminum mole fraction from about $x = 0.35$, where the Γ and L conduction-band minima cross, to about 0.4 eV at $x = 0.22$, where DX levels cross the bottom of the conduction-band.

II.4.2.2 The substrate trap model

Traps have a dominant role in producing semi-insulating behavior in GaAs substrates as mentioned above and generally have a significant effect on compound semiconductor device operation. A high density of both donor- and acceptor-like traps exists in the SI substrate [Martin et al; 1977, Mitonneau et al; 1977] where no less than fifteen different electron traps, and twelve different hole traps exist in a variety of SI GaAs materials. The four kinds of traps are important in determining the properties of the SI GaAs material [Barton and Snowden; 1990]. These are deep-donor, deep acceptor, shallow-donor and shallow-acceptor traps present in the band-gap of the material.

The deep-donor trap, commonly referred to as the EL2 trap level, resides at an energy level between 0.75 and 0.8 eV below the conduction-band-edge. It is present in densities varying between 10^{20} and 10^{23} m^{-3}, depending upon the method of preparation of the material. The deep-acceptor trap is present at an energy-level about 0.8 eV above the valence band edge. It is associated with chromium which is often deliberately introduced to compensate for shallow-donor. It is introduced in the concentration range from 10^{21} to a few times 10^{23} m^{-3} [Singh and Snowden; 1999]. The shallow-donor trap is usually attributed to silicon introduced from the walls of the reactor vessel. The shallow-acceptor trap is often associated to carbon. These shallow-levels are present in concentrations of about 10^{22} to10^{23} m^{-3}. In GaAs substrate grown by LEC technique, only EL2 and shallow acceptor traps are present.

In the present work, the charge-control model is extended to model the substrate trap related phenomena by modifying the local net charge density as in Equation II.1.

II.4.3 Backgating effect

Deep-level traps, especially those at interfaces, tend to adversely affect the performance of FETs and ICs. Examples of these effects are backgating, across-wafer variation of threshold voltage, saturation drain current, and leakage current in MESFETs, HEMTs, and delta-doped FETs; as well as the limitation of switching speed and IC complexity.

The 'backgating effect' refers to the phenomenon that the drain current of MESFET decreases when a negative voltage is applied to a nearby electrode or to the backside of the substrate [Kocot and Stolte; 1982; Shenai and Dutton; 1988, Ohno and Goto; 1990]. Such an effect can cause undesirable coupling or cross talk between adjacent devices that can limit the integration scale of GaAs IC's. The cause of this undesirable effect was thought to be due to deep-level impurities near the substrate [Kocot and Stolte; 1982; Shenai and Dutton; 1988], and hence the insertion of several kinds of buffer layers in epitaxial structures was proposed to reduce it and improve RF performance [Bond et al; 1996].

Backgating effect tends to show threshold character. Regularly, it is measured by the change in drain current for a given negative voltage applied to the side gate and by the threshold side-gate voltage, at which drain current starts varying appreciably [Khuchua et al; 2003].

Most researchers do agree that deep-level traps in the substrate should play a key part in backgating. By using the concept of i–n junction (n GaAs film on i GaAs substrate or buffer layer) an analog of the pn junction [Kitahara et al; 1982], it was conjectured that applying a side-gate voltage widens the depletion layer in the film. However, this model does not represent the threshold character of backgating.

The model proposed by lee [Lee et al; 1982] allows for the redistribution of side-gate voltage between the i–n junction and the bulk of the substrate. The resistance of the substrate drops sharply when side-gate voltage crosses V_T, the threshold voltage at which substrate traps reach maximum occupancy. As a result, the side-gate voltage drops mainly across the i–n junction, so that the widths of the depletion layer and the n-GaAs layer increase and decrease, respectively. However, the theory of space charge-limited current [Lampert and Mark; 1973] implies that V_T should vary as the square of the distance between the n-film and the side gate, whereas experiments [Makram-Ebeid and Minondo; 1985, Chang et al; 1984] indicate a linear relation.

The threshold character of backgating is related to a sharp decrease in substrate resistance [Li et al; 1990 (a, b)], which in turn is associated with the impact ionization of deep-level traps. If there are two types of deep level trap in the substrate and the impact-ionization coefficient is large enough, the equation for the free electron density in the substrate has a number of

physically meaningful solutions, so that the substrate shows an S-type current–voltage characteristic. As a result, the substrate may switch from a high to a low resistance value due to an abrupt increase in carrier density. Again, this leads to a certain proportion of side-gate voltage dropping across the i–n junction, so that its depletion layer widens, while the conductance of the n-film decreases.

backgating is also related to the detrapping of holes from deep acceptors in the space-charge region of the i–n junction by the Poole–Frenkel effect [Gergel'V.et al; 1990]. Interestingly, they have revealed that backgating may or may not have threshold, depending on the degree of compensation in the substrate.

II.5 Summary

In this chapter, we investigated two transistor models, i.e., the drift diffusion (DDM) and the hydrodynamic (HDM). The later was retained for recessed gate MESFET and pHEMT because it takes into account main phenomena that occur in transistors especially in the case of high miniaturization and high frequency operation. Based on BTE and electron single gas approaches, the hydrodynamic model resolves self-consequently the Poisson's equation and the transport equations. First, the electromagnetic part of Poisson's equation is neglected since just the electrostatic potential will be solved at low frequencies. While, at high frequency, the electron transport is seriously affected, thus, the displacement current was included in all time domain simulations.

The tree transport equations relate to particle, momentum and energy equations solved by the method of moments. Thus, a detailed description about the two dimensional hydrodynamic model was given. Then, the nature of deep levels and their effects on the GaAs metal semiconductor field effect MESFET and High electron mobility transistor HEMT were introduced, and the origin of some deep levels expressed. The Backgating effect was also investigated as the most important effect of the presence of the deep levels in the GaAs MESFET substrate

The drift diffusion Model (DDM) is quiet efficient for simple planar devices, while in more complicate stucture, the hydrodynamic Model (HDM) is more suitable. However, for mm-range frequencies, the physical model could be too complicated to implement if we want to include high frequencies parasitic effects such as the wave propagation effects. Thus, an electrical approach is needed.

Chapter III

Analytical and Electrical Modelling of Field Effect Transistors

III.1 Introduction

An accurate knowledge of the electrical properties of the semiconductor material as well as the nature of the physical contact to the material allows a reliable determination of the electrical characteristics of GaAs devices. Thus, both physical properties and structure geometry parameters are required for efficient device modeling. Also, accurate large-signal FET models are particularly critical for reliable performance prediction of nonlinear microwave circuits.

Firstly, the structural description of the MESFET and the physical meaning of its circuit parameters are given. Then, we provide the extraction process of these parameters. The small-signal modeling methodology is also studied as the basis of a large-signal modeling approach.

GaAs MESFET and HEMT technology has matured and Monolithic Microwave Integrated Circuits(MMICs) operating above 100GHz have become standard products [Golio; 1991, Mass; 2003].Such devices are based on a large number of closely packed passive and active structures, transmission lines, and discontinuities operating at high speeds and frequencies [Liou and Schwierz; 2003, Cidronali; 2003].

In the millimeter-wave range, to deal with non-negligible electromagnetic effects such as undesired radiation and parasitic coupling between circuit elements, an integrated circuit design requires a full-wave approach to accurately analyze these effects. This implies solving Maxwell's equations and taking into account the interaction between parasitic electromagnetic waves and circuit elements. Since this interaction can affect the overall system performance, the entire system needs to be characterized as a whole package by a full-wave analysis incorporating all transistor components.

As the operating frequency of FETs increases to the millimetre-wave range, the physical dimensions of the electrodes become comparable to the wavelength [Grondin et al; 1999].As a consequence, the impedance at the input of the device electrode becomes different from that at the output side of the electrode [Alsunaidi et al; 1996]. Thus, the electrodes of the device exhibit different phase velocities for input and output signals, which affect the overall performance of the device due to the mismatch in phase velocities. The possibility of achieving an accurate modeling should be addressed by the full-wave device analysis and

global circuit modeling as presented in [Goasguen et al; 2001, Movahhedi; 2006, Imtiaz; and Ghazaly 1997].

Let us first introduce the concept of a new distributed FET model. In the proposed approach, each infinitesimal segment of the model was divided into two parts namely, active and passive, whose elements are all per unit length. The passive part describes the behaviour of the transistor as a set of three coupled lines (symbolizing the electrodes while the active part relates to a distributed equivalent circuit [Asadi and Yagoub; 2010 (a)]; in time-domain, this approach leads to a set of differential equations that should be solved to fully characterize the model.

We selected the well-known efficient discretization technique called the lumped segmentation approach (also called the transmission line method) to analyze each infinitesimal segment of the proposed model [Dounavis et al; 2001, Achar and Nakhla; 2001, Chang; 1989, Grivet- Talocia; 2003, Dounavis; 2002].

Then, to numerically get the model element values, the Finite Difference Time Domain (FDTD) method was preferred. In fact, this method is widely used in solving various kinds of electromagnetic problems, wherein lossy, nonlinear, and in homogeneous media and transient problem can be considered [Asadi and Yagoub; 2010(b), Tafove; 1992, Sadiku; 1992].

III.2 The MESFET

III.2.1 Device description

A cross-section view of a GaAs MESFET structure is shown in Figure III.1 [Golio; 1991]. At microwave frequencies, the most important parameter is the "length" of the gate along the carrier path. The shorter the gate length, the higher could be the signal frequency. If the FET is to handle a large amount of current, the gate width must be increased appropriately.

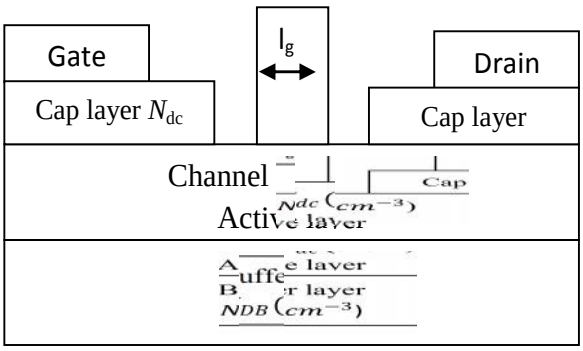


Figure III.1: Example of simulated gate recessed FET structure.

Relationships between currents and voltages are displayed in Figure III.3. The channel current I_{ds} is plotted as a function of applied drain-source voltage for different gate-source voltage levels, highlighting three operating regions:

- *The linear region* is the region where the current flow is almost linear with the drain voltage. As the drain potential increases, the depletion region at the drain end of the gate becomes larger than at the source end. Since the electrical field increases with the drain-source potential, a related increase in electron velocity occurs; this simultaneously makes a linear increasing current through the channel region.
- Increasing the drain voltage allows the electrons to reach their maximum limiting velocity at the drain end of the gate. At this point, the current does not follow the drain bias increasing: thus, the device is saturated and its operation enters *the saturation region.*
- Finally, when gate and drain bias become very large, the device boards in *the breakdown region* [Shur; 1978, Bose; 2001], and the drain current increases sharply.

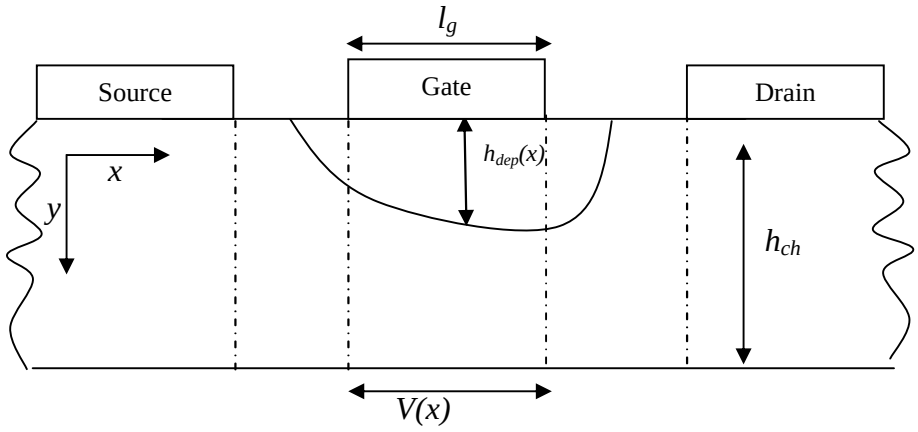


Figure III.2: A cross sectional view of a biased GaAs MESFET channel.

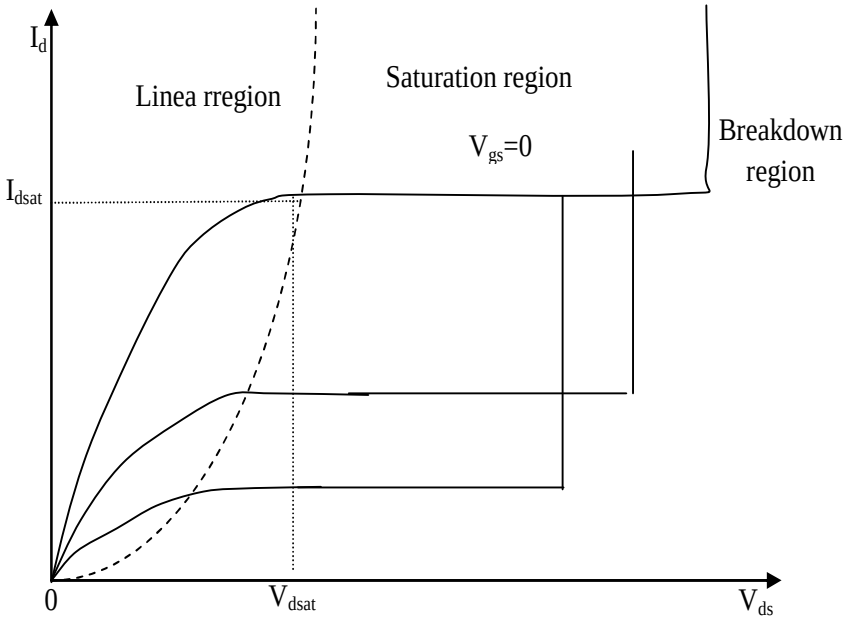


Figure III.3: Basic output current-voltage characteristics of the FET transistor.

III.2.2 Physical meaning of the circuit elements

During the last decade, generating efficient measurement-based GaAs FET models has been one of the major issues in computer-aided design (CAD) of RF/microwave circuits. In such process, providing designers with accurate electrical equivalent small-signal models is indeed crucial.

The equivalent circuit shown in Figure III.4 is widely considered as an accurate small-signal model for virtually all types of GaAs MESFETs [Dambrine; 1988] up to at least 25GHz [Ladbrooke; 1989]. Furthermore, if the parasitic elements in the equivalent circuit are carefully taken in account, it could be used at higher frequencies.

As illustrated in the equivalent circuit, the components of a single GaAs MESFET can be limited to a set of 15 frequency-independent variables. Basically, these fifteen unknowns can be divided into two groups:

I- The intrinsic elements g_m, g_{ds}, C_{gs}, C_{gd} (which includes, in fact, the drain-gate parasitic), C_{ds}, R_i and τ, whose values are function of the bias conditions.

II- The extrinsic elements L_g, L_s, L_d, R_g, R_s, R_d, C_{pd} and C_{pg}, which are independent of the biasing conditions.

This electrical circuit is deduced from the physical behavior of the transistor as shown in Figures III.5 to III.7. From these figures, it is easy to recognize that each lumped element in

the equivalent circuit of a GaAs MESFET is related with a corresponding physical part of the transistor.

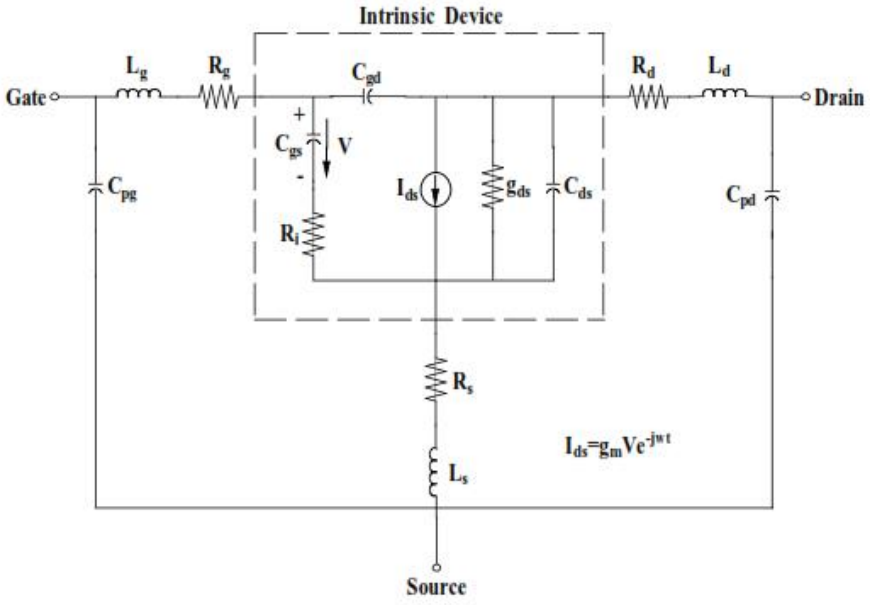


Figure III.4: MESFET small-signal equivalent circuit including parasitic elements.

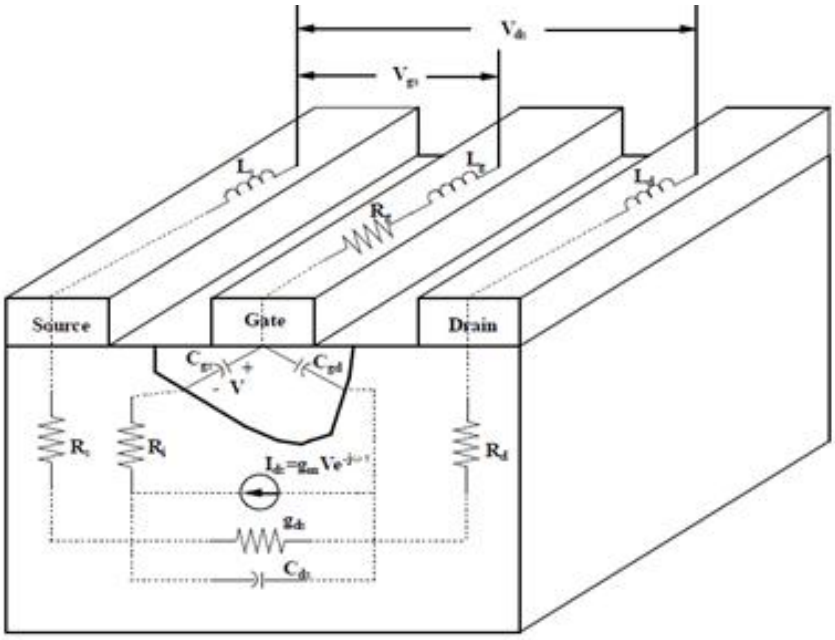


Figure III.5: Physical cross-section of the GaAs MESFET small-signal model.

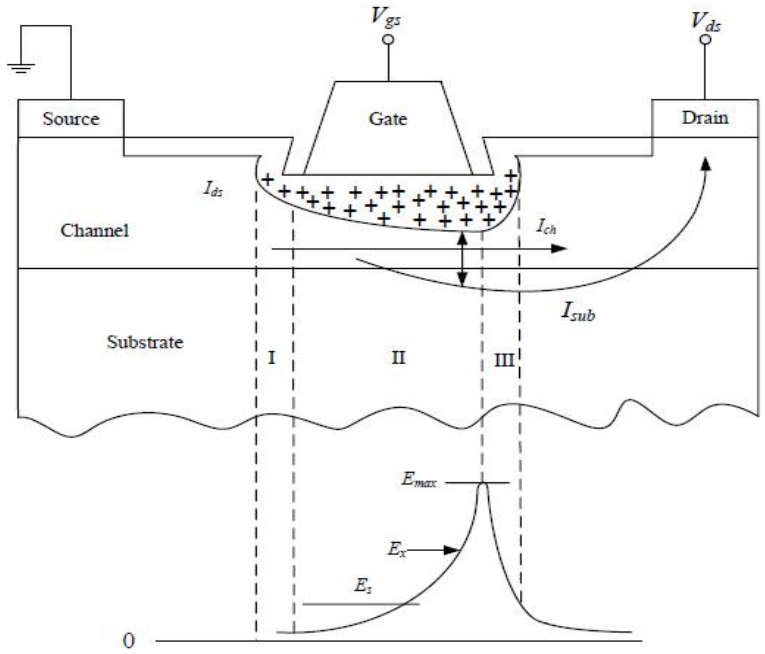


Figure III.6:Cross-sectional view of an operating MESFET showing the scattering of carriers under intense electric field into the substrate and subsequently collected by the drain contact.

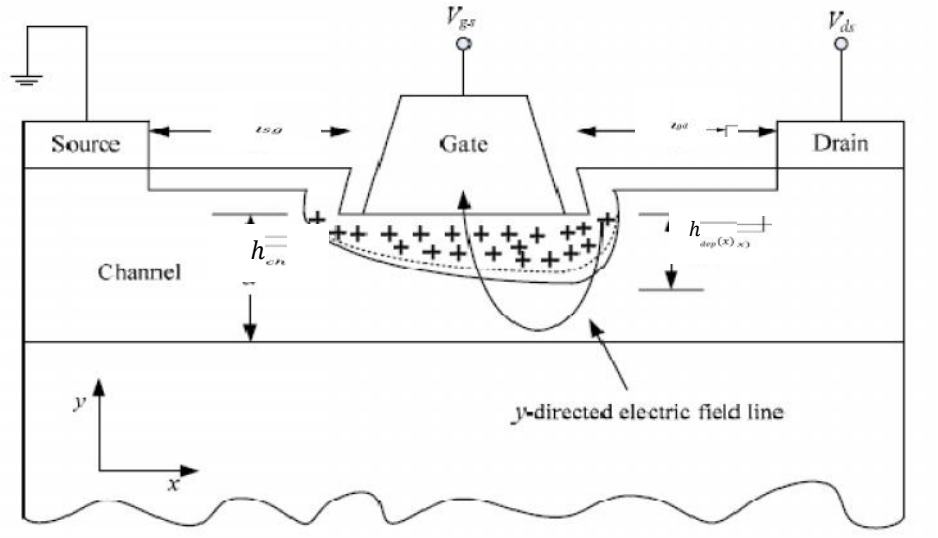


Figure III.7: Cross-sectional view of an operating GaAs MESFET indicating the depletion modification due to transverse electric field.

For long channels, according to the condition that the gate length l_g is longer than the channel thickness h_{ch}, the potential associated with the depletion region under the device boundary conditions is given by [Sze; 1981]:

$$\square_b = \frac{qh_{dep}^2 N_D}{2\varepsilon_S} \qquad \text{(III.1)}$$

where ϕ_b is the built in potential, q is the electron charge, N_D is the doping density of the channel, h_{dep} is the depletion width, and ε_s is the permittivity of the semiconductor (GaAs). According to [Yang; 1978], the threshold voltage is related to the gate-source voltage V_{gs} and the drain bias V_{ds} as follow:

$$V_{th} = \phi_b - V_{gs} + V_{ds} \tag{III.2}$$

III.2.2.1 Intrinsic elements

From the MESFET square law of the drain current as given in [Yang; 1978], the transconductance g_m and the output conductance g_{ds} are as follow:

$$g_m = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{Vd=cst} = \frac{q^2 N_D^2 \mu h_{dep}^3 w_{dev}}{2\varepsilon_s l_g V_{th}} \left[\sqrt{\frac{\phi_b - V_{gs}}{V_{th}}} - 1\right] \tag{III.3}$$

$$g_{ds} = \left.\frac{\partial I_{ds}}{\partial V_d}\right|_{Vgs=cst} = \frac{q^2 N_D^2 \mu h_{dep}^3 w_{dev}}{2\varepsilon_s l_g V_{th}} \tag{III.4}$$

where I_{ds} is the drain current. The intrinsic gate-source C_{gs} and gate- drain C_{gd} capacities are given as [Memon; 2008]:

$$C_{gs} = \left(\frac{\pi}{2} + \frac{l_g}{h_{dep}}\right)\varepsilon_s w_{dev}\,, \quad C_{gd} = \frac{\pi}{2}\varepsilon_s w_{dev} \tag{III.5}$$

here the quantities w_{dev} and h_{dep} denote the device width and depletion width, respectively. The dc resistance R_{dc} under the gate is given as [Ahmed; 995]:

$$R_{dc} = \frac{3 v_s l_g}{\mu I_{ch}} \tag{III.6}$$

where I_{ch} is the channel current (I_{ch}=$I_{ds} - I_{sub}$, with I_{sub} the substrate current) and μ is the carriers mobility. Since the ac resistance is approximately one third of the dc resistance, [Ladbrooke; 1991] gives the channel resistance as

$$R_i = \frac{v_s l_g}{\mu . I_{ch}} \tag{III.7}$$

III.2.2.2 Parasitic inductances L_g, L_d and L_s

The parasitic inductances come up from the metal contact pads of the device [Golio; 1991]. Their values are dependent upon the surface features of the device [Khalaf; 2000, Ladbrooke; 1991]. For short gate length devices, L_g is usually the largest and a function of the specific circuit topology. The value of L_g is given as [Ladbrooke; 1989]:

$$L_g = \frac{h u_{fp}}{p_s^2 l_g} w_{dev} \tag{III.8}$$

where p_s is the number of parallel strips into which the total gate-width is divided, μ_{fp} is the free space permeability. Due to the impact of the parasitic inductances on device performance, especially at high frequencies, an accuracy characterization is required. The typical values of L_g and L_d are on the order of 5 to 10 pH, while L_s is often smaller, around 1 pH for on wafer and chip devices. The package and bond wires, in a range of 100-300pH, add additional parasitic inductances that in many cases dominate the device parasitics, and must be accounted for in the circuit model.

III.2.2.3 Parasitic resistances R_s, R_d and R_g

R_g, the gate resistance that physically arises from the metallization resistance of the Schottky contact, is given by:

$$R_g = \frac{\rho w_{dev}}{3.p_S^2 H.l_g} \qquad \text{(III.9)}$$

where ρ is the resistivity and H is the height of the gate strip. Resistances R_s and R_d are introduced to account for the respective resistive contacts of source and drain as well as for any bulk resistance leading to the active channel. Their values are on the order of ohms [Tuzun; 2006].Investigation and measurements show a slight bias dependent behavior of these resistances. They are given by:

$$R_s = R_c + \frac{l_{sd}}{q\mu_p N_D w_{dev}} \frac{1}{h_{ch}}, \qquad R_d = R_c + \frac{l_{gd}}{q\mu_p N_D w_{dev}} . \frac{1}{h_{ch}} \qquad \text{(III.10)}$$

where R_c is the resistance representing the ohmic contacts, l_{sg} is the source-to-gate length, l_{gd} is the gate-to-drain length and h_{ch} is the channel thickness.

III.2.2.4 Parasitic capacitances C_{pg} and C_{pd}

The parasitic capacitances come primarily from the stray capacitance between the metal pads. As the inductors, the capacitances are related to the device structure, where the pad capacitance consists on the crossover capacitance of the metal lines and the capacitance between the pad and the back face of the semi-insulating substrate, usually connected to the source terminal. Nevertheless, it is usually known that the crossover capacitance is much smaller than the substrate capacitance [Dilorenzo and Khandelwal; 1982].Note that the pad capacitances C_{pg} and C_{pd} could be ignored for on-wafer devices (~1pF).

III.2.2.5 Cut-off frequency

The cut-off frequency, f_t, can be defined as the frequency at which $\left|\frac{I_{ds}}{I_g}\right|$ falls to one under short circuit output conditions. As shown in Figure III.8, we have

$$I_{ds} = g'_m V'_{gs} \quad with \quad g'_m = \frac{g_m}{1+g_m R_s} \tag{III.11}$$

I_g is the gate to source current. By applying Kirchoff' law, one can get:

$$I_g = jw_{Av}(C_{gs} + C_{gd})V'_{gs} \tag{III.12}$$

Taking these last two equations under unity gain condition leads to

$$\left|\frac{I_{ds}}{I_g}\right| = \frac{g'_m}{jw_{Av}(C_{gs}+C_{gd})} \tag{III.13}$$

After taking into account the pad capacitances $C_p = C_{pg} + C_{pd}$the cut-off frequency expression can be expressed as

$$f_t = \frac{g'_m}{2\pi(C_{gs}+C_{gd}+C_p)} \tag{III.14}$$

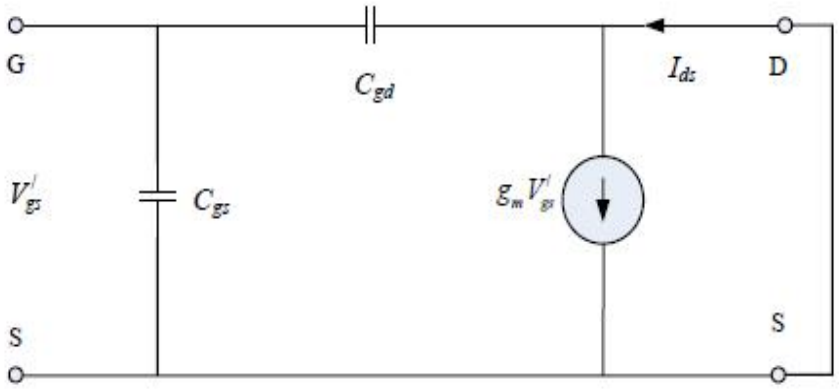


Figure III.8: The equivalent circuit of a GaAs MESFET with short drain-source terminals.

III.2.2.6 Transconductance delay

Due to instantaneous changes in gate voltage, the drain current I_{ds} needs some delay to respond, quantified by the transconductance delay. The physically meaning of the transconductance delay is the necessary time for the charge to redistribute itself after a changing in gate voltage [Golio; 1991]. The typical value of τ is 1ps for microwave MESFETs and it tends to decrease when l_g decreases [Diamond and Laviron; 1982]. It is given by

$$\tau = \frac{C_{gs}+C_{gd}}{g'_m} \tag{III.15}$$

III.3 Small-signal model

III.3.1 Introduction

The GaAs FET small-signal model is extremely important for microwave circuit design. Small-signal models provide a link between the measured S-parameters and the electrical processes occurring within the device. Each equivalent circuit element provides a lumped element approximation to some aspect of the device physics.

A physically meaningful circuit topology provides an excellent match to the measured S-parameters over a wide frequency range. When equivalent circuit elements are properly extracted, the model can be valid even beyond the frequency range of measurements; thus, providing the possibility of extrapolating device performance to frequencies beyond existing measurement capabilities.

Furthermore, accurate small-signal modelling is also the basis for accurate large-signal and noise modelling. In this work, we investigated both cold-FET and hot-FET techniques with conventional small-signal parameter extraction methodologies. For most of these traditional small-signal modelling methods, the results of some extrinsic parameters vary more or less with different biasing conditions which would decrease the accuracy of its S-parameter performance. For instance, in Dambrine's model [Dambrine; 1988], the calculated parasitic capacitor C_{pd} varies with the V_{gs} values under which the cold-FET measurement data is collected.

Moreover, for all traditional methods using the Cold-FET approach, a very large forward gate current is adopted, which would produce an irreversible damage to the transistor. To solve these problems, a novel analytical extraction method for extrinsic and intrinsic FET parameters is proposed. This analytical method could eliminate the conventional cold-FET and hot-FET modelling constraints and allows an ease in inline process tracking. The resulting extrinsic small-signal parameters are independent of biasing voltage. In addition, a better S-parameter agreement can be achieved compared to conventional methods.

III.3.2 Parameter extraction technologies for GaAsFET Small-signal model

III.3.2.1 De-embedding technique

Figure III.4 shows a typical GaAs FET small-signal equivalent circuit. Since the intrinsic device exhibits a PI topology, it is more convenient to use the admittance parameters (Y-parameters) to characterize its electrical properties. Once the values of the parasitic components are known, their effects on the measured device properties can be removed from

the device characteristics through matrix operations. As a result, the intrinsic device Y-parameters (or S-parameters) can be derived. This process is called de-embedding. The de-embedding technique is also critical for accurate device measurement because high-frequency measurements are always influenced by parasitic effects due to external elements like chip influences, packaging, and test fixture. This makes the determination of the model parameters for the intrinsic device complicated. It is possible to measure and characterize the parasitic components of the chip, the package of the transistor or the test fixture alone. After de-embedding, measured device data can be transferred to the inner device. The MESFET parasitics are either in series or in parallel with the intrinsic device. Thus, the de-embedding of series and parallel parasitic elements form the basis for the de-embedding procedure.

III.3.2.2 De-embedding procedure of typical FET device parasitics

Figure III.9 summarizes the parasitic de-embedding method for extracting the intrinsic device Y-parameters [Jingyi; 2002]. It has the following procedures:

1- Measure the device S-parameters at the extrinsic plane (denoted as S_{total}).

2- Convert scattering S-parameters (S_{total}) to admittance Y-parameters (Y_{total}) and then, subtract C_{pg} and C_{pd}. This will remove the parallel parasitic capacitor effects.

3- Convert the obtained admittance Y-parameters to impedance Z-parameters and then, subtract the parasitic resistors R_g, R_d, R_s and the parasitic inductors L_g, L_d, L_s. This will remove the series parasitic component effects leading to the intrinsic device Z-parameters denoted as Z_{in}.

4- Convert intrinsic Z-parameters Z_{in} to either Y-parameters Y_{in} or S-parameters S_{in} depending on the desired intrinsic device description.

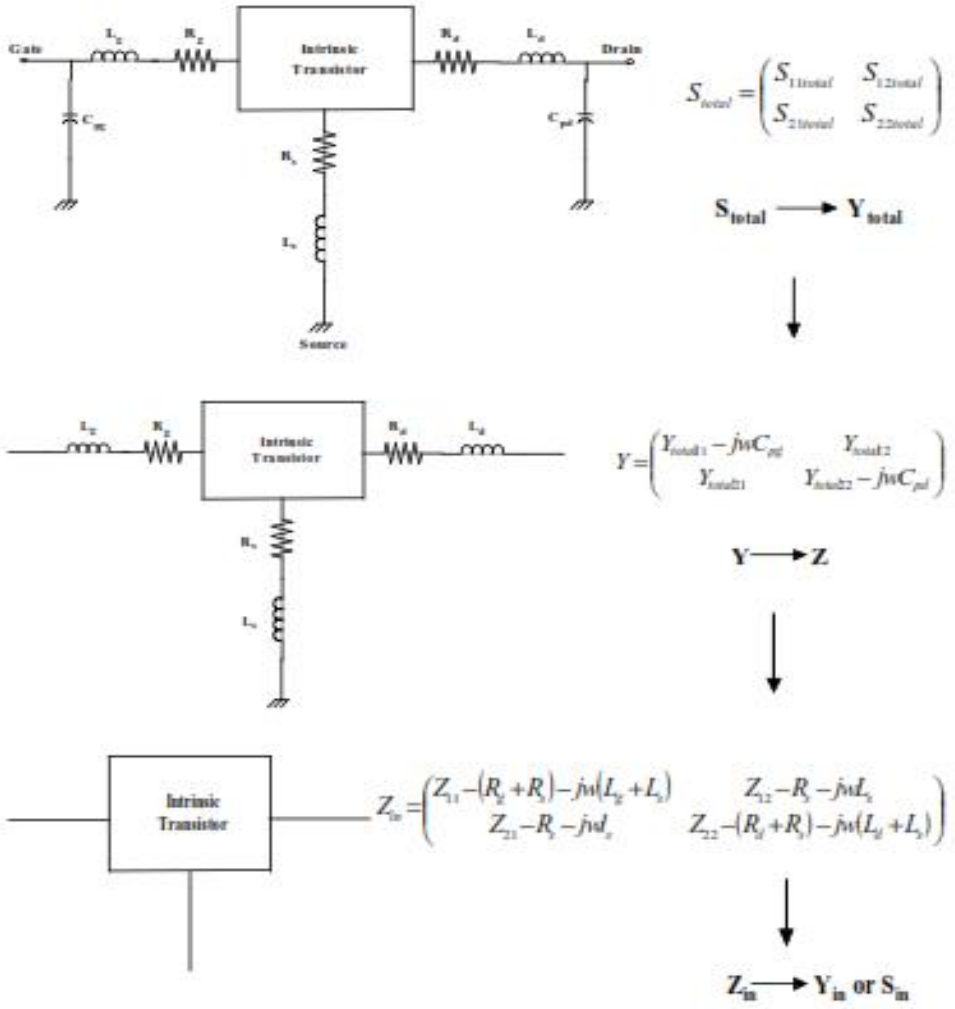


Figure III.9: De-embedding method for extracting intrinsic the admittance matrix [Jingyi; 2002, Zheng; 2010].

III.3.3 Cold-FET Techniques

Figure III.4 shows the most frequently circuit topology used for FET modeling up to 40 GHz. The extrinsic elements include parasitic resistances R_g, R_d, R_s, parasitic capacitances C_{pg}, C_{pd}, and parasitic inductances L_g, L_d, L_s. Cold-FET techniques determine these parasitic elements from S-parameter data measured at various V_{gs} values, with V_{ds}=0.

III.3.3.1 Extraction of parasitic resistances and inductances

Parasitic resistances and inductances are computed from the measurement of S-parameters with DC forward gate bias ($V_{gs}>V_{bi}>0$) and floating drain for different I_{gs} currents [Jingyi; 2002, Zheng; 2010]. The considered approach is that of Dambrine [Dambrine; 1988], in which the influence of parasitic capacitances C_{pg} and C_{pd} are neglected. Thus, a simple model is proposed as below.

$$Z_{11} = R_s + R_g + \frac{R_{ch}}{3} + \frac{n_s KT}{qI_{gs}} + j\omega\left(L_s + L_g\right) \quad \text{(III.16)}$$

$$Z_{12} = Z_{21} = R_s + \frac{R_{ch}}{2} + j\omega L_s \quad \text{(III.17)}$$

$$Z_{22} = R_s + R_d + R_{ch} + j\omega(L_s + L_d) \quad \text{(III.18)}$$

In some models, the effect of parasitic capacitances C_{pg} and C_{pd} is considered. This approach gives better L_s extraction. Under forward gate bias (V_{gs}>V_{bi}> 0) conditions, the equivalent circuit is the one shown in Figure III.10. The corresponding Z-parameters are expressed as follows [Reynoso-Hernandez et al; 1996, Reynoso-Hernandez et al; 1997].

$$Z_{11}(\omega) = \left\{(R_1 + R_3) + \omega^2 C_{pg}(R_1 + R_3)(L_s - C_{pd}R_3^2)\right\} + j\omega\left\{\left(L_s + L_g\right) - C_{pd}R_3^2 + C_{pg}(R_1 + R_3)^2\right\} \quad \text{III.19}$$

$$Z_{12}(\omega) = \left\{R_3 + \omega^2 L_s\left[C_{pd}(R_2 + R_3) + C_{pg}(R_1 + R_3)\right]\right\} + j\omega\left\{L_s - R_3\left[C_{pd}(R_2 + R_3) + C_{pg}(R_1 + R_3)\right]\right\} \quad \text{III.20}$$

$$Z_{22}(\omega) = \left\{(R_2 + R_3) + \omega^2 C_{pd}(R_2 + R_3)(L_s - C_{pg}R_3^2)\right\} + j\omega\left\{(L_s + L_d) - C_{pg}R_3^2 + C_{pd}(R_2 + R_3)^2\right\} \quad \text{III.21}$$

with

$$R_1 = R_g - \frac{R_{ch}}{6} + \frac{n_s KT}{qI_{gs}},$$

$$R_2 = R_d + \frac{R_{ch}}{2},$$

$$R_3 = R_s + \frac{R_{ch}}{2}.$$

R_{ch} is the channel resistance at cold-FET (V_{gs}>V_{bi}) condition, n_s is the ideality factor.

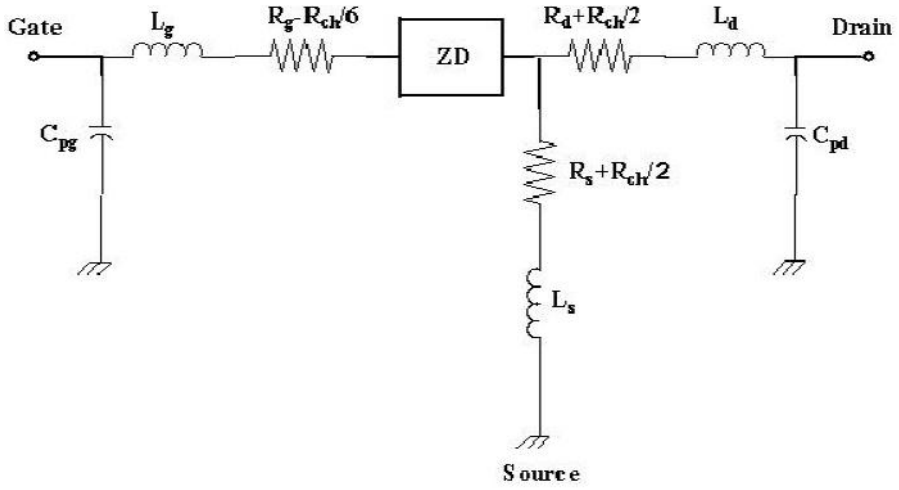


Figure III.10: Small-signal equivalent circuit with floating drain at $V_{gs}>V_{bi}>0$ [Jingyi; 2002].

Real parts of Cold-FET Z-parameters are used to determine the parasitic resistors. At low frequencies (below 5GHz), the "ω^2" terms in the above equations can be ignored.

Thus, the {Re (Z_{ij}), with i,j = 1, 2}, depend only on the access resistances. R_s, R_d and R_{ch} are directly extracted from Re(Z_{12}) and Re(Z_{22}), respectively. As for Re(Z_{11}), the extraction of the access resistances is achieved by noting that the plot of Re(Z_{11}) versus 1/I_{gs} is a straight line. Re$(Z_{11})_0$, the intercept point of the plot with the y-axis, is equal to

$$Re(Z_{11})_0 = R_s + R_g + \frac{R_{ch}}{2} \qquad \text{(III.22)}$$

By neglecting R_{ch}, we can found:

$$R_s = Re(Z_{12}) \qquad \text{(III.23)}$$

$$R_d = Re(Z_{22}) - Re(Z_{12}) \qquad \text{(III.24)}$$

$$R_g = Re(Z_{11})_0 - Re(Z_{12}) \qquad \text{(III.25)}$$

Under the same conditions, the parasitic inductances are evaluated from the imaginary parts of the cold-FET Z-parameters as:

$$L_s = \frac{Im(Z_{12})}{\omega} + A_s \qquad \text{(III.26)}$$

$$L_d = \frac{Im(Z_{22}) - Im(Z_{12})}{\omega} + A_d \qquad \text{(III.27)}$$

$$L_g = \frac{Im(Z_{11}) - Im(Z_{12})}{\omega} + A_g \qquad \text{(III.28)}$$

with

$$A_s = \left[C_{pd}(R_2 + R_3) + C_{pg}(R_1 + R_3)\right],$$

$$A_d = C_{pd}R_2(R_2 + R_3) - C_{pg}R_1R_3\ ,$$

$$A_g = C_{pg}R_1(R_1 + R_3) - C_{pd}R_2R_3.$$

III.3.4 Hot-FET Techniques

The intrinsic elements of the MESFET equivalent circuit are usually determined from Hot-FET (V_{ds}>0) S-parameter measurement data after de-embedding the extrinsic elements. Two intrinsic elements extraction approaches based on hot-FET techniques are most commonly used namely, the analytical methods [Dambrine; 1988].

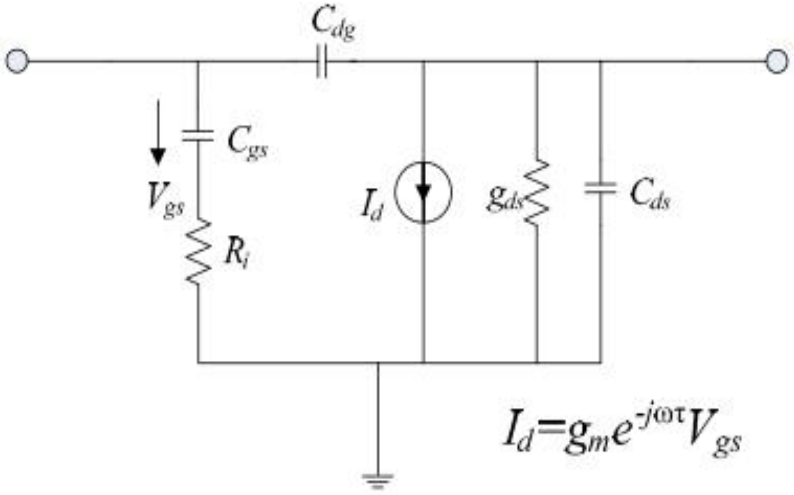


Figure III.11: The small-signal equivalent circuit for intrinsic device of GaAs MESFET [Jingyi; 2002]

In the analytical method, the intrinsic elements are directly derived from the intrinsic Y-parameters. Figure III.11 shows the small-signal equivalent circuit for the intrinsic device of GaAs MESFET. From this equivalent circuit topology, the intrinsic device Y-parameter matrix has the following expression:

$$Y_{int} = \begin{bmatrix} \frac{sC_{gs}}{1+sR_iC_{gs}} + sC_{dg} & -sC_{dg} \\ \frac{g_m \exp(-s\tau)}{1+sC_{gs}R_i} - sC_{dg} & g_{ds} + s(C_{dg} + sC_{gs}) \end{bmatrix} \qquad \text{(III.29)}$$

where s is equal to jw. The intrinsic Y-parameters of the device are then given by:

$$Y_{11} = \frac{R_iC_{gs}^2\omega^2}{D} + j\omega\left(\frac{C_{gs}}{D} + C_{gd}\right) \qquad \text{(III.30)}$$

$$Y_{12} = -j\omega C_{gd} \quad \text{(III.31)}$$

$$Y_{21} = \frac{g_m \exp(-j\omega\tau)}{1+jR_i C_{gs}\omega} - j\omega C_{gd} \quad \text{(III.32)}$$

$$Y_{22} = g_d + j\omega\left(C_{ds} + C_{gd}\right) \quad \text{(III.33)}$$

where $D = 1 + R_i C_{gs}^2 \omega^2$. For low-noise devices and at low frequencies (less than 5 GHz as stated in [Dambrine; 1988]), the term $R_i C_{gs}^2 \omega^2 < 0.01$ and $D = 1$.

By separating the Y-matrix into real and imaginary parts, the elements of the small-signal equivalent circuit can be determined analytically as follows [Dambrine; 1988]:

$$C_{gd} = -\frac{Im(Y_{12})}{\omega} \quad \text{(III.34)}$$

$$C_{gs} = -\frac{Im(Y_{11})-\omega C_{gd}}{\omega}\left(1 + \frac{\left(Re(Y_{11})\right)^2}{\left(Im(Y_{11})-\omega C_{gd}\right)^2}\right) \quad \text{(III.35)}$$

$$R_i = \frac{Re(Y_{11})}{\left(Im(Y_{11})-\omega C_{gd}\right)^2+\left(Re(Y_{11})\right)^2} \quad \text{(III.36)}$$

$$g_m = \sqrt{\left(\left(Re(Y_{21})\right)^2 + \left(Im(Y_{21}) + \omega C_{gd}\right)^2\right)\left(1 + \omega^2 C_{gs}^2 R_i^2\right)} \quad \text{(III.37)}$$

$$\tau = \frac{1}{\omega} arcsin\left(\frac{-\omega C_{gd} - Im(Y_{21}) - \omega C_{gs} R_i Re(Y_{21})}{g_m}\right) \quad \text{(III.38)}$$

$$C_{ds} = \frac{Im(Y_{22})-\omega C_{gd}}{\omega} \quad \text{(III.39)}$$

$$g_{ds} = Re(Y_{22}) \quad \text{(III.40)}$$

III.4 MESFET Nonlinear properties: Large-signal models

Large-signal models are required for circuit simulation in predicting large-signal and/or nonlinear performance. In fact, a large-signal model is required when the circuit is subject to large time-varying signals carried over a constant bias. The signal is usually large enough that the nonlinearity of the device cannot be ignored.

A typical equivalent circuit for a MESFET large-signal model is shown in Figure III.12. The equivalent circuit is divided into the extrinsic parasitic elements and the intrinsic device as in the case of small-signal. The extrinsic elements include C_{pg}, C_{pd}, L_g, L_d, L_s, R_g, R_d, and R_s, which are bias-independent. The intrinsic device is enclosed into the dashed-line box.

Among the elements kept in the dashed-line box, the nonlinear elements could include the drain source current I_{ds}, the gate capacitances C_{gs} and C_{gd}, as well as the diodes D_{gs} and D_{gd}. The drain source current is usually considered as the main non linear source. The expression of the transconductance and the output conductance are derived from the current I_{ds}. The behavior of the depletion region under the gate is represented by the capacitances C_{gs} and C_{gd}. The diode D_{gs} represents the forward-bias gate current while the diode D_{gd} is included to model the drain-gate avalanche current.

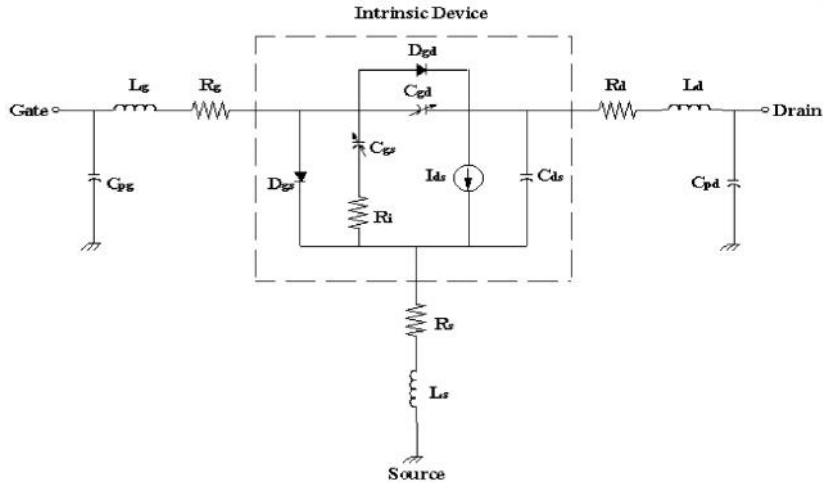


Figure III.12 Equivalent circuit for MESFET large-signal model [Jingyi; 2002].

III.5 Nonlinear transistor models

Many different models have been proposed to predict MESFET characteristics [Golio; 1991, Rodriguez and England; 1992].They can be classified into two groups namely, physical models and numerical models.

Despite their accuracy, numerical models with field-dependent characteristics of carrier velocity in the channel are not suitable for use in circuit design simulators due to their complexity and the large number of parameters involved. A DC model based on device fabrication parameters, known as physical model is generally preferred by designers assuming that it can predict the device characteristics to a reasonable accuracy [Golio; 1991].

III.5.1 Curtice quadratic model

A good FET model for circuit simulator was first proposed by V.Tuyl [Tuyl and Liechti; 1974]. Later, Curtice modified the model [Curtice; 1980] which is now known as Curtice quadratic FET model. The Curtice model describes I_{ds} as a function of V_d and V_{gs} as:

$$I_{ds} = \beta (V_{gs} - V_{th})^2 \times \tanh(\square\, V_d)\,(1 + \lambda V_d) \qquad \text{(III.41)}$$

The variable α is used to simulate the linear region *I-V* characteristics, β is the transconductance parameter and λ predicts the dependence of I_{ds} on V_d after the onset of the current saturation. Hyperbolic tangent function is used to simulate I_{ds} for $0 \leq V_d \leq V_{breakdown}$. Based on equation III.41, g_m and g_d expressions are given respectively as

$$g_m = \frac{2\, I_{ds}}{V_{gs} - V_{th}} \qquad \text{(III.42)}$$

$$g_d = I_{ds}\left(\frac{\lambda}{1+\lambda V_d} + \frac{2\alpha}{\sinh(2\alpha V_d)}\right) \qquad \text{(III.43)}$$

The observed and simulated I-V characteristics of a submicron GaAs MESFET in FigureIII-13-(a) reveal that the Curtice model performance is relatively better in the linear region whereas it deteriorates significantly in the saturation region of operation. Thus, for submicron GaAs MESFETs, the model performance is not within acceptable margin. The values of g_m and g_d given by Equations III.42 and III.43, respectively, are in good agreement with experimental data as shown in Figures.III.13-(b) and -(c) (at V_{gs}= 0V). . On the other hand, the model does not predict well the values of g_m (V_{gs}) for the device under consideration, as shown in Figure III.13-b. Hence, one can conclude that the Curtice quadratic model is not suitable to predict DC characteristics of a submicron GaAs MESFET.

III.5.2 Materka model

Based on the work of T.Taki [Taki; 1978], Materka proposed the following expression for I_{ds} (V_{gs}, V_{ds}) characteristics [Kacprzak and Materka; 1983]:

$$I_{ds} = I_{dss}\left[1 - \frac{V_{gs}}{V_{th}+\gamma V_d}\right]^2 \times tanh\left[\frac{\alpha V_d}{V_{gs}-V_{th}-\gamma V_d}\right] \qquad \text{(III.44)}$$

$$g_m = 2I_{ds}\left[\frac{\sinh\left(\frac{2\alpha V_d}{V_{gs}-V_{th}-\gamma V_d}\right)-1}{(V_{gs}-V_{th}-\gamma V_d)\sinh\left(\frac{2\alpha V_d}{V_{gs}-V_{th}-\gamma V_d}\right)}\right] \qquad \text{(III.45)}$$

$$g_d = 2I_{ds}\left[\left(1 + \frac{1}{V_{gs}-V_{th}-\gamma V_d}\right) + \frac{\gamma V_{gs}}{(V_{th}+\gamma V_d)(V_{gs}-V_{th}-\gamma V_d)}\right] \qquad \text{(III.46)}$$

The hyperbolic tangent function in equation III.44 goes to unity for higher values of V_d which is the case when $V_d > V_{sat}$, then equation III.44 for γ= 0 is reduced to the Shockley equation as

$$I_{ds} = I_{dss}\left[1 - \frac{V_{gs}}{V_{th}}\right]^2 \qquad \text{(III.47)}$$

So, after the onset of current saturation, Materka model expression is the same as that of Shockley square law expression.

In submicron GaAs MESFETs, the value of g_d in the saturation region is usually positive which eventually increases the value of $V_{th.}$ Thus, in Materka model, $V_{th} + \gamma V_d$ term is used to simulate the change in V_{th} as a function of V_d.

Using that model, the I-V characteristics of a submicron GaAs MESFET have been plotted in Figure III.14 (a). It is clear that there is no accordance between observed and simulated characteristics, which demonstrates the failure of Materka model. This is due to the inability of the model to simulate finite value of g_d in the saturation region which is usually observed in short channel MESFETs. The corresponding g_m and g_d are shown in Figure III.14 (b) and-(c), respectively.

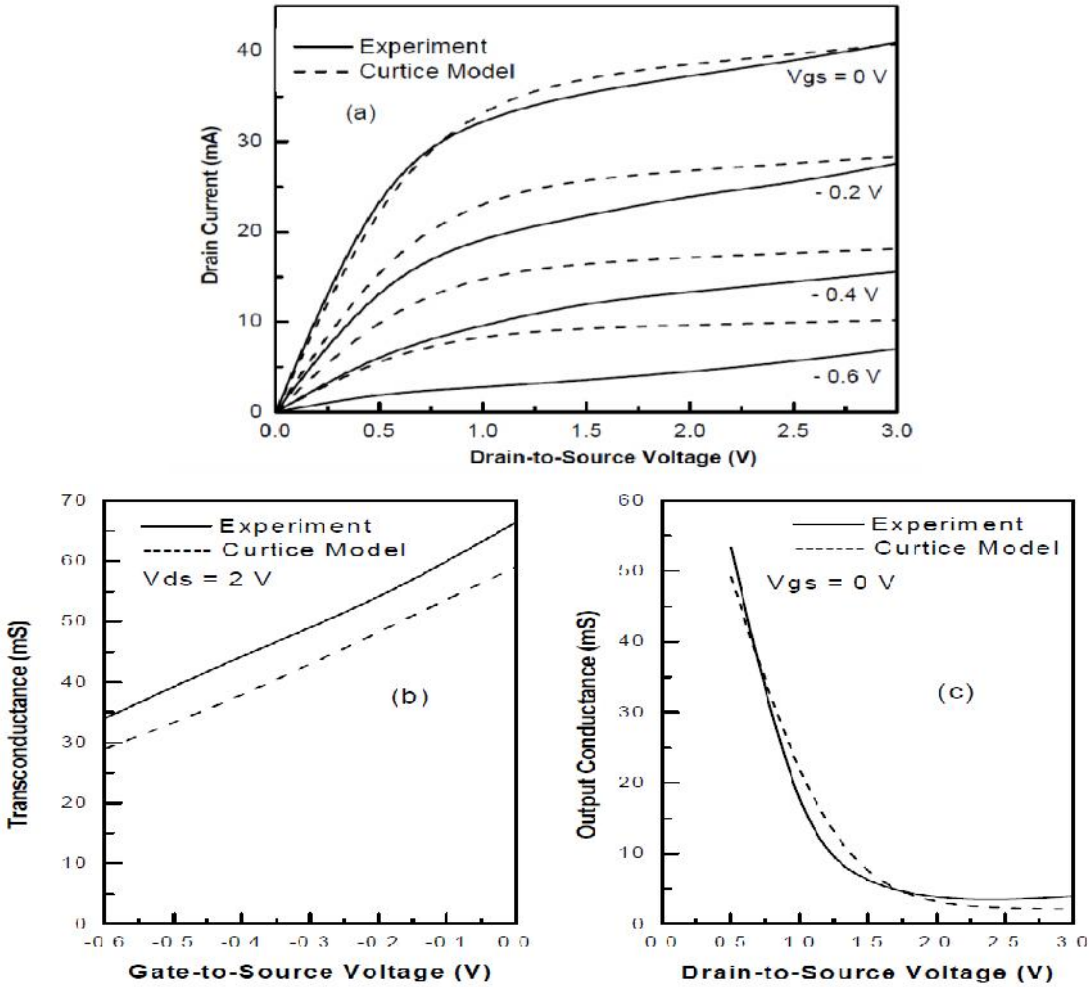


Figure III.13: Observed and simulated characteristics of a 0.28 x 150 µm^{2}GaAs MESFET by using Curtice quadratic DC model (a) output I-V characteristics, (b) transconductance and (c) output conductance [Memon; 2008].

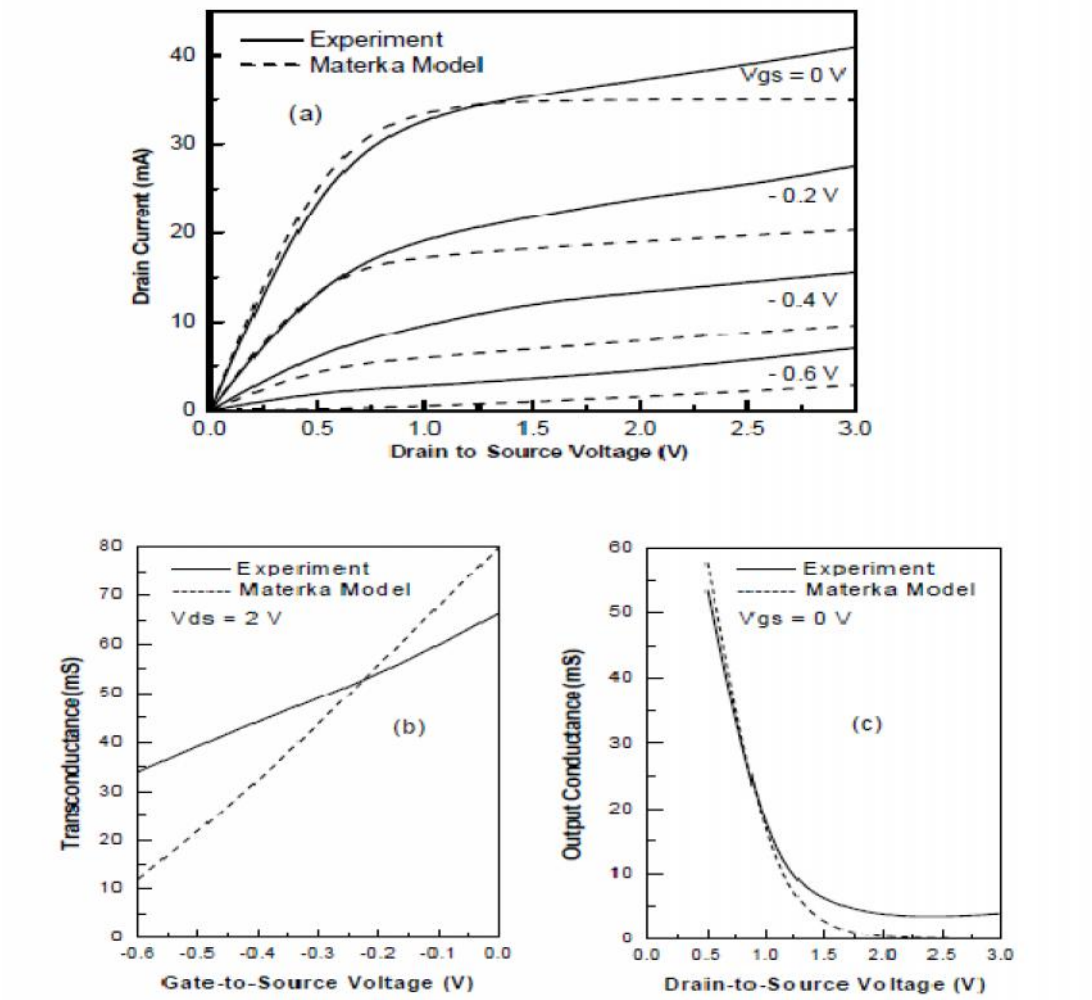


Figure III.14: Observed and simulated characteristics of a 0.28 x 150 µm^{2}GaAsMESFET by using Materka nonlinear DC model (a) output I-V characteristics,(b) transconductance and (c) output conductance [Memon; 2008].

III.5.3 Statz model

The Statz model has been proposed to simulate I_{ds} (V_d, V_{gs}) characteristics by using the following expression [Statz et al; 1987]:

$$I_{ds} = (1 + \lambda V_d)\left(\frac{\beta(V_{gs}-V_{th})^2}{1+\delta(\beta(V_{gs}-V_{th})}\right) \times \left[1 - \left[1 - \frac{\propto V_d}{3}\right]^3\right] for\ 0 < V_d < \frac{3}{\propto} \qquad \text{(III.48)}$$

$$I_{ds} = (1 + \lambda V_d)\left(\frac{\beta(V_{gs}-V_{th})^2}{1+\delta(\beta(V_{gs}-V_{th})}\right) for V_d \geq \frac{3}{\propto} \qquad \text{(III.49)}$$

Here δ defines the voltage range transition and other variables have usual meanings. The magnitude of g_m, based on equation (III.48), can be expressed as:

$$g_m = \begin{cases} \frac{I_{ds}}{\beta^2(V_{gs}-V_{th})^2} for\ 0 < V_d < \frac{3}{\propto} \\ \frac{I_D}{\beta^2(V_{gs}-V_{th})^2} forV_d \geq \frac{3}{\propto} \end{cases} \quad \text{(III.50)}$$

and

$$g_d = \begin{cases} \frac{\lambda I_{ds}}{1+\lambda V_d} + \propto I_{ds}(1 - \frac{\propto V_{DS}}{3}) for\ 0 < V_d < \frac{3}{\propto} \\ \frac{\lambda I_{ds}}{1+\lambda V_d} forV_d \geq \frac{3}{\propto} \end{cases} \quad \text{(III.51)}$$

with

$$I_{ds} = I_{ds0}(1 + \lambda V_d)$$

$$I_{ds0} = \frac{\beta(V_{gs} - V_{th})^2}{1 + \delta(V_{gs} - V_{th})}$$

The Statz model is relatively complicated compared to the two other models discussed above. It is polynomial in nature and difficult to handle. The basic parameters of a physical model have been dealt with in a complicated manner and the square law rule given by the Shockley equation has been violated.

Figure.III.15 shows the simulated and the measured characteristics for a submicron GaAs MESFETs. As for the Materka case, an inconvenient accordance between the measured and the simulated characteristics demonstrates the inability of Statz model to predict the response of the device. Examination of Figure.III.15 showed that the Statz model exhibited less gate control which could be a main reason that caused a significant discrepancy as seen in all the three plots of the Figure.

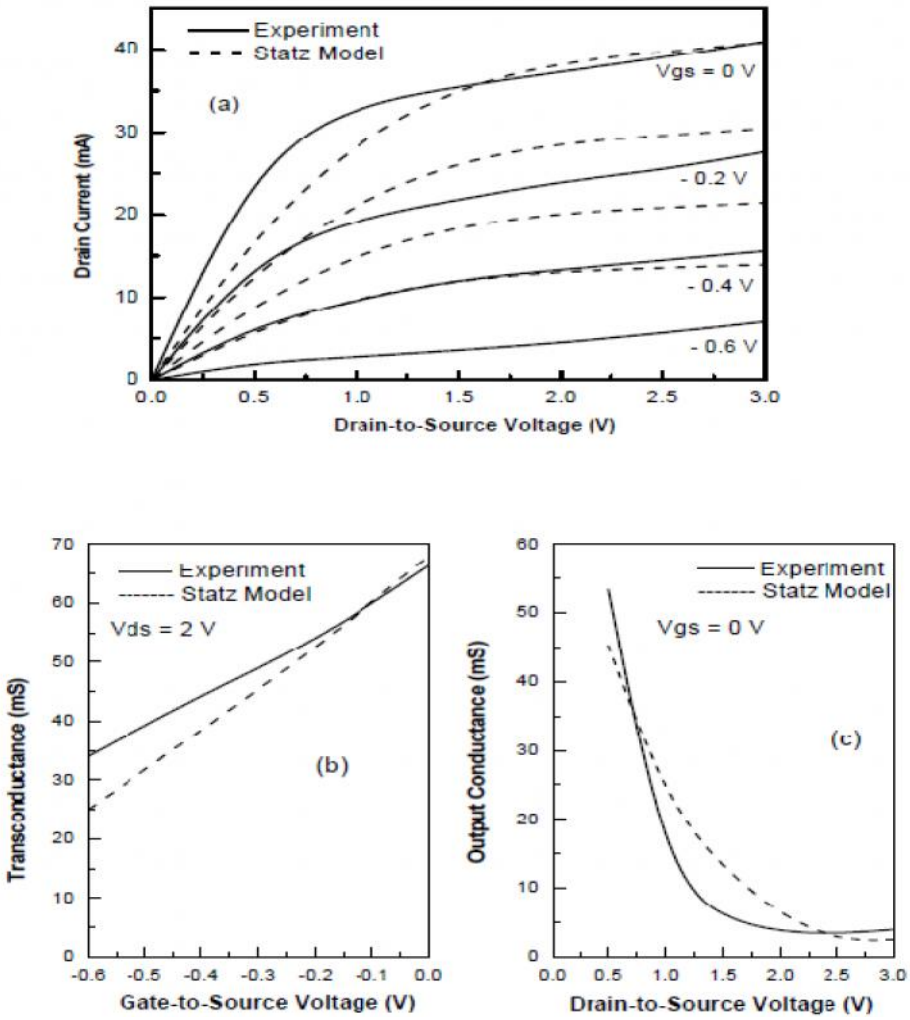


Figure III.15: Observed and simulated characteristics of a 0.28 x 150 µm^{2}GaAsMESFET by using Statz nonlinear DC model (a) output I-V characteristics, (b) transconductance and (c) output conductance[Memon; 2008].

III.5.4 Curtice Ettenberg Cubic model

The Curtice model based on the work of Curtice-Ettenberg consists of the Voltage controlled current I_{ds} given as [Curtice and Ettenberg; 1985]:

$$I_{ds} = (A_{0+}A_1V_1 + A_2V_1^2 + A_3V_1^3) \times tanh(\gamma V_d) \qquad \text{(III.52)}$$

where ¥ is the saturation parameter. The hyperbolic tangent function is used to simulate I_{ds} for the condition $0 < V_d < V_{breakdown}$ as opposed to the Shockley model which simulates I_{ds} only for $V_{sat} < V_d < V_{breakdown}$.

The transconductance g_m and the output conductance g_d are given as:

$$\begin{cases} g_m = \left(A_1V_2 + 2.A_2V_2 + 3A_3V_1^2V_2\right)tanh(¥V_d) \\ g_d = \left(A_0 + A_1V_1 + A_2V_1^2 + A_3V_1^3\right)sech^2(¥V_d)¥ - \ .V_{gs}\left(A_1 + 2.A_2V_1 + 3A_3V_1^2\right)tanh(¥V_d) + \dfrac{1}{V_{d0}} \end{cases} \quad \text{(III.53)}$$

with

$$V_1 = V_{gs}(1 + \ (V_{d0} - V_d))$$

$$V_2 = (1 + \ (V_{d0} + V_d))$$

The V_{gs} and V_d are the gate-source and drain voltages, respectively, while the parameter β models the pinch-off voltage dependence on the drain-source voltage. Parameters A_0, A_1, A_2, and A_3 are polynomial fitting coefficients, and V_{d0} is the drain-source voltage at which the polynomial coefficients are evaluated.

The drain-source and gate-drain charge and capacitance are given by:

$$\begin{cases} Q_{gs} = 2 \times V_{bi}C_{gs0}/\sqrt{1 - (V_{gs}/V_{bi})} & if V_{gs} < F_cV_{bi} \\ C_{gs} = \partial Q_{gs}/\partial V_{gs} = C_{gs0}/\sqrt{1 - (V_{gs}/V_{bi})} \end{cases} \quad \text{(III.54)}$$

$$\begin{cases} Q_{gs} = 2 \times V_{bi}C_{gs0}\left[1 - \sqrt{1 - F_c}\right] + \left[\frac{C_{gs0}}{\sqrt[3]{(1-F_c)}}\right] \\ \quad \left\{\left(1 - \frac{3*F_c}{2}\right) \times (V_{gs} - F_cV_{bi})\left(\frac{V_{gs}^2 - (F_cV_{bi})^2}{4*V_{bi}}\right)\right\} \quad if\ V_{gs} \geq F_cV_{bi} \\ C_{gs} = \partial Q_{gs}/\partial V_{gs} = \left[\frac{C_{gs0}}{\sqrt[3]{(1-F_c)}}\right] \times \left[1 - \frac{3F_c}{2} + \frac{V_{gs}}{2V_{bi}}\right] \end{cases} \quad \text{(III.55)}$$

$$\begin{cases} Q_{gd} = 2 \times V_{bi}C_{gd0}/\left[1 - \sqrt{1 - (V_{gd}/V_{bi})}\right] & if V_{gd} < F_cV_{bi} \\ C_{gd} = \partial Q_{gd}/\partial V_{gd} = C_{gd0}/\sqrt{1 - (V_{gd}/V_{bi})} \end{cases} \quad \text{(III.56)}$$

$$\begin{cases} Q_{gd} = 2 \times V_{bi}C_{gd0}\left[1 - \sqrt{1 - F_c}\right] + \left[\frac{C_{gd0}}{\sqrt[3]{(1-F_c)}}\right] \\ \quad \left\{\left(1 - \frac{3*F_c}{2}\right) \times (V_{gd} - F_cV_{bi})\left(\frac{V_{gd}^2 - (F_cV_{bi})^2}{4*V_{bi}}\right)\right\} \quad if V_{gd} \geq F_cV_{bi} \\ C_{gd} = \partial Q_{gd}/\partial V_{gd} = \left[\frac{C_{gd0}}{\sqrt[3]{(1-F_c)}}\right] \times \left[1 - \frac{3F_c}{2} + \frac{V_{gd}}{2V_{bi}}\right] \end{cases} \quad \text{(III.57)}$$

The built-in potential V_{bi} of the Schottky gate as well as the gate-source and gate-drain capacitances C_{gs0} and C_{gd0}, respectively, are measured at zero bias.

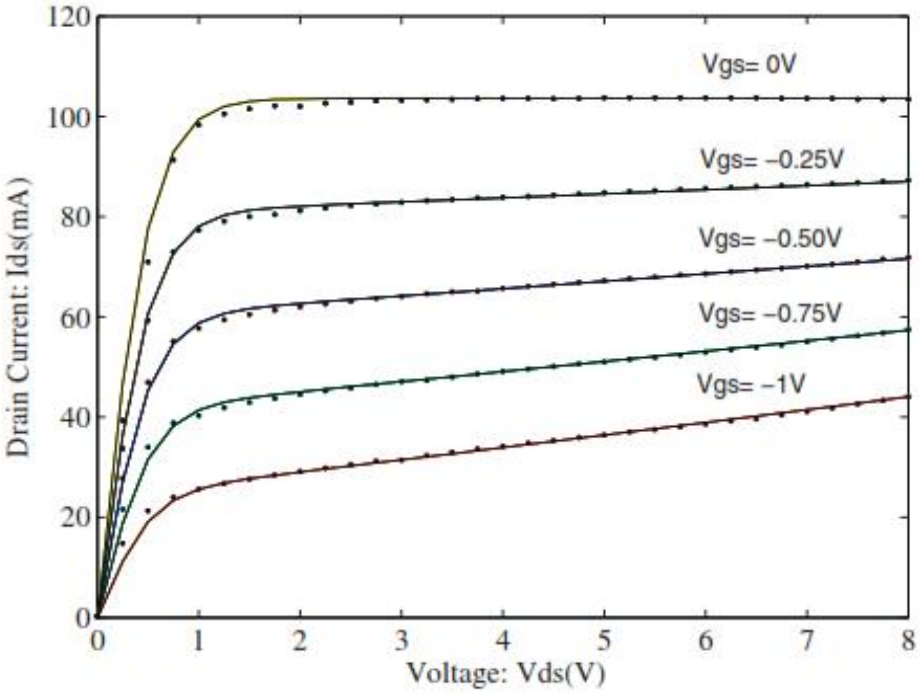


Figure III.16: A 0.7×(4×150)µm GaAs MESFET Simulated (solid line) and measured (symbol) DC characteristics for Curtice - Ettenberg model.[Samrat et al; 2009].

Figure III.16 shows a successful comparison of modeled I_{ds} vs. V_{ds} characteristics using Curtice-Ettenberg with measurement results. We will thus retain this model as the one to be used in our electrical simulations.

III.6 Finite Differential Time Domain Analysis (FDTD)

III.6.1 Introduction

Taking into consideration the increasing demand for higher performance and lower cost, monolithic microwave integrated circuits (MMICs) may include a large number of closely packed passive and active structures, several levels of transmission lines, and discontinuities on the same chip [Goswami et al; 2001]. The enhancement flow of data in telecommunications requires MMIC systems operating at high speeds, frequencies, and even sometimes, over very broad bandwidths. However, by increasing the operating frequency, modeling and simulation of devices and circuits become more challenging [Alsunaidi et al; 1996].

In fact, electromagnetic interactions must be taken into account to get a precise device modeling in particular for active devices with gate width on the order of wavelength [Alsunaidi et al; 1996]. Indeed, when the device dimensions become comparable to

wavelength, the input active transmission line, e.g., the gate electrode, presents a different reactance than the output transmission line, e.g., the drain electrode. Therefore, they exhibit different phase velocities for input and output signals. Thus, by increasing the frequency and/ or device dimensions, the phase cancellation due to the phase velocity mismatching will affect the performance of the device [Ghazaly; 1989, Ghazaly and Itoh; 1988]. In such cases, the wave propagation effect will influence the electrical performance of the device. So, this phenomena needs to be considered accurately in device modeling.

Full-wave analysis and *global modeling approach* can be used to consider the wave propagation effect along the device structure. Nevertheless, this type of analysis is time consuming and needs a huge CPU time.

Despite of some efficient numerical methods that have been recently proposed for simulation time reduction [Goasguen et al; 2001, Hussein and El. Ghazaly; 2004, Movahhedi and Abdipour; 2006(a, b)], the above approaches need more attention for implementation in a simulation software. On the other side, device behavior in high frequencies can be well described using *semi-distributed models* which can be easily implemented in CAD routines of simulators [Movahhedi and Abdipour; 2006(b), Abdipour and Pacaud; 1996, Ongareau et al; 1994,Waliullah et al; 2002]. But the semi-distributed model cannot accurately evaluate the effect of wave propagation and phase cancellation on the device performance [Alsunaidi et al; 1996].

The Finite Difference Time Domain (FDTD) method is widely used in solving various kinds of electromagnetic problems, wherein lossy, nonlinear, inhomogeneous media and transient problems need to be considered [Taflove; 1996]. By applying this modeling technique, the scattering parameters and the I-V characteristics of a sub micrometer-gate FET were obtained. The results obtained by the physical model were compared with those obtained by this method and also the measurements and as expected the proposed physical model agrees with the full-wave analysis model.

III.6.2 Model Identification

A typical millimeter-wave field effect transistor is shown in Figure III.5. Three coupled electrodes constitute the terminals of the device deposited on a thin layer of GaAs supported by a semi-insulating GaAs substrate. As operating frequency of the MESFET increases up to the millimeter (mm) wave range, the dimensions of the electrodes become comparable to the wavelength. In this situation, the transmission line properties of the electrodes need to be considered [Wang et al; 2005, Lin and Chiu; 2005, Huang; 2005].

Fully distributed models are among the accurate models that can be applied to calculate the effect of wave propagation along the MESFET electrodes.

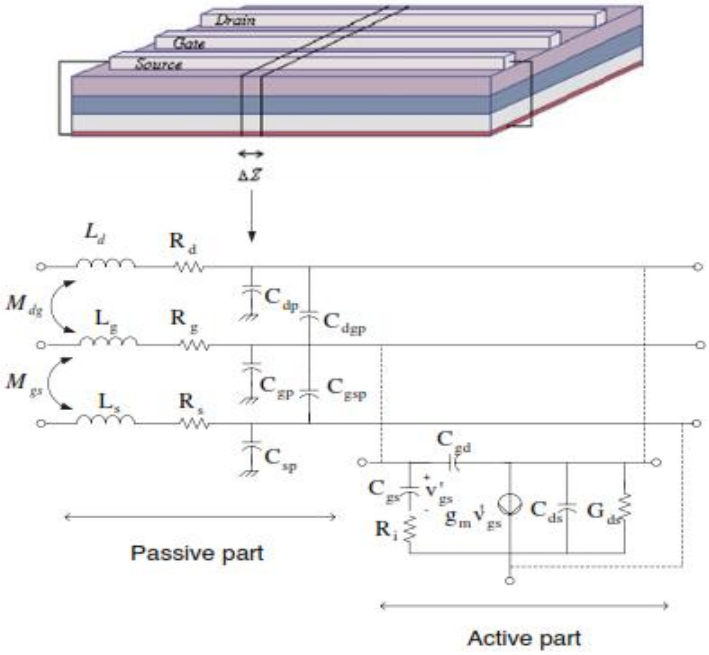


Figure III.17: An equivalent circuit model of a differential segment of the transistor (AMTL) [a linear model for the active part] [Asadi; 2011].

Since the device terminals are considered as active multiconductor transmission lines (AMTL), an equivalent circuit should be developed to model them. Thus, let us consider an infinitely small portion of the transmission line length as shown in Figure III.17. Each part is represented by a six-port equivalent circuit which combines a conventional MESFET small-signal circuit model and another circuit element to account for the coupled transmission line effects of the electrode structure where all parameters are per unit-length.

By applying kirchhoff's current and voltage laws to the left loop of the conventional FET circuit as illustrated in Figure III.17 with $\Delta x \rightarrow 0$, we obtain the following equations [Asadi; 2011]:

$$I_d(x+\Delta x,t)+C_{11}\Delta x\frac{\partial V_d(x+\Delta x,t)}{\partial t}-C_{12}\Delta x\frac{\partial V_g(x+\Delta x,t)}{\partial t}-C_{13}\Delta x\frac{\partial V_s(x+\Delta x,t)}{\partial t}$$
$$+G_m\Delta x V_g'(x,t)+G_{ds}\Delta x(V_d(x,t)-V_s(x,t))=I_d(x,t) \qquad \text{(III.58)}$$

$$V_d(x+\Delta x,t)+R_d\Delta x I_d(x,t)+L_{dd}\Delta x\frac{\partial I_d(x,t)}{\partial t}+M_{gd}\Delta x\frac{\partial I_g(x,t)}{\partial t}+M_{ds}\Delta x\frac{\partial I_s(x,t)}{\partial t}=V_d(x,t) \qquad \text{(III.59)}$$

By setting $\Delta x \rightarrow 0$, we obtain [Mondal; 1989]

$$\frac{\partial I_d(x,t)}{\partial x}+C_{11}\frac{\partial V_d(x,t)}{\partial t}-C_{12}\frac{\partial V_g(x,t)}{\partial t}-C_{13}\frac{\partial V_s(x,t)}{\partial t}+G_m V'_g(x,t)+G_{ds}(V_d(x,t)-V_s(x,t))=0 \quad \text{(III.60)}$$

$$\frac{\partial V_d(x,t)}{\partial x}+R_d I_d(x,t)+L_{dd}\frac{\partial I_d(x,t)}{\partial t}+M_{gd}\frac{\partial I_g(x,t)}{\partial t}+M_{ds}\frac{\partial I_s(x,t)}{\partial t}=0 \quad \text{(III.61)}$$

The same procedure applied for gate and source electrodes, we get similar equations:

$$\frac{\partial I_g(x,t)}{\partial x}+C_{22}\frac{\partial V_g(x,t)}{\partial t}-C_{12}\frac{\partial V_d(x,t)}{\partial t}+C_{gs}\frac{\partial V'_g(x,t)}{\partial t}=0 \quad \text{(III.62)}$$

$$\frac{\partial V_g(x,t)}{\partial x}+R_g I_g(x,t)+L_{gg}\frac{\partial I_g(x,t)}{\partial t}+M_{gd}\frac{\partial I_d(x,t)}{\partial t}+M_{gs}\frac{\partial I_s(x,t)}{\partial t}=0 \quad \text{(III.63)}$$

$$\frac{\partial I_s(x,t)}{\partial x}+C_{33}\frac{\partial V_s(x,t)}{\partial t}-C_{13}\frac{\partial V_d(x,t)}{\partial t}-C_{gs}\frac{\partial V'_g(x,t)}{\partial t}-G_m V'_g(x,t)+G_{ds}(V_s(x,t)-V_d(x,t))=0 \quad \text{(III.64)}$$

$$\frac{\partial V_s(x,t)}{\partial x}+R_s I_s(x,t)+L_{ss}\frac{\partial I_s(x,t)}{\partial t}+M_{ds}\frac{\partial I_d(x,t)}{\partial t}+M_{gs}\frac{\partial I_g(x,t)}{\partial t}=0 \quad \text{(III.65)}$$

The gate-source loop leads to another equation which could be written as

$$V'_g(x,t)+V_s(x,t)+R_i C_{gs}\frac{\partial V'_g(x,t)}{\partial t}-V_g(x,t)=0 \quad \text{(III.66)}$$

where

$$C_{11}=C_{dp}+C_{ds}+C_{dg} \qquad C_{22}=C_{dp}+C_{dg} \qquad C_{33}=C_{sp}+C_{ds}$$

$$C_{12}=C_{dg} \qquad C_{13}=C_{ds}$$

Then, the above equations could be simplified into two matrix equations as follows:

$$\frac{\partial}{\partial x}\begin{bmatrix} I_d(x,t) \\ I_g(x,t) \\ I_s(x,t) \\ 0 \end{bmatrix}+\frac{\partial}{\partial t}\begin{bmatrix} C_{11} & -C_{12} & -C_{13} & 0 \\ -C_{12} & C_{22} & 0 & C_{gs} \\ -C_{13} & 0 & C_{33} & -C_{gs} \\ 0 & 0 & 0 & R_i C_{gs} \end{bmatrix}\begin{bmatrix} V_d(x,t) \\ V_g(x,t) \\ V_s(x,t) \\ V'_g(x,t) \end{bmatrix}+ \begin{bmatrix} G_{ds} & 0 & -G_{ds} & G_m \\ 0 & 0 & 0 & 0 \\ -G_{ds} & 0 & G_{ds} & -G_m \\ 0 & -1 & 1 & 1 \end{bmatrix}\begin{bmatrix} V_d(x,t) \\ V_g(x,t) \\ V_s(x,t) \\ V'_g(x,t) \end{bmatrix}=0 \quad \text{(III.67)}$$

$$\frac{\partial}{\partial x}\begin{bmatrix} V_d(x,t) \\ V_g(x,t) \\ V_s(x,t) \end{bmatrix} + \frac{\partial}{\partial t}\begin{bmatrix} L_{dd} & M_{gd} & M_{ds} \\ M_{gd} & L_{gg} & M_{gs} \\ M_{ds} & M_{gs} & L_{ss} \end{bmatrix}\begin{bmatrix} I_d(x,t) \\ I_g(x,t) \\ I_s(x,t) \end{bmatrix} + \begin{bmatrix} R_d & 0 & 0 \\ 0 & R_g & 0 \\ 0 & 0 & R_s \end{bmatrix}\begin{bmatrix} I_d(x,t) \\ I_g(x,t) \\ I_s(x,t) \end{bmatrix} = 0 \qquad \text{(III.68)}$$

where V_d, V_g, and V_s, are the drain, gate and source voltages, respectively. V'_g is the voltage across the gate-source capacitor, and I_d, I_g and I_s are the drain, gate and source currents, respectively. These variables are time-dependent and function of the position x along the transistor width.

The proposed FET model is embodied in the linear equations.

$$\frac{\partial}{\partial x}[\mathrm{I}'(x,t)] + [\mathrm{C}]\frac{\partial}{\partial t}[\mathrm{V}'(x,t)] + [\mathrm{G}][\mathrm{V}'(x,t)] = 0 \qquad \text{(III.69-a)}$$

$$\frac{\partial}{\partial x}[\mathrm{V}(x,t)] + [\mathrm{L}]\frac{\partial}{\partial t}[\mathrm{I}(x,t)] + [\mathrm{R}][\mathrm{I}(x,t)] = 0 \qquad \text{(III.69-b)}$$

With

$$[\mathrm{I}'(x,\mathrm{t})] = \begin{bmatrix} I_d(x,t) \\ I_g(x,t) \\ I_s(x,t) \\ 0 \end{bmatrix} \quad [\mathrm{V}(x,\mathrm{t})] = \begin{bmatrix} V_d(x,t) \\ V_g(x,t) \\ V_s(x,t) \end{bmatrix} \quad [\mathrm{V}'(x,\mathrm{t})] = \begin{bmatrix} V_d(x,t) \\ V_g(x,t) \\ V_s(x,t) \\ V'_g(x,t) \end{bmatrix} \quad [\mathrm{I}(x,\mathrm{t})] = \begin{bmatrix} I_d(x,t) \\ I_g(x,t) \\ I_s(x,t) \end{bmatrix}$$

$$[L] = \begin{bmatrix} L_{dd} & M_{gd} & M_{ds} \\ M_{gd} & L_{gg} & M_{gs} \\ M_{ds} & M_{gs} & L_{ss} \end{bmatrix}, [R] = \begin{bmatrix} R_d & 0 & 0 \\ 0 & R_g & 0 \\ 0 & 0 & R_s \end{bmatrix}$$

$$[C] = \begin{bmatrix} C_{11} & -C_{12} & -C_{13} & 0 \\ -C_{12} & C_{22} & 0 & C_{gs} \\ -C_{13} & 0 & C_{33} & -C_{gs} \\ 0 & 0 & 0 & R_i C_{gs} \end{bmatrix} \qquad [G] = \begin{bmatrix} G_{ds} & 0 & -G_{ds} & G_m \\ 0 & 0 & 0 & 0 \\ -G_{ds} & 0 & G_{ds} & -G_m \\ 0 & -1 & 1 & 1 \end{bmatrix}$$

III.6.2.1 Solution of the linear system

Various time-domain methods like the finite difference time-domain (FDTD) method [Yee; 1966], the transmission line matrix (TLM) method [Sadiku; 2001], and the finite integration technique (FIT) [Wenquan; 2002] have been successfully used to solve the linear system described in equation III.69. However, there are many significant differences between these three methods in terms of CPU time and implementation complexity.

The FDTD technique was retained mainly for its simplicity and accuracy compared to the above-mentioned methods [Taflove and Hangness; 2005].

As reported in [Asadi; 2011], applications of the FDTD method to the full-wave solution of Maxwell's equations have shown that accuracy and stability of the solution can be achieved if the electric and magnetic field solution points are chosen to alternate in space and be separated by one-half the position discretization, e.g., $\Delta x/2$, and to also be interlaced in time and separated by $\Delta t/2$. The condition for this set of recursion relations to be stable is the Courant condition mentioned in [Waliullah et al; 2002] by $\Delta t \le \frac{\Delta x}{v}$, which requires the time step to be not greater than the propagation time over each cell. The Δx step is chosen sufficiently small such that each Δx section is electrically small at the operating frequency range.

Then, with applying the finite difference approximation to III.69 gives:

$$\frac{1}{\Delta x}\left([I'^{n+1/2}_{k}]-[I'^{n+1/2}_{k-1}]\right)+\frac{1}{\Delta t}[\mathrm{C}]\left([V'^{n+1}_{k}]-[V'^{n}_{k}]\right)+\frac{1}{2}[\mathrm{G}]\left([\mathrm{V'^{n+1}_{k}}]+[\mathrm{V'^{n}_{k}}]\right)=0 \quad \text{(III.70-a)}$$

$$\frac{1}{\Delta x}\left([V^{n+1}_{k+1}]-[V^{n+1}_{k}]\right)+\frac{1}{\Delta t}[\mathrm{L}]\left([I^{n+3/2}_{k}]-[I^{n+1/2}_{k}]\right)+\frac{1}{2}[\mathrm{R}]\left([\mathrm{I^{n+3/2}_{k}}]+[\mathrm{I^{n+1/2}_{k}}]\right)=0 \quad \text{(II.70-b)}$$

with

$$[V_i{}^j] \equiv [V((i-1)\Delta x,\, j\Delta t)] \qquad [V'_i{}^j] \equiv [V'((i-1)\Delta x,\, j\Delta t)]$$

$$[I_i{}^j] \equiv [I((i-\tfrac{1}{2})\Delta x,\, j\Delta t)] \qquad [I'_i{}^j] \equiv [I'((i-\tfrac{1}{2})\Delta x,\, j\Delta t)]$$

Solving these equations give the required recursion relations:

$$[V'^{n+1}_{k}]=\left(\frac{1}{\mathrm{a}t}[C]+\frac{1}{2}[G]\right)^{-1}\left\{\left(\frac{1}{\mathrm{a}t}[C]-\frac{1}{2}[G]\right)[V'^{n}_{k}]-\frac{1}{\mathrm{a}x}([I'^{n+1/2}_{k}]-[I'^{n+1/2}_{k-1}])\right\} \quad \text{(III.71)}$$

$$[\mathrm{I}^{n+3/2}_{k}]=\left(\frac{1}{\Delta t}[L]+\frac{1}{2}[R]\right)^{-1}\left\{\left(\frac{1}{\Delta t}[L]-\frac{1}{2}[R]\right)[\mathrm{I}^{n+1/2}_{k}]-\frac{1}{\Delta x}([V^{n+1}_{k+1}]-[V^{n+1}_{k}]\right\} \quad \text{(III.72)}$$

To solve the active transmission line equations, the leap-frog method was used because of its simplicity and accuracy [Taflove and Hangness; 2005]. First, the solutions started with an initially relaxed line having zero voltage and current values. Then, voltages along the electrode of transistor were solved for a fixed time from III.71 while currents were solved for from III.72.

III.7 Summary

In this chapter, we started by a brief discussion on the operation of GaAs MESFETs in microwave frequencies. Thus, a review of the existing models has been provided. First, a basic description of the MESFET device was presented. Then, after examining the basic device operations, the physical origin of each equivalent circuit element has been investigated, leading to the equivalent small signal circuit. This was followed by an overview of the small-signal model extraction. First, some important concepts for parameter extraction were addressed, including de-embedding technique and the selection of an objective function. Then, different small signal model parameter extraction approaches have been discussed, covering, both cold-FET and hot-FET techniques. This approach led to a proposed nonlinear model, which accurately considers the effect of wave propagation along the transistor electrodes. A finite differential time-domain method was adopted as an approach for analyzing such method.

Chapter IV

Results and discussions

IV.1 Introduction

This work was carried out in two stages. The first was in the Laboratory of Semiconducting and Metallic Materials (LMSM), University of Biskra. The second one was realized in the School of Electrical Engineering and Computer Science (SEECS), University of Ottawa (Canada).

The purpose of this work is to simulate the effects of substrate deep levels on the characteristics of Gallium Arsenide based -FieldEffect Transistors (GaAsFETs). Three types of GaAs FETs were investigated. The first one is a simple planar transistor, in which the channel is made of a single material, namely GaAs. This transistor is referred to as GaAs MESFET (for Metal Semiconductor Field Effect Transistor). The channel of the second and third transistor is made of several (at least three) different regions of different materials, namely GaAs, AlGaAs and InGaAs. For the two last, the purpose of the multi-material channel is to improve the carrier mobility, hence the name High Electron Mobility Transistor (HEMT) given to these types of transistors. For planar GaAsMESFETs, an in-house developed software is used to simulate the effect of different types of deep levels in the substrate on their channel conductance and is carried out in LMSM. This software uses the classic drift diffusion model (DDM) to numerically solve the partial differential equations applied to the transistor. In DDM, the average carrier energy, available in form of carrier temperature, is neglected since the transistor dimensions are large enough to justify this assumption. However for HEMTs and recessed gate MESFETs, the transistor dimensions are sub-micronics, hence the necessity to take into accounts the effects neglected in DDM. The hydrodynamic model (HDM) is an improvement of DDM since it takes into account the above mentioned phenomena. A commercial software, namely SILVACO MERCURY, is used to apply HDM in sub-micron MESFETs and HEMTs. MERCURY combines physical (HDM) and electrical modeling to calculate the DC current-voltage (I-V) characteristics as well as the AC (high frequency) scattering parameters (S-parameters) of sub-micronic MESFET and HEMTs. These sub-micronic transistors were also electrically modeled by commercial software, namely ADS (Advanced Design System), in order to compare it to HDM modeling. In ADS, the equivalent circuit parameters were obtained from the transistor data sheet using the non-linear Curtice-cubic model [Curtice; 1985]. DDM results for MESFETs were successfully compared to published results. MERCURY I-V and S-

parameters simulations of a GaAs recessed gate GaAs MESFET (Ne71000) were validated by comparing them to ADS simulation. After validation, a simulation study was carried out on the relation between the gate length, the recessed technology and the high frequency performance of HEMTs. The pseudomorphic high electron mobility transistor pHEMT was investigated. An AlGaAs/InGaAs/GaAs pseudomorphic HEMT (pHEMT) was chosen as example. Finally the effect of deep levels on the I-V characteristics and the high frequency performances of these HEMTs was simulated. All these were carried out at SEECS.

IV.2 Planar GaAs MESFET

IV.2.1. Introduction

Deep levels in the substrate of FETs have a double effect. On one hand, they are useful in the semi-insulating property of the substrate. On the other hand, they can have a degrading effect. For example, the conductance can be influenced by the presence of these deep levels and their types. Thus, they may have a significant effect on compound semiconductor device operation. The reduction of the conductance and conductance by a negative voltage applied to the substrate, termed Backgating, is numerically modelled to clarify which type of traps is responsible of this phenomenon.

IV.2.2. Sample structure

The substrate is assumed to contain shallow and deep levels. The density of deep levels is usually greater than that of shallow levels for typical semi-insulating substrates **[**Lindquist; 1977]. Deep acceptors are assumed to be located at the middle of the energy gap (E_V + 0.7 eV), which is a typical value for Cr levels in Cr-doped semi insulating GaAs widely used as substrate for GaAs FETs while deep donors are located at E_C - 0.75 eV which is a typical value for the well-known EL_2 [Kokot; 1982].The channel is n-type with a density of 10^{16} cm^{-3} shallow levels. The channel thickness is a_c= 0.2 µm, the buffer layer is six times the channel thickness and that of the substrate is a_s=10 µm. The backgating is studied for two types of devices: with and without a high purity buffer layer between the channel and the SI substrate. A schematic view of the simulated transistor is presented in Figure IV.1.

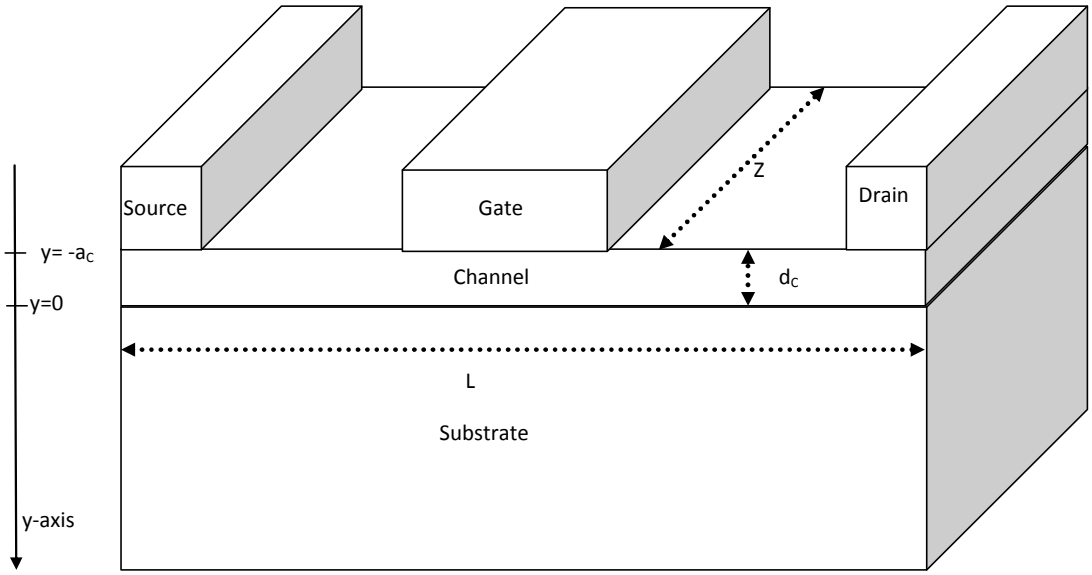


Figure IV.1: A schematic view of the simulated planar GaAs MESFET structure.

Since a bias is applied to the substrate, a depletion region is developed at the interface between the channel and the substrate. Therefore the electron density is reduced at the interface because of this depletion region. The electron density is evaluated as a function of the applied bias to the substrate in the absence or presence of different types of deep levels. A one-dimensional simulation (in the *y*-direction) was carried out to evaluate this electron density. The one-dimension simulation in this case is justified by the fact that the channel is very long and the applied voltage between the drain and the source is very small to keep the channel in the ohmic mode of operation of the transistor. That is the channel can be accurately considered as a simple ohmic resistance.

IV.2.3 Backgating effect

Backgating is studied by calculating the space charge induced by the partial depletion of the channel under an applied substrate voltage to reduce its effective thickness and hence the conductance. Since the channel is n-type for the GaAs-MESFET, then the conductance is given by *G*:

$$G = \frac{I_{ch}}{V_{ds}} = \frac{q \mu_n Z}{L} \int_{-a_c}^{0} n dy \qquad \text{(IV.1)}$$

I_{ch} is the current and V_{ds} is the applied voltage in the channel. q is the electronic charge, and μ_n is the electron mobility in the channel. L and Z are the length and the width of the channel, respectively. The integral boundaries are at the contact with the gate ($y=-a_c$) and the interface

with the substrate (*y=0*). *n* is the electron density in the channel. The normalised conductance is then G/G_0; G and G_0 being the conductance under an applied bias and under zero bias, respectively.

IV.2.4 Simulation results:

IV.2.4.1 The effect of deep acceptors and donors

First, we consider that only a deep acceptor is present in the substrate. The normalized calculated conductance is presented in Figure IV.2. The conductance decreases with increasing density of the deep acceptor. It is observed that the reduction of the conductance occurs at lower voltage than in the case of their absence. This is evident since acceptors give the substrate a p-type like semiconductor, with a higher density than in previous case (without traps). Hence an negative applied voltage to the substrate is a reverse bias. The depletion region at the channel-substrate interface widens causing a decrease in the channel width and hence in its conductance.

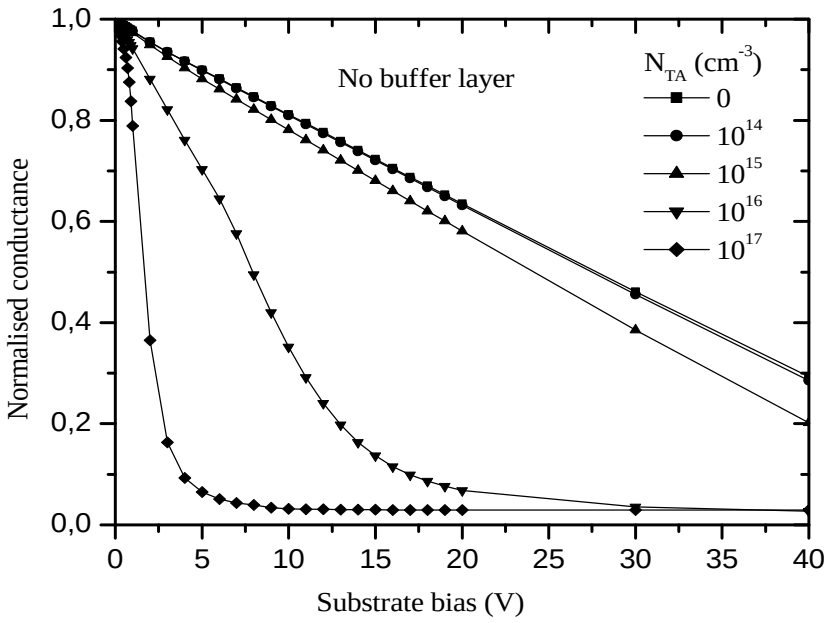


Figure IV.2: The normalized conductance as a function of the reverse voltage applied to the substrate of the MESFET without a buffer layer with the deep acceptor density increasing from 0 to 10^{17} cm^{-3}.

Adding deep donors to substrate makes the conductance reduction have a threshold. So increasing the deep donor density increases the threshold, as shown in Figure IV.3. At high deep donor density the conductance remains constant, but beyond a certain value of the

applied voltage it drops rapidly. A higher voltage is then required to reach the channel-substrate interface to cause a reduction in the channel conductance. This is the case of backgating with threshold voltage. So, the donors reduce backgating. When the donors are large than acceptors their effect becomes more apparent. Hence to reduce the effect of deep acceptors (responsible for backgating), they are compensated by deep donors. This increases the electron density and lowers that of holes in the substrate.

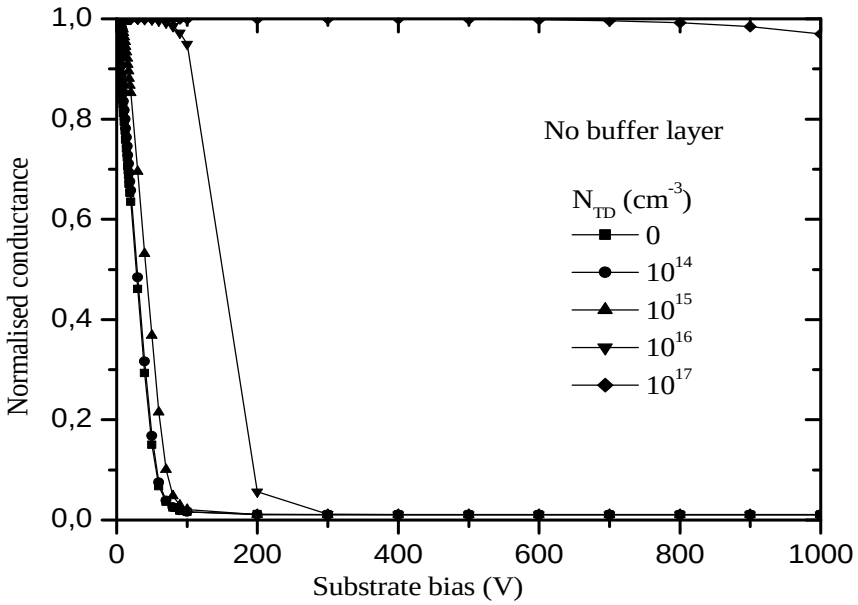


Figure IV.3: The normalized conductance as a function of the reverse voltage applied to the substrate of the MESFET without a buffer layer with the deep donor density increasing from 0 to 10^{17} cm^{-3}.

IV.2.4.2 The presence of a buffer layer

Adding a buffer layer can have an effect on backgating and this is shown in Figures IV.4 and IV.5 in the presence of deep acceptors and donors respectively. A buffer layer reduces the effect of deep centersin the substrate on the space charge region at the channel–substrate interface, which is responsible for backgating. Deep acceptors enhance backgating, and thus reducing their effect by adding a buffer layer will reduce backgating too (FigureIV.4 is compared with Figure IV.2). As to deep donors, they reduce backgating, and thus when their effect is reduced by adding a buffer layer, backgating is enhanced (by comparing Figure IV.5 with Figure IV. 3).

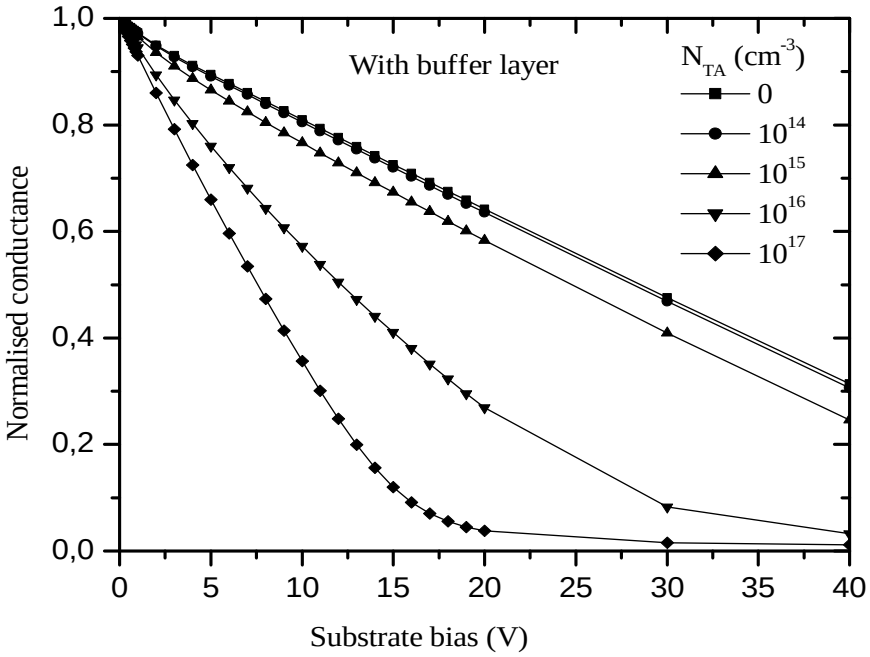


Figure IV.4: The normalized conductance as a function of the reverse voltage applied to the substrate of the MESFET with a buffer layer with the deep acceptor density increasing from 0 to 10^{17} cm^{-3}.

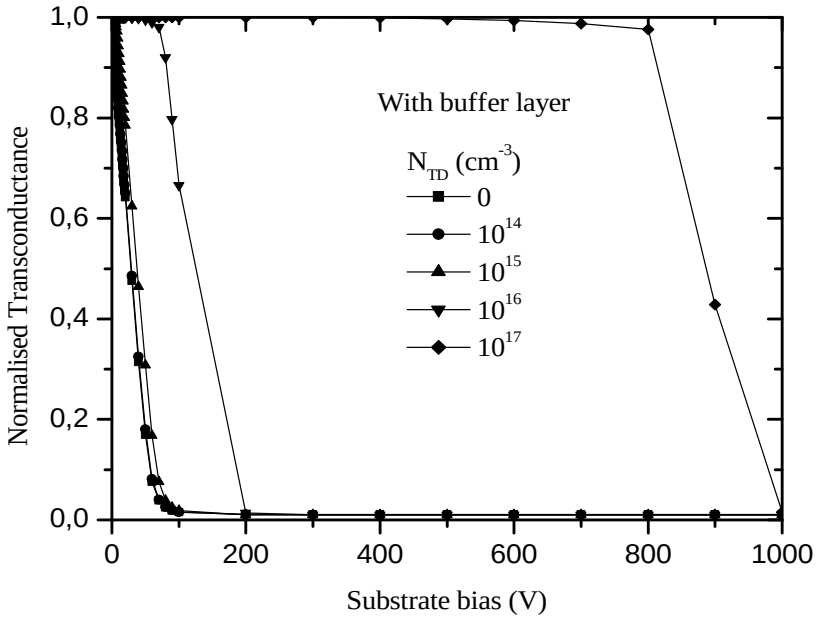


Figure IV.5: The normalized conductance as a function of the reverse voltage applied to the substrate of the MESFET with a buffer layer with the deep donor density increasing from 0 to 10^{17} cm^{-3}.

IV.2.5 Conclusion

The backgating effect in GaAs Field Effect Transistors was numerically modelled as a function of the density of deep acceptors and donors and the presence of a buffer layer. The presence of deep acceptors in the substrate increases the backgating. The donors reduce the backgating since they make the substrate less p-type hence the depletion region inside the channel decreases. The buffer layer also reduces backgating. As a suggestion to reduce backgating, one can add high density of deep donors to compensate deep acceptors [Sengouga and Abdeslam; 2008].

IV-3 Recessed gate GaAs MESFET

IV.3.1. Introduction

In this section, the hydrodynamic model will be validated. For this purpose, the NE71000, a low-noise Ku-K band recessed gate GaAs MESFET, for which experimental characterization was performed at SEECS, is simulated by MERCURY and ADS. Figure IV.6 presents a schematic view of the recessed gate GaAs MESFET used in this work.

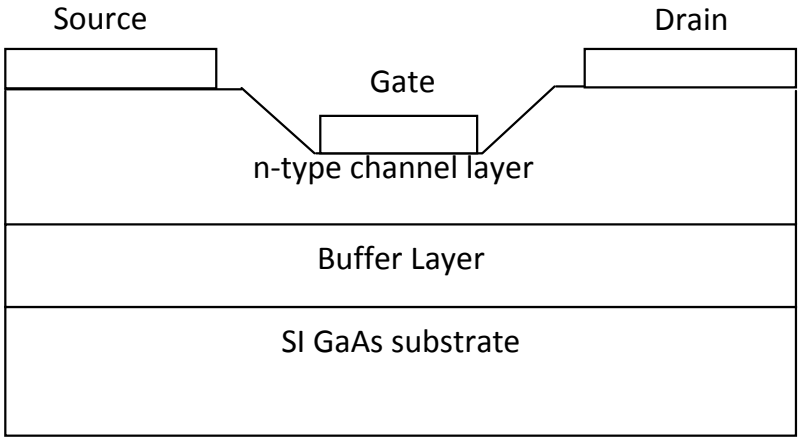


Figure IV.6: A schematic view of the recessed gate NE71000 GaAs MESFET used to validate the hydrodynamic model by MERCURY.

IV.3.2 The hydrodynamic model

The hydrodynamic model solves a set of four equations, (II.1), (II.13)-(II.15), using MERCURY. The physical parameters of the recessed gate GaAs MESFET are summarized in Table IV.1, some of them taken from [Asadi; 2011].However, some quantities such as the recess depth and the buffer layer thickness are not given in these references. They were

adjusted so that the simulation is as close as possible to measurements. For this particular transistor they are found to be approximately as given in the table IV.1.

Table IV.1: The parameters of the NE71000 recessed gate GaAs MESFET used in the HDM simulation by MERCURY. These parameters are supplied at SEECS.

Physical Parameters	Value (unit)
Channel thickness (a)	0.1 µm
p-buffer layer thickness	0.15 µm
Substrate thickness	0.15 µm
Total gate width w_{dev}	280 µm
Number of fingers p_s	4
Finger width	280/4=70 µm
Gate length l_g	0.3 µm
Recessed gate depth	0.028 µm
Donor doping density	$2.5\times10^{17}cm^{-3}$
Built in voltage V_{bi}	0.6516 V

The bulk parameters used for the recessed gate GaAs MESFET are reported in Table IV.2.
In order to validate HDM, the following procedures were carried out. First, the current voltage (I-V) characteristics were obtained through MERCURY, using the parameters in Tables IV-1 and IV-2. These characteristics include small as well as large signal modelling and have been successfully compared to measurement (Figure IV.7).

Table IV.2: Bulk parameters of GaAs used in the HDM simulation by MERCURY.

Bulk material Parameters	Value (unit)
Γ valley energy gap E_g (Γ)	1.42 eV
L valley energy gap E_g (L)	1.73 eV
X valley energy gap Eg (X)	1.91 eV
Electron affinity χ_{aff}	5.49 eV
Relative permittivity ε_r	12.85
Γ valley electron effective mass $m_c(\Gamma)$	0.063 m_e
L valley electron effective mass $m_c(L)$	0.221 m_e
X valley electron effective mass $m_c(X)$	0.410 m_e
Thermal resistivity ρ_{th}	2.27 K.cm/W
Electron mass at rest m_0=m_e	9.1095×10^{-31} Kg

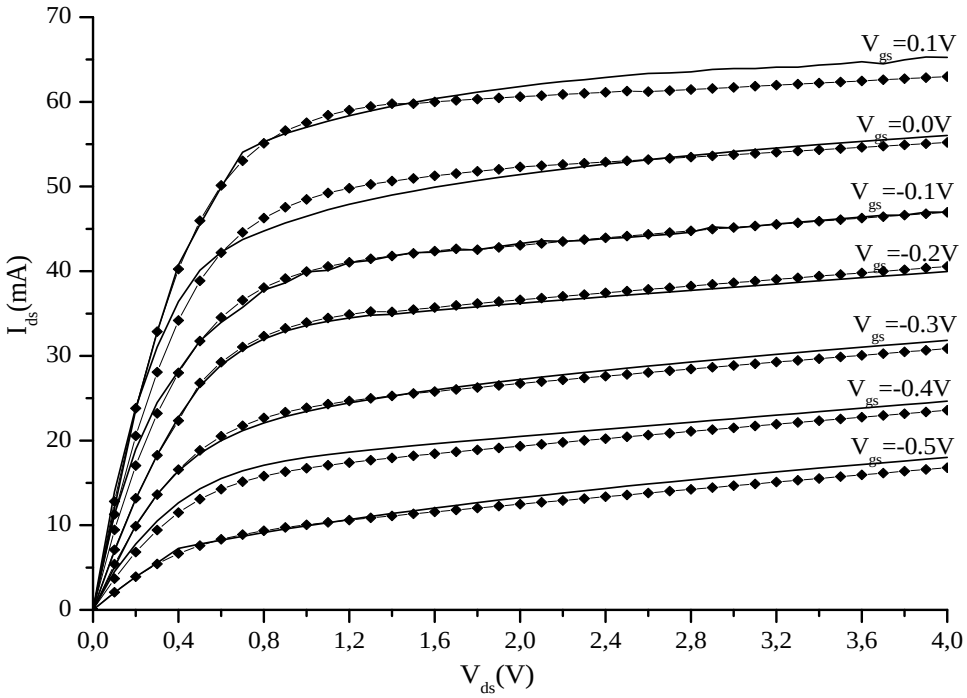


Figure IV.7: Comparison of I-V characteristics simulated by Mercury (solid line) and measured (symbol) for the recessed gate NE71000 transistor.

The small signal regime can also be represented by scattering-parameters (S-parameters).Thus, the S-parameters were also evaluated by MERCURY, and as for the I-V curves, they have been successfully compared to measurements, as shown in Figure IV.8, especially in the low part of the spectrum.

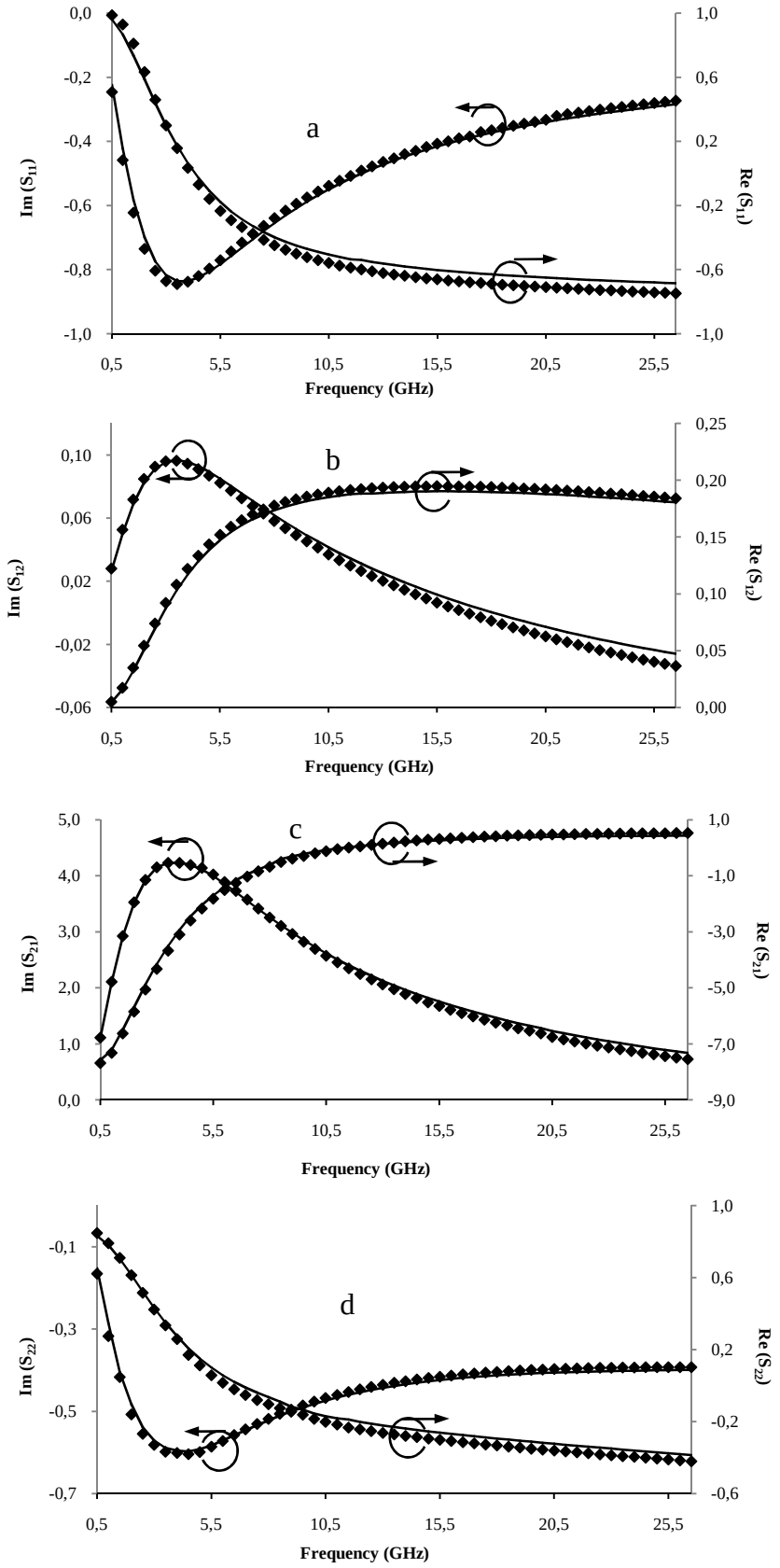


Figure IV. 8: Comparison of S-parameters simulated by Mercury (solid) and measured (symbol) for the recessed gate NE71000 transistor.

IV.3.3. Electrical modelling

After modelling the transistor using the hydrodynamic model implemented in Mercury, the next step was to simulate the I-V characteristics and S-parameters in the ADS software, a circuit based simulator. The equivalent circuit of the transistor used by ADS is shown in Figure IV.9. This equivalent circuit is based on the Cubic Curtice model [Curtice and Ettenberg; 1985]. First the wave propagation effect is not taken into account. This means that the parasitic elements in the equivalent circuit are constant, *i.e*, frequency independent.

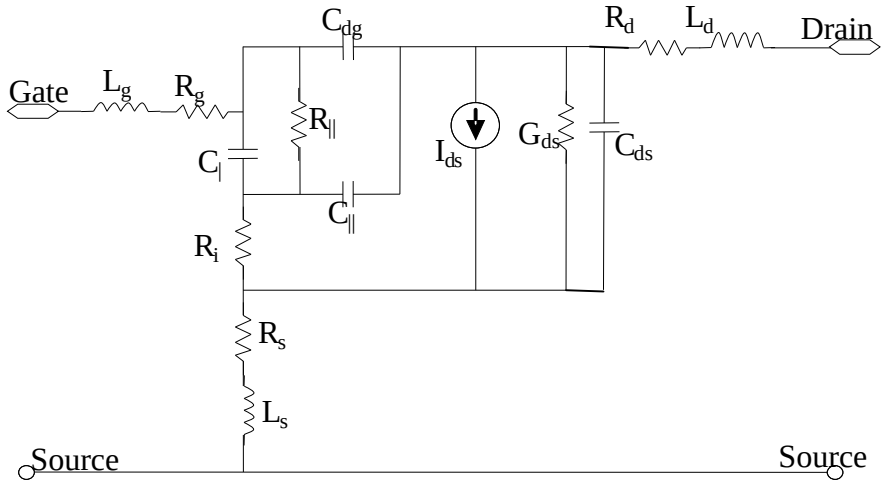


Figure IV.9: The NE710000 equivalent circuit based on the Curtice model used by ADS to simulate the linear and nonlinear I-V characteristics and the small signal S-parameters. The values of the equivalent circuit element are given in Table IV.3.

The values of the equivalent circuit elements are summarized in Table IV.3. The drain-source current of the current generator I_d is given by Equation III.52.

As seen in Figure IV.10, the simulated I-V characteristics simulated by ADS are in good agreement with measurements. Note that in the equivalent circuit the resistance $R_{||}$ has a very high value, usually greater than 1MΩ since it represents the resistance to the current flowing to the gate. This current is negligible since the gate is reverse-biased. Thus, to facilitate ADS modeling, this resistance was considered as infinite.

Table IV.3: The elements of the equivalent circuit and Curtice parameters used by ADS to simulate the I-V characteristics for NE71000.

Circuit elements	Numerical Values
L_d	0.005 nH
L_s	0.001 nH
L_g	0.005 nH
R_d	1.5 Ω
R_s	1.5 Ω
R_g	2.0 Ω
R_i	1.6 Ω
$R_{\|\|}$	1 MΩ
C_{dg}	0.033 pF
C_{ds}	0.03 pF
$C_{\|}$	0.28 pF
$C_{\|\|}$	0.064 pF
G_{ds}	1.5 mS
Curtice cubic parameter values used in Equation III.52	
A_0	0.058
A_1	0.1034
A_2	-0.00924
A_3	-0.048
¥	2.345
	0.0212

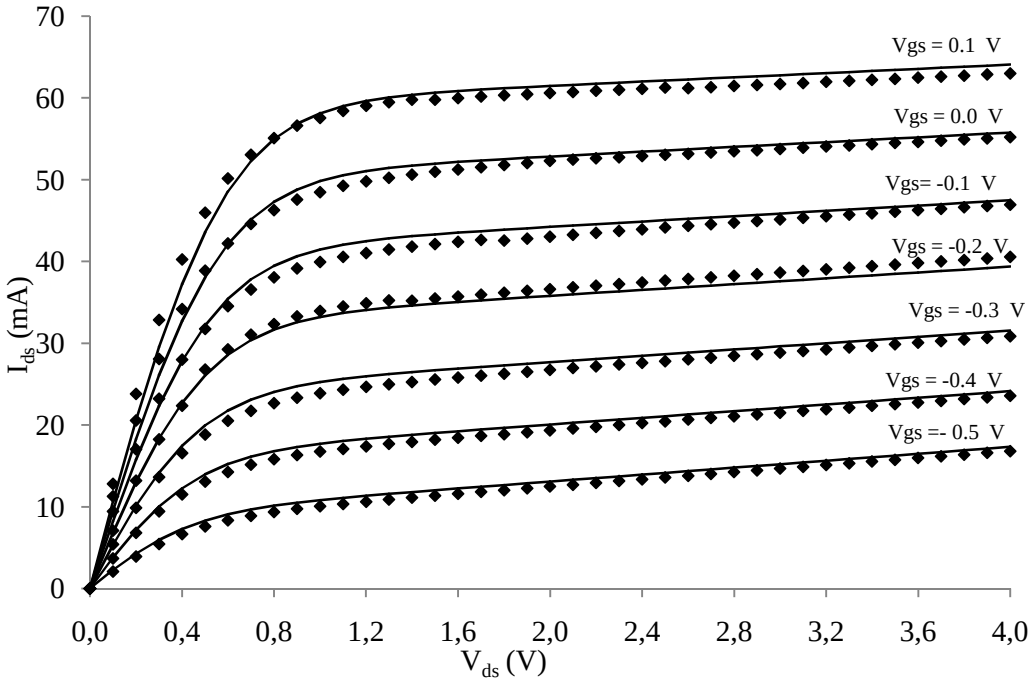


Figure IV.10 Comparison of I-V characteristics simulated by ADS (solid line) and measured (symbol) for the recessed gate NE71000 transistor.

Note that a MATLAB code was used to extract the equivalent circuit elements (Figure V.9) from measured S-parameters using the methodology presented in chapter III (Section III.3.2). This circuit was implemented in ADS to obtain the corresponding S-parameters called "S-parameters without wave effect". Figure IV-11 shows a good agreement with measurements, particularly in the lower part of the frequency spectrum.

However, as the frequency increases, the disagreement increases. This relative slight disagreement at high frequencies will be explained later in terms of propagating wave effect. The necessity to introduce a "corrected model" is therefore obvious.

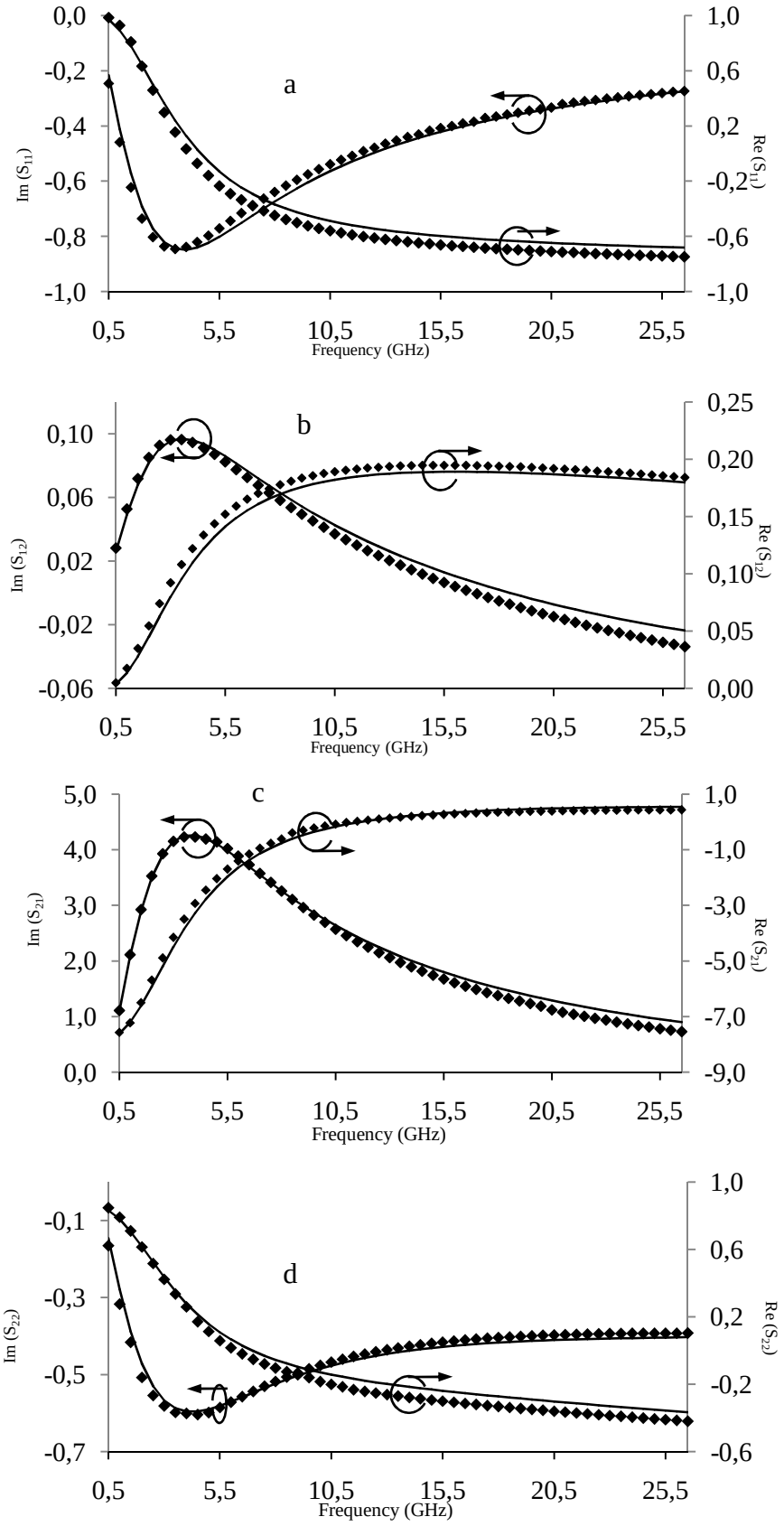


Figure IV.11: Comparison of S-parameters simulated by ADS (solid line) without the wave propagation effect and measured (symbol) for the recessed gate NE71000 transistor.

So, we took into account the wave propagation effect, which include the miniaturization effects associated to high frequency operation. Since this effect is a time-dependent effect, the time-domain FDTD approach was used to reevaluate these parasitic elements. In fact, the transistor terminals are now considered as transmission lines instead of short-circuits. Then, the parasitic elements should be seen as distributed elements, quantified per unit length (Table IV.4).

From the equations describing the FDTD procedure, we determine the input-output currents and voltages at both ends of the transmission lines. This allows deducing the time-dependent values of the parasitic elements.

Since the I-V characteristics are usually measured as DC values (low frequency), they are not investigated in this section. Therefore we only consider the S-parameters since they are highly frequency dependent. The S-parameters are usually measured versus the signal frequency. Therefore, the time-domain transmission line input/output currents and voltages as detailed in Chapter III are converted to frequency domain relationships (through a Fast Fourier Transform). The transistor Y-parameters are first calculated (for a bias of V_{ds}= 3 V and I_{ds}= 10 mA) following the procedure developed in Chapter III. They are then converted to S-parameters. The obtained S-parameters taking into account the wave propagation effect, compared to measurement and simulated S-parameters without wave propagation effect, are shown in Figure IV-12. The simulated S-parameters including the wave propagation effect are in a better agreement with measurements than without wave effect especially at high frequencies. The need for a better model which includes wave-propagation effect is therefore demonstrated.

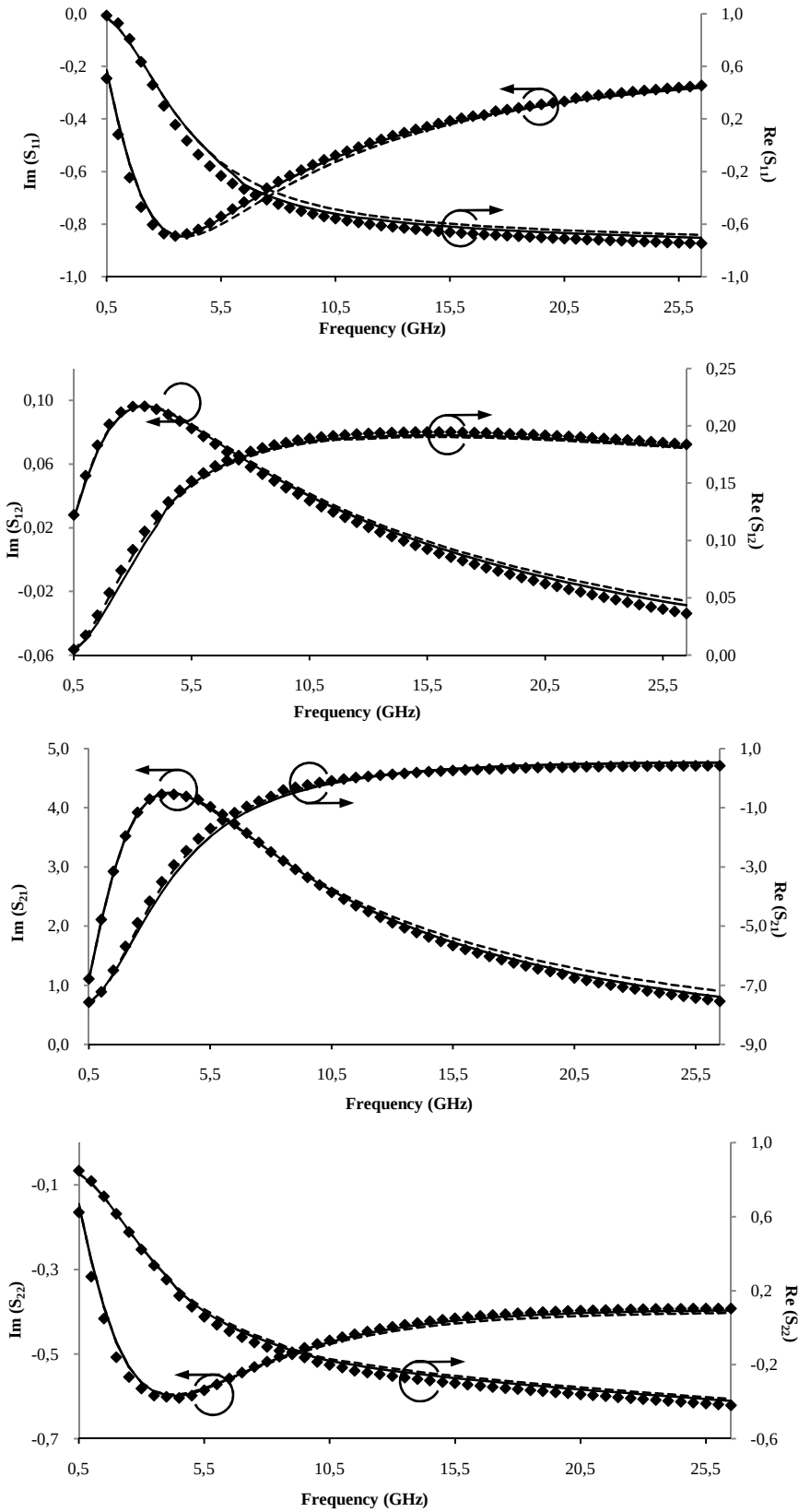
IV.3.4. Comparison between HDM and ADS

In order to evaluate the different models used in this study, simulated and measured S-parameters are reproduced in Figure IV.13 for the sake of comparison. It is evident that the ADS simulated S-parameters without taking into account the wave propagation effect are the furthest from measurements. Meanwhile, S-parameters simulated by ADS, taking into account the wave propagation effect, are in very good agreement with measurements. The Mercury (HDM) simulations give satisfactory results versus measurements. This is a very important result since it validates the physical modelling by Mercury using

.HDM. Therefore HDM modelling will be adapted for further simulations (next sections).

Table IV.4: Numerical values of extrinsic and intrinsic elements. (The transistor was biased at V_{ds}= 3 V and I_{ds}= 10 mA)

Electrical « distributed » model elements	Values(per unit length)
L_d	780 nH/m
L_s	780 nH/m
L_g	161 nH/m
M_{gd}	360 nH/m
M_{gs}	360 nH/m
M_{ds}	240 nH/m
R_d	900 Ω/m
R_s	900 Ω/m
R_g	34300 Ω/m
C_{gp}	0.6 pF/m
C_{dp}	87 pF/m
C_{sp}	148 pF/m
C_{ds}	0.0178 nF/m
C_{gs}	0.771 nF/m
C_{gd}	0.1178 nF/m
g_m	146.42 S/m
R_i	0.002 Ω/m
G_{ds}	15.46 mho/m



FigureIV.12: Comparison between ADS simulated S-parameters calculated (for a bias of V_{ds}= 3 V and I_{ds}= 10 mA) taking into account wave propagation effects (solid line), ADS simulated S-parameters without wave propagation effects (dashed line) and measurements (symbol).

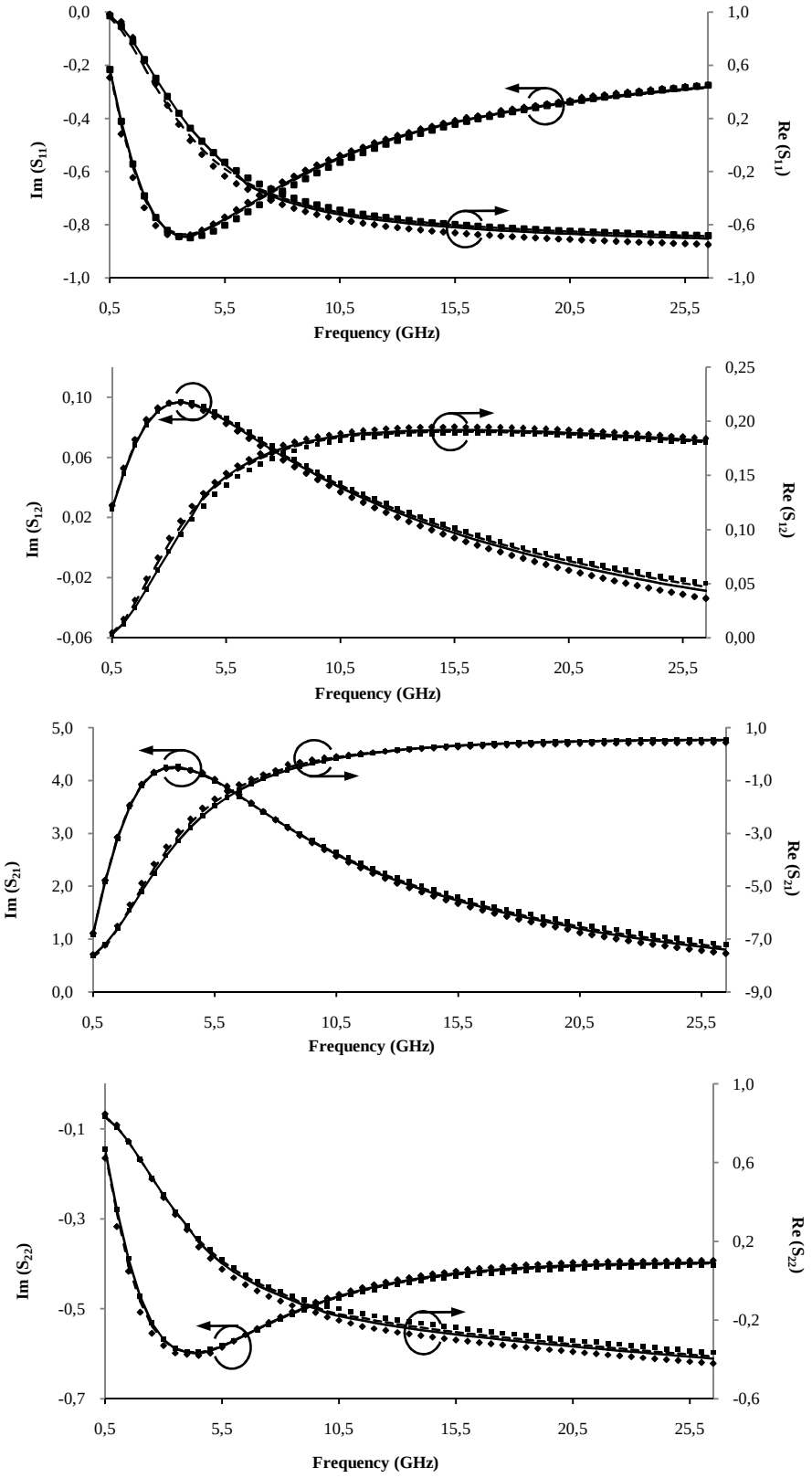


Figure IV.13: Comparison between ADS simulated S-parameterscalculated (for a bias of V_{ds}= 3 V and I_{ds}= 10 mA) taking into account wave propagation effects (solid line), ADS simulated S-parameters without wave propagation effects (dashed line) measurements (♦) and Mercury simulation data (■).

IV.3.5 Effect of the gate length

Once the HDM model has been validated, it was used to assess the effect of the gate geometry on the recessed gate MESFET performances. First, the gate length effect on the I-V characteristics, the transconductance, the conductance and the capacitance of the electrodes C_{gd} and C_{gs} are simulated by Mercury using HDM. Second, the effect of the recess depth effect on the same parameters was simulated.

IV.3.5.1 Effect of the gate length on the I-V characteristics

It is well known (equations III.3-5) that reducing the transistor gate length is a useful way to increase its transconductance, output conductance and gate-source capacitance. These parameters will in turn affect the transistor performance such as the cutoff frequency f_t which is an approximate criterion used to compare the operation speed limitation of the devices. f_t can be represented in term of the gate length ($f_t = \frac{v_{sat}}{l_g}$).

From Figure IV.14, it is clear that as the gate length is reduced, the channel current increases. This is mainly due to the inctrease in the lateral electric field which is inversly proportional to the gate length ($E = V/l_g$). This increase in the electric field will increases the channnel (drain-source) current (I_{ds}) since this latter is mainly a drift current, that is $I_{ds} = AJ_{ds} = A\sigma E$. Here σ is the channel conductivity, A is the channel area throuch which the current flows and J_{ds} is the channel (drain-source) current density.

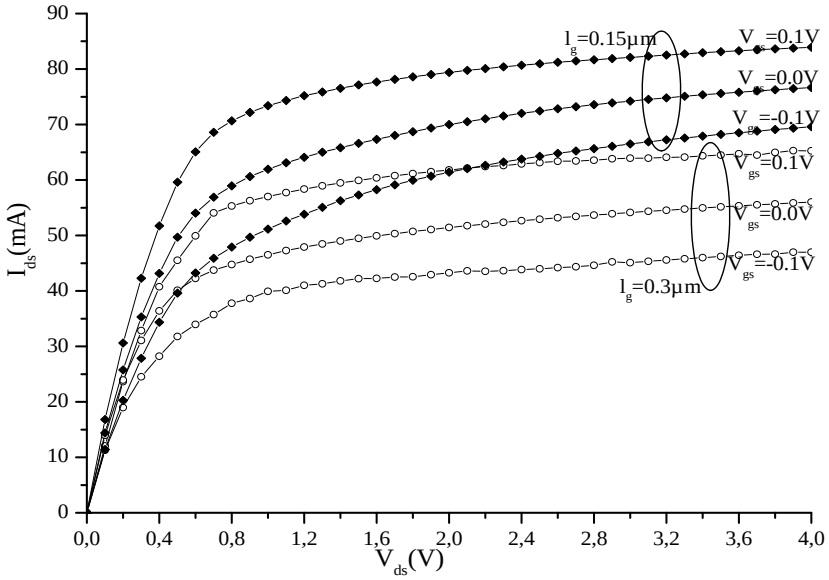


Figure IV.14: The gate length effect on the I-V characteristics of the recessed gate GaAsMESFET for different gate voltages.

IV.3.5.2 Effect of the gate length on the transconductance

The gate length effect on the transistor transconductance was simulated versus the gate-source voltage, for a fixed drain-source voltage. An example of the gate length effect on the transistor transconductance, at a drain-source voltage of $V_{ds} = 0.5\ \mathrm{V}$, is shown in Figure IV.15.

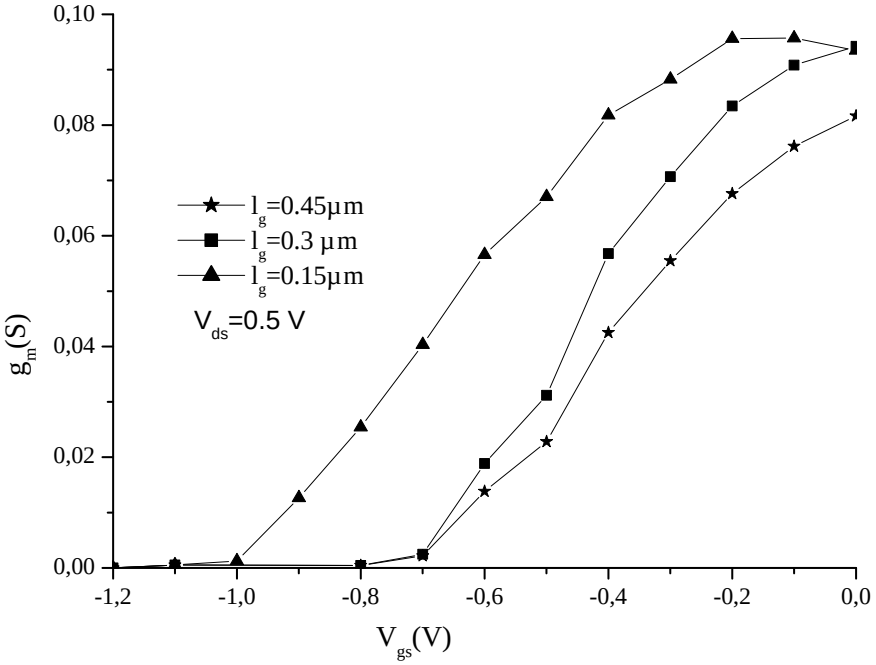


Figure IV.15: The transistor transconductance versus the gate-source voltage at different gate lengths under V_{ds}=0.5 V.

As expected, the transconductance increases inversely to the gate length (Figure IV.14) and the reverse bias on the gate.

IV.3.5.3 Effect of the gate length on the output conductance

The effect of the gate length on the tranistor conductance was also simulated. The gate-source voltage is fixed at $V_{gs} = -0.1\ \mathrm{V}$ and the conductance is plotted versus the drain-source voltage (Figure IV.16). Firstly the conductance increases with decreasing gate length. This is obvious since the conductance is inversly proportional to the gate length ($g_{ds} = \sigma A / l_g$).

Secondly, the conductance deacreses with increasing drain-source voltage. Although the conductance is roughly proportional to the drain-source current, it is inversly proprtional to the drain-source voltage ($g_{ds} = \partial I_{ds} / \partial V_{ds}$). The increasing rate (slope) with the latter increases slower than with the first hence the decrease in the conductance.

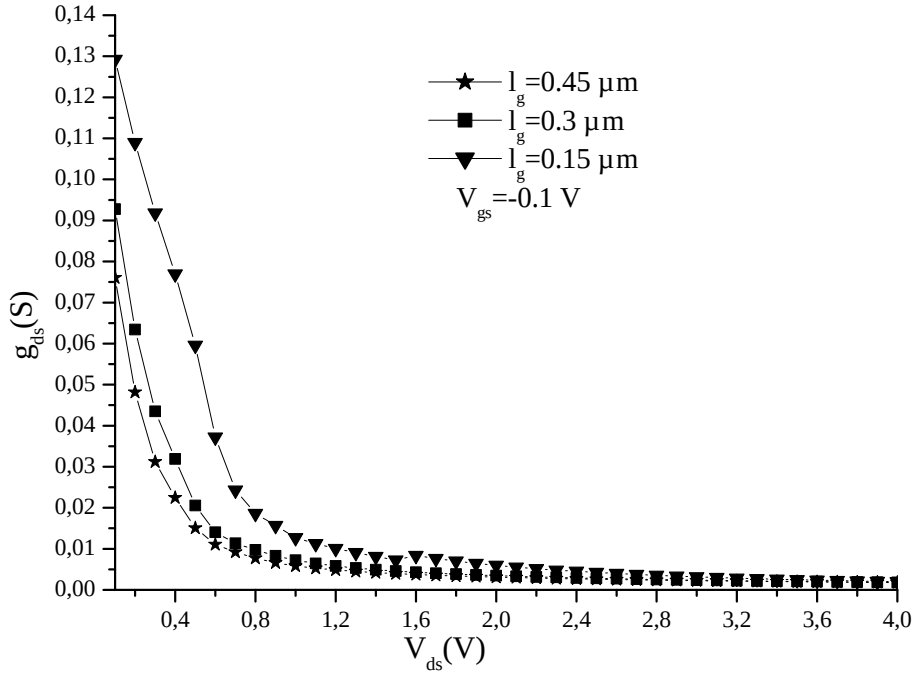


Figure IV.16: The transistor output conductance versus the drain-source voltage at different gate lengths under V_{gs}=-0.1 V.

IV.3.5.4 Effect of the gate length on the capacitances

The effect of the gate length on the gate-source capacitance $C_{gs}$was evaluated as well. In Figure IV.17, C_{gs} is plotted vs. V_{gs} for different gate lengths and at a drain-source voltage of $V_{ds} = 0.5$ V. On one hand, this capacitance decreases with increasing reverse gate-source bias. On the other hand, it increases with increasing gate length. It is well known that this capacitance represents the depletion region in the channel at the source end. Hence it is inversely proportional to this depletion region width and directly proportional to the gate area (and hence to its length) ($C_{gs} \propto l_g/h_{dep|s}$). Here $h_{dep|s}$ is the depletion region in the channel at the source end.

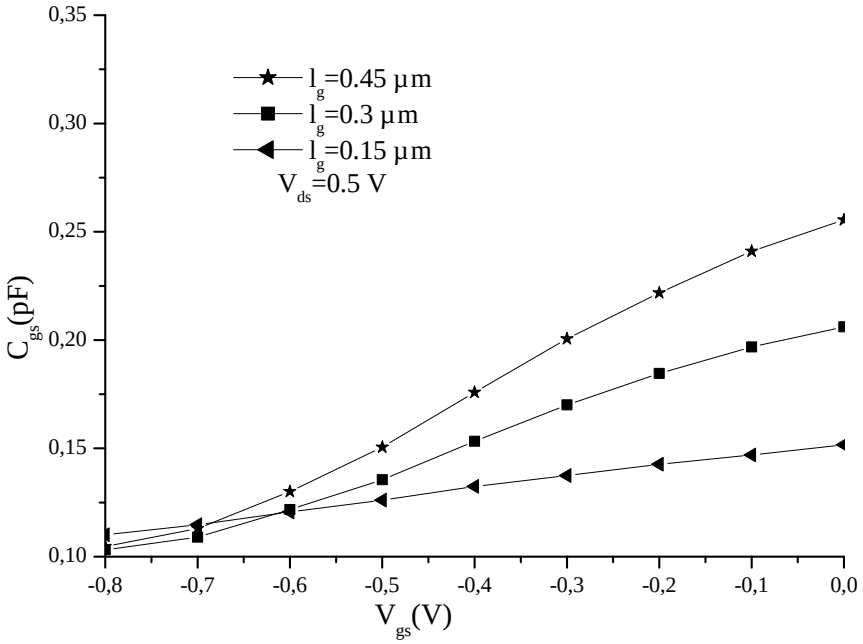


Figure IV.17: The gate-source capacitance versus the gate-source voltage under a drain-source voltage of V_{ds}=0.5 V at different gate lengths.

The next step was to simulate the effect of the gate length on the gate-drain capacitance (C_{gd}). Unlike the gate-source capacitance C_{gs}, this capacitance depends on both gate-source and drain-source voltages, hence its variation will be presented versus both voltages. C_{gd} versus V_{gs} at a drain-source voltage of $V_{ds} = 0.5\,\mathrm{V}$ for different gate lengths, is shown in Figure IV.18. Similarly,C_{gs} decreases with increasing reverse gate-source bias while it increases with increasing gate length. This capacitance represents the depletion region in the channel at the drain end. Hence it is inversely proportional to this depletion region width and directly proportional to the gate area (and hence to its length) ($C_{gd} \propto l_g/h_{dep|d}$). Here $h_{dep|d}$ is the depletion region in the channel at the drain end which increases with increasing reverse gate-source bias.

Figure IV.19 shows the variation of C_{gd} versus V_{ds} at a gate-source voltage of $V_{gs} = -0.1\,\mathrm{V}$ for different gate lengths. This capacitance decreases with increasing drain-source bias while it increases with increasing gate length. Using the same analysis as for its dependence on the gate-source voltage, the depletion region at the drain end increases with increasing drain-source voltage and hence the capacitance decreases.

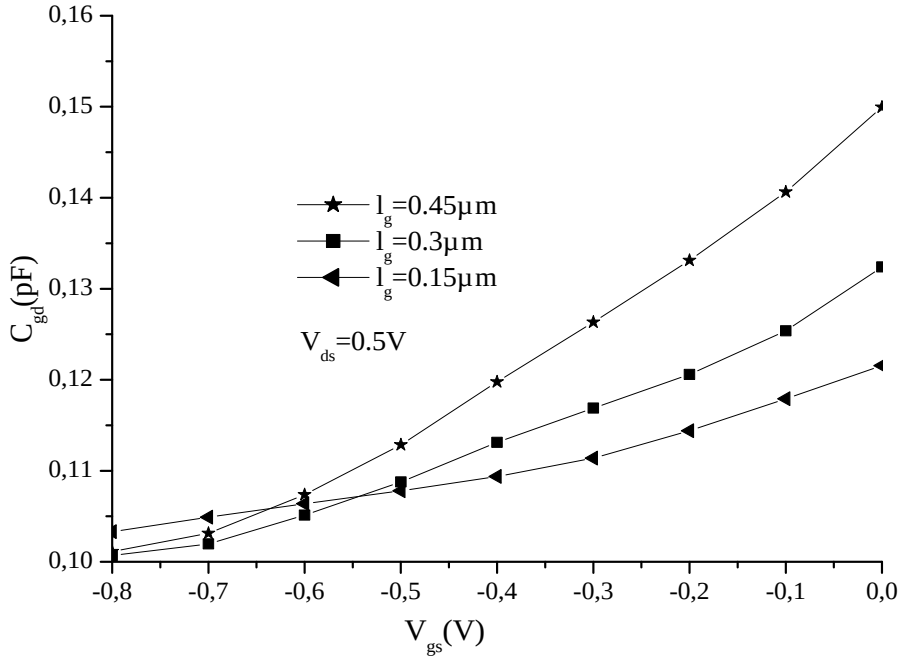


Figure IV.18: The gate-drain capacitance(C_{gd}) versus the gate-source voltage(V_{gs}) for different gate lengths under a drain-source voltage of V_{gs}= 0.5 V.

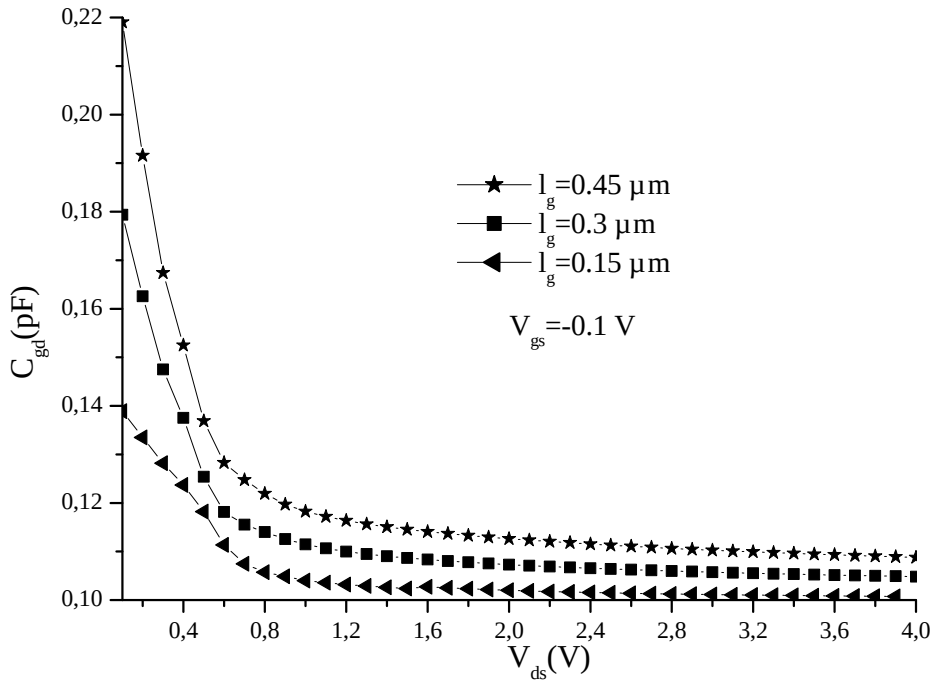


Figure IV.19: The gate-drain capacitance(C_{gd}) versus the drain-source voltage(V_{ds}) for different gate lengths under a gate-source voltage ofV_{gs}=-0.1V.

IV.3.6 Effect of recess gate depth

The recess gate consists on the reduction of the layer under the gate so that it will be under the drain and source contact planes as shown in Figure IV.6. The recess structure is useful in controlling the transistor pinch-off voltage, the reduction of the source and drain parasitic series resistances and improving the ohmic contacts in the source and drain regions.

Reducing the source and drain parasitic resistances improves the noise, the frequency performance and the transconductance of the transistor. The noise figure (a noise performance indicator) is related to these parasitic resistances by the Fukui formula given by [Fukui; 1979]:

$$N_f = 1 + K_f . C_{gs} \sqrt{(R_g + R_s)/g_m} \qquad \text{(IV.14)}$$

Where K_f is a constant, R_g is the gate resistance, R_s is the source resistance, g_m is the transconductance and C_{gs} is the gate-to-source capacitance.

Their frequency performance is characterized by the cutoff frequency and the maximum oscillation frequency. The latter is inversely proportional to the parasitic resistance through the relation given by [Sze and Ng; 2007]:

$$f_{max} = \sqrt{f_t / 8\pi R_g C_g} \qquad \text{(IV.15)}$$

here C_g is the sum of the gate-source and gate – drain capacitances, f_t is the cut-off frequency.

It is evident that the reduction of the series resistance increases the maximum oscillation frequency which in turn increases the cutoff frequency as shown in relation (I.22).

For good high frequency and noise performance, depth and shape of recess are both important. Increasing the value of gate recess-depth reduces the residual channel thickness which leads to increased output conductance [Mishra; 1986].

The recessed gate position, depth and geometric shape can also improve the electric field distribution and the device breakdown [Omori et al; 1989, Ohata et al; 1980].

IV.3.6.1 Effect of recess gate depth on the I-V characteristics

The recess gate depth effect on the I-V characteristics of the recessed gate GaAs MESFET is presented in Figure IV.20. Although the current is reduced by the recess structure, it will benefit other parameters as will be shown.

The saturation drain current is reduced with respect to the increasing of the recess gate depth. When the recess gate depth is varied from 0.028 µm to 0.032 µm, the narrow channel region under the gate is increased and therefore the drain current is decreased.

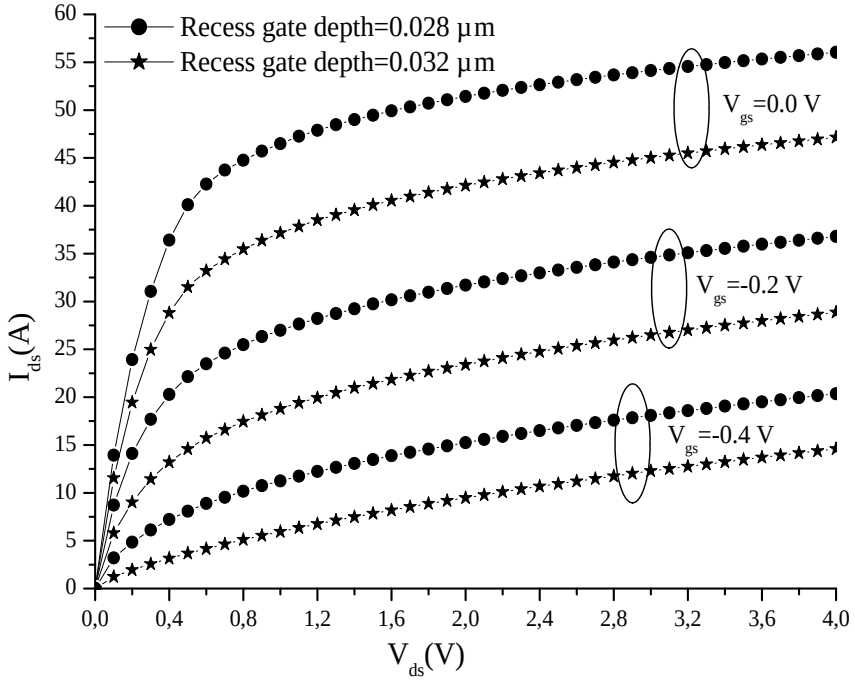


Figure IV.20: The gate recess depth influence on the I-V characteristics for a 0.3×280 µm×µm recessed gate GaAs MESFET.

IV.3.6.2 Effect of recess gate depth on the transconductance

The transconducatnce g_m versus the gate-source voltage V_{gs} for different gate recess depths is presented in Figure IV.21. The first observation is that g_m shows a peak (i.e., g_{max}) at a certain gate-source voltage, depending on the recess depth. Below the peak voltage (V_{peak}) g_m decreases with increasing recess gate depth while above this voltage, it increases with increasing recess gate depth. The transconductance improvement leads to an increase of the cutoff and maximum oscillation frequencies as given by equation (IV.15).

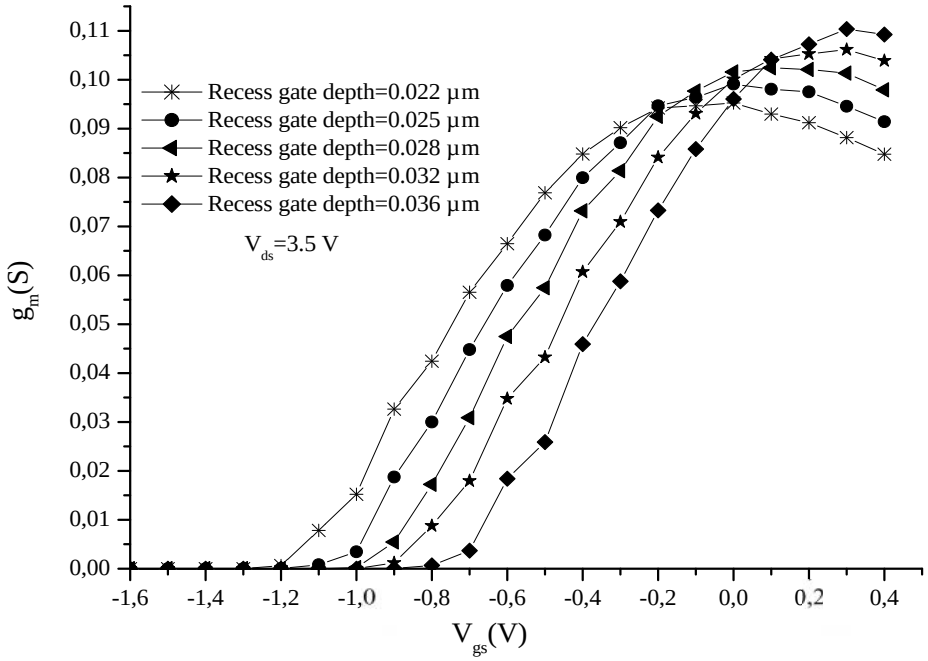


Figure IV.21: The transconductance g_n versus the gate-source voltage V_{gs} of a 0.3×280 µm^2 GaAs MESFETfor a different gate recess depth under drain-source voltage $V_{ds} = 3.5\,V$.

From Figure IV.21, one can get the maximum transconductance variation against the gate recess depth as shown in Figure IV.22. As seen, increasing the recess gate depth increases the maximum transconductance, and hence the cutoff frequency (f_t).

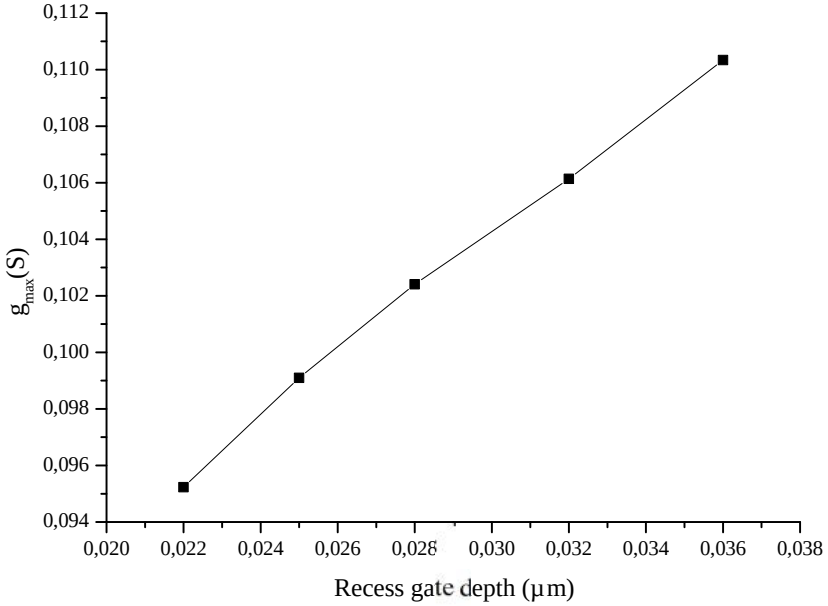


Figure IV.22: The maximum transconductance g_n versus the recess gate depths of a 0.3×280 µm^{2}GaAs MESFETunder drain-source voltage $V_{ds} = 3.5\,V$.

IV.3.6.3 Effect of recess gate depth on the output condcutance

Figure IV.23 shows the dc output conductance as function of the drain voltage for different recess gate depth at a gate-source voltage of -0.1 V. As seen, increasing the recess depth under the gate reduces the dc output conductance. This is because the channel width under the gate is reduced, which increases the vertical channel electric field and this in turn reduces the control of the carrier transfer in the channel with drain-source voltage. Consequently, this gives a reduction of the dc output conductance and increases the control of the gate-source voltage on the channel [Razavi et al; 2011]. As a result, increasing the recess gate depth improves the performance of the transistor since the maximum oscillation frequency, f_{max}, is roughly proportional to the drain-source resistance, R_{ds}, ($f_{max} = \frac{f_t}{2}\sqrt{\frac{R_{ds}}{R_{i+}R_g}}$) [Golio, 1991], i.e., the inverse of the output conductance g_{ds}.

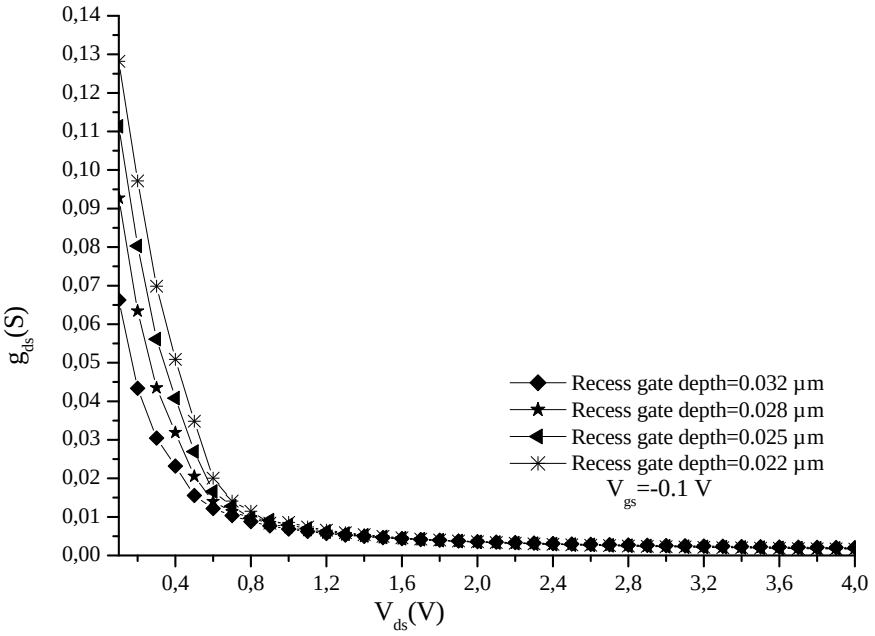


Figure IV.23: The 0.3×280 µm² GaAs MESFET output conductance as a function of the drain-source bias for different recess gate depths at a bias of $V_{gs} = -0.1\,V$.

IV.3.6.4 Effect of recess gate depth on the capacitances

Then, the gate-source capacitance dependence on the ac signal frequency was evaluated. For $V_{gs} = -0.1\,V$ and $V_{ds} = 3.5\,V$. Figure IV.24 shows that increasing the recess gate depth reduces C_{gs}. Therefore, reducing the channel thickness under the gate reduces the gate-source capacitance C_{gs}, which is important for high frequency operation as demonstrated by equation I.22.

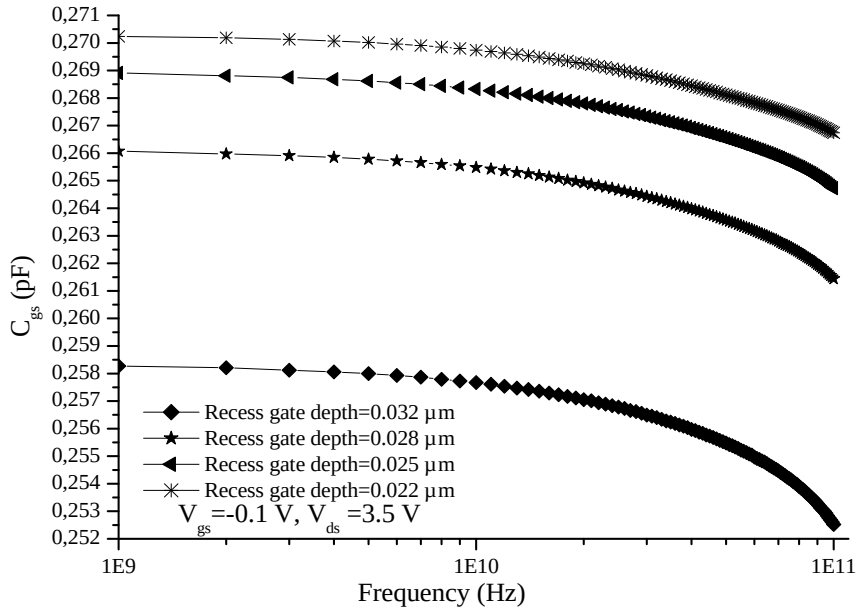


Figure IV.24: The 0.3×280 µm² GaAs MESFET gate-source capacitance versus the ac signal frequency for different gate recess depths at a bias of $V_{ds} = 3.5\,V$ and $V_{gs} = -0.1\,V$.

The dependence of the gate-drain capacitance C_{gd} as a function of frequency at $V_{gs} = -0.1\,V$ and $V_{ds} = 3.5\,V$ is shown in Figure IV.25.

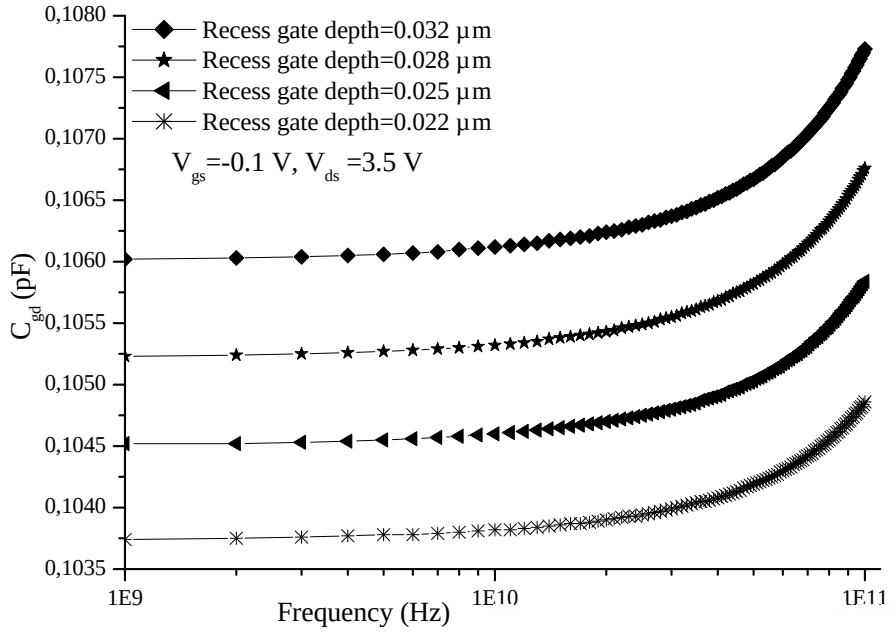


Figure IV.25: The 0.3×280 µm²GaAs MESFET gate-drain capacitance appearance for different gate recess depth at a bias of $V_{ds} = 3.5\,V$ and $V_{gs} = -0.1\,V$.

As this figure shows, increasing the recess depth of the gate increases C_{gd} which may degrade the device performance at high frequencies. Fortunately, the frequency performance of the transistor is not solely affected by C_{gd} but rather by the sum $C_g = C_{gd} + C_{gs}$. For the same recess depth and frequency, C_{gs} is higher than C_{gd}. Therefore, C_g is predominated by C_{gs} as depicted by Figure IV.26. Therefore, reducing the channel thickness under the gate reduces the gate capacitance which in turn improves the device performance at high frequencies.

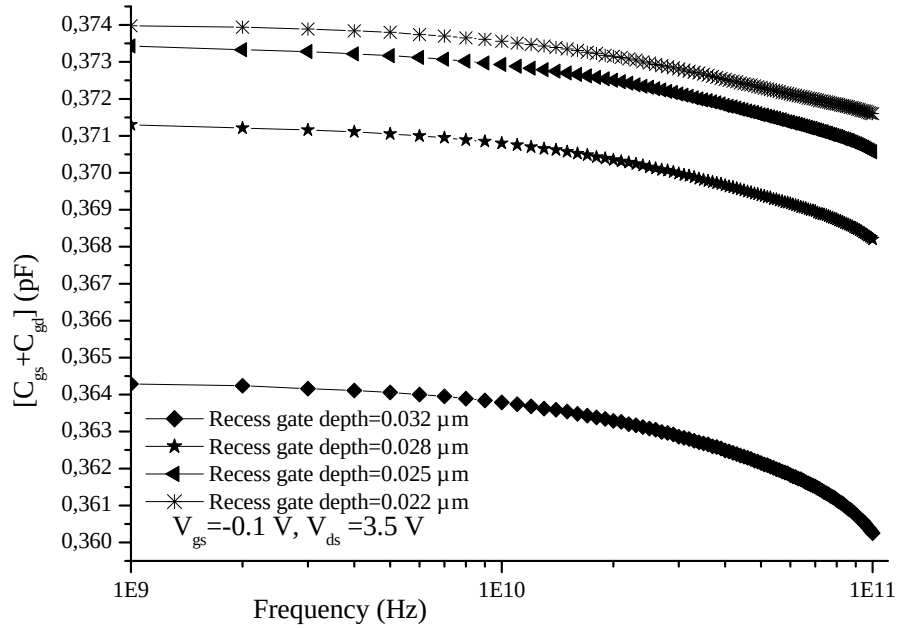


Figure IV.26: The 0.3×280 µm² GaAs MESFET gate capacitance appearance for different gate recess depthat a bias of $V_{ds} = 3.5\,V$ and $V_{gs} = -0.1\,V$.

So to summarize, from the point of view of device processing, in order to have higher MESFET transconductance and thus good performance, there are two key issues:

1. The gate length must be as small as possible
2. The gate recess depth must be carefully controlled.

IV.3.7 Nonlinear-regime capacitance

For large-signal modelling, the nonlinear behavior of GaAs MESFET does not only concern the drain current-voltage characteristics, I-V, but also the gate capacitance-voltage characteristics (C_{gs}-V and C_{gd}-V). Furthermore, the physical model discussed in section IV.3.2 should give an accurate representation of device operation under different bias conditions. The I-V characteristics were already studied (section IV.3.2).

Physically, the depletion layer beneath the gate creates a continuous space-charge region under the gate that expands from the source region to the drain region. The charge in this depletion region is balanced by an equal amount of charge on the gate electrode. The gate charge changes with gate-to-source and drain-to-source voltage. As a result, C_{gs} and C_{gd} depend on both V_{gs} and V_{ds} and not only on the voltage across them. The gate-drain capacitance C_{gd} is considerably smaller in magnitude than C_{gs} except in a certain transition region where both drain and source voltages are approximately equal. Charge is a constitutive quantity that cannot be directly measured. The nonlinear capacitances are usually extracted from S-parameter measurement in the whole transistor working domain. There are different ways in modelling MESFET charge (capacitance); the physical model proposed in chapter II is able to describe bias dependence of the capacitances.

It is not easy to model precisely the MESFET gate capacitances, where existing commercial models are valid in only certain device operation regions. For instance, modelling in the linear region and in the saturation knee region is difficult.

Charge (capacitance) performance, as expressed in chapter III, section III.5.4, is critical in predicting the nonlinear characteristics of MESFETs and therefore, the large-signal performance of MESFET circuits. As the physical model takes into account the gate charge model, it is accurate under various device biasing conditions. In particular, the performance prediction in the linear and saturation knee regions is reliable.

The nonlinear behaviour of the C-V characteristics is depicted in Figures IV.27 and IV.28. In these Figures, the physical model gives accurate results over various device operation regions, especially in the linear region where the variation of C_{gd} and C_{gs} is not well defined [Zhong; 2010]. In this region, C_{gd} decreases rapidly while increasing the drain-source voltage. In the saturation regime, the model is able to follow the small variation of C_{gd} vs. V_{gs} and C_{gs} vs.V_{ds}. Other models cannot predict the capacitance variations in the different regimes (linear, sub-threshold, or knee regions) [Zhong; 2010].

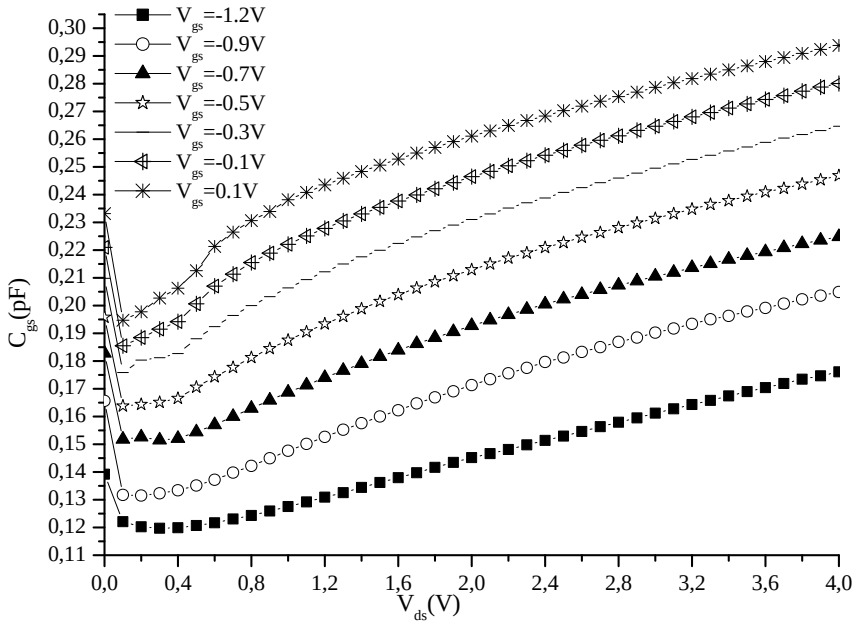


Figure IV.27: C_{gs} capacitance versus the drain-source voltage extracted from S-parameter for the 0.3×280 µm² recess GaAs MESFET under different gate-source voltages.

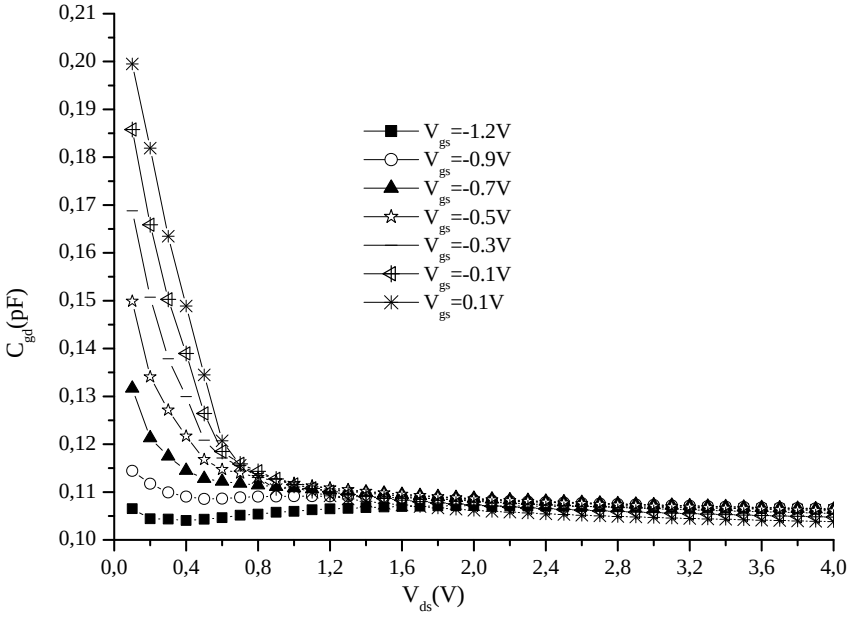


Figure IV.28: C_{gd} capacitance versus the drain-source voltage extracted from S-parameter for the 0.3×280 µm² recess GaAs MESFET under different gate-source voltages.

IV.4 The AlGaAs/InGaAs/GaAs pseudomorphic high electron mobility transistor (pHEMT)

Until the advent of the HEMT, the GaAs MESFET was the most widely used transistor for both microwave and high speed digital applications. However, since electrons must transit through the doped channel in a MESFET, it does not take full advantage of the high mobility in GaAs. The result is more than a 50 percent reduction in the electron mobility, since ionized dopants scatter electrons. Hence, separation of the dopant channel from the electron transit channel leads to an improved performance of the HEMT (see chapter I). Although GaAs MESFETs and HEMTs share similar physical equations and electrical equivalent circuits, HEMT and MESFET channel structures are different. Due to the two dimensional electron gas 2DEG layer resulting from the band-gap difference between $Al_xGa_{1-x}As$ and $In_xGa_{1-x}As$, pseudomorphic HEMT (pHEMT) (Appendix B) has superior mobility leading to lower parasitic drain and source resistances. Furthermore, with higher cutoff frequency f_t and maximum oscillation frequency f_{max}, these devices exhibit lower noise figure and higher gain [Hoke et al; 1990].

IV.4.1 The I-V characteristics for AlGaAs/InGaAs/GaAs pHEMT

In this section, we present the physical modeling of a 0.3×300 μm^2 AlGaAs/InGaAs/GaAs pHEMT and its accuracy will be demonstrated by successful comparison with measurements. The device structure and material properties used in this work are summarized in Tables IV.5 and IV.6.

Table IV.5: GaAs /$Al_{0.23}Ga_{0.77}As$/ $In_{0.22}Ga_{0.78}As$/GaAs pHEMT parameters

Device Parameters & values	pHEMT		
	GaAs	$Al_{0.23}Ga_{0.77}As$	$In_{0.22}Ga_{0.78}As$
Layer thickness	0.1 (µm)	0.035 (µm)	0.01 (µm)
Substrate thickness	2.30 (µm)		
$w_{dev}\times P_s$	60 (µm)×5		
l_g	0.3 (µm)		
Recessed gate depth	0.1 (µm)		
Donor doping density	3×10^{17} (cm^{-3}) Uniform distribution	3×10^{12} (cm^{-2}) Gaussian distribution	Undoped

Table IV.6: The semiconductors properties used in the pHEMT.

Material properties	pHEMT		
	GaAs	$Al_{0.23}Ga_{0.77}As$	$In_{0.22}Ga_{0.78}As$
E_g	1.42eV	1.70eV	1.37eV
	13.0	10.79	14.09
N_c	$4.5\times10^{16}cm^{-3}$	$5.89\times10^{17}cm^{-3}$	$3.11\times10^{17}cm^{-3}$

So, the I-V characteristics of the 0.3×300 μm^2 AlGaAs/InGaAs/GaAs pHEMT were successfully compared to those measured as shown in Figure IV.29.

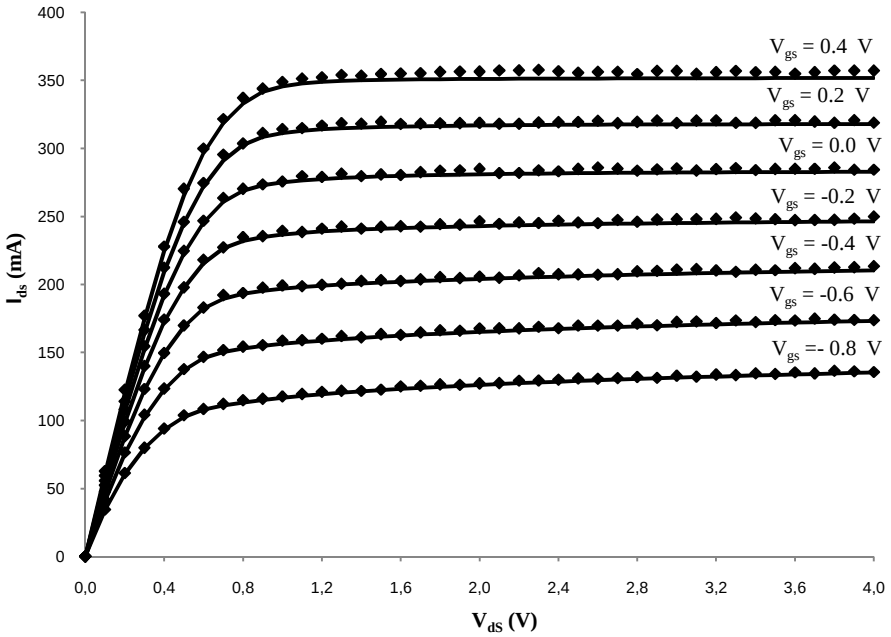


Figure IV.29:Comparison between simulated I-V characteristics (solid) and measurements (Symbol).for a 0.3×300 μm^2 AlGaAs/InGaAs/GaAs pHEMT.

IV.4.2 The transconductance-voltage dependence of the AlGaAs/InGaAs/GaAs pHEMT

Firstly, we evaluated the g_m-V_{gs} dependence as shown in Figure IV.30. In this Figure, the transconductance has a maximum g_{max} (peak) at a gate-source voltage of V_{gs}=-0.8 V. Indeed, an increase of g_{max} value from 155.67 mS to 227.59 mS was observed as the gate length l_g scaled down from 0.45 µm to 0.15 µm. The short gate-to-channel distance is the main reason for such high g_m due to the improvement of carrier transport properties [Chang et al; 2013].

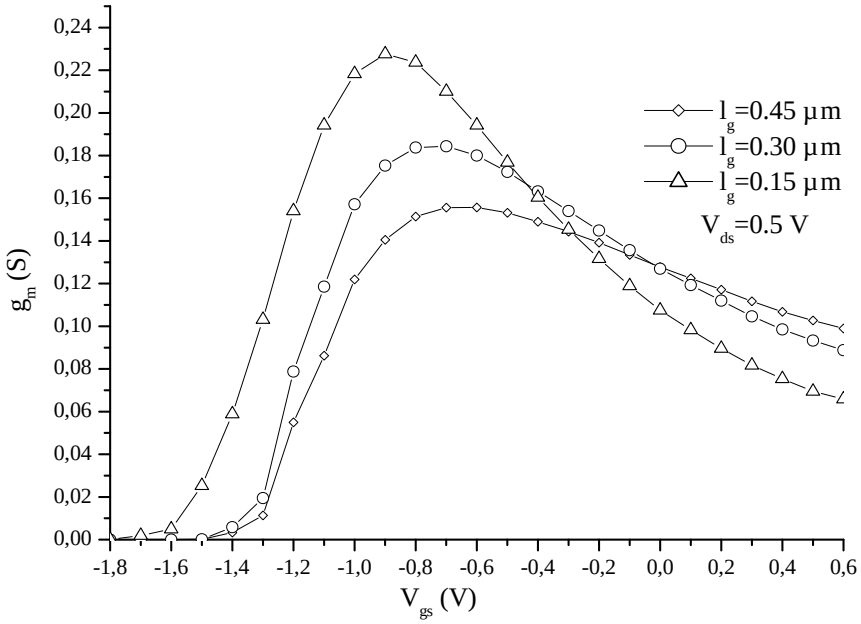


Figure IV.30: Transconductance versus gate-source voltage with different gate lengths of the 0.3×300 µm² AlGaAs/InGaAs/GaAs pHEMT under drain-source V_{ds}=0.5 V.

IV.4.3 The output conductance-voltage dependence of the AlGaAs/InGaAs/GaAs pHEMT

As shown in Figure IV.31, the output conductance is strongly affected by the gate length, as detailed in section IV.3.5.3.

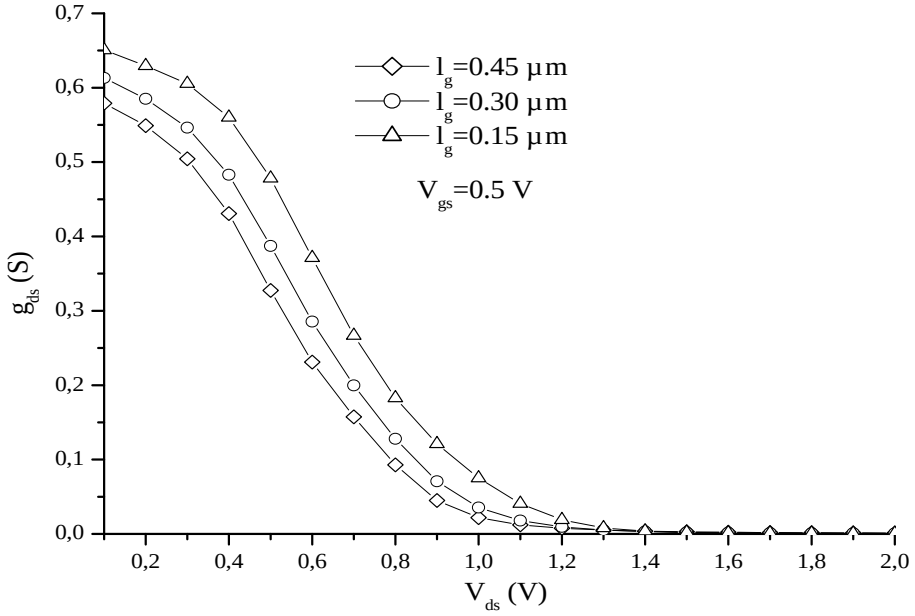


Figure IV.31: The output conductance versus drain-source voltage with different gate lengths of the 0.3×300 µm² AlGaAs/InGaAs/GaAs pHEMT under gate-source V_{gs}=0.5 V.

IV.4.4 The delta doping dependence of the AlGaAs/InGaAs/GaAs pHEMT

As discussed above, the gate length influences the pHEMT performance. Another way of improving the device performance is the control of its doped layer properties. The delta doped layer is one of the best routes to improve the transfer efficiency of electrons from the delta-doped AlGaAs layer to the InGaAs channel.

From the point view of materials, the transfer efficiency of electrons from the delta-doped AlGaAs layer to the InGaAs channel is very important for good control ability of electrons by the gate. If the electron transfer efficiency is low, there will be a lot of electrons residing in the delta-doped layer. These electrons will act as electron screen layer and thus, will weak the electrons control ability of the gate [Cao et al, 2001].

The effect of the delta doping density on the transconductance is shown in Figure IV.32.

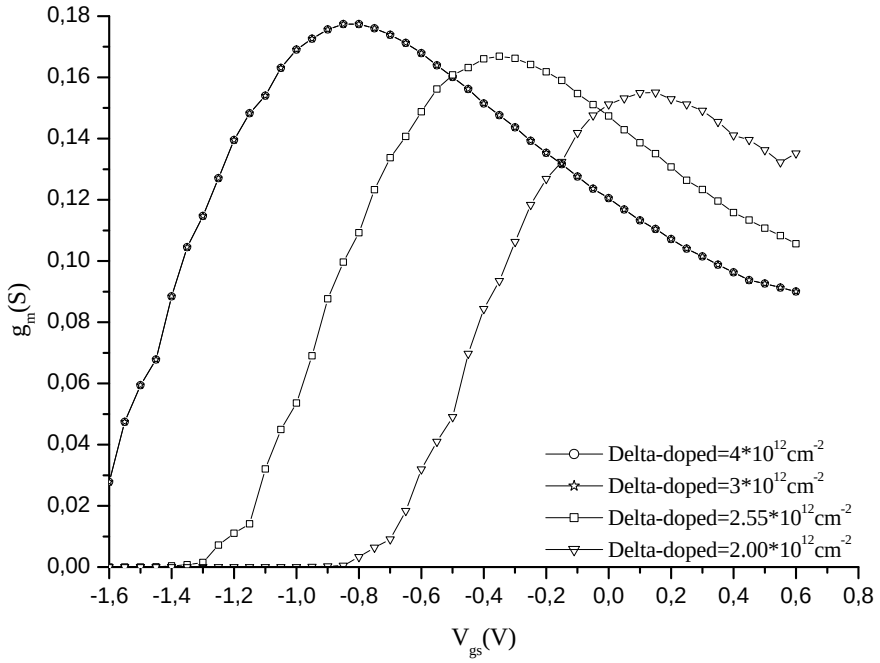


Figure IV.32: The delta-doping density effect on the 0.3×300 µm^2 AlGaAs/InGaAs/GaAs pHEMT transconductance versus the gate-source voltages and drain-source V_{ds}=0.5 V.

The peak transconductance increases with increasing delta doping density. This peak also shifts to more negative gate-source voltage. This is what is meant by for good control ability of electrons by the gate [Cao et al, 2001].

IV.4.5 Trapping effect on the HEMTs element parameters

Trapping phenomenon is a serious limitation in device performance [Singh and Snowden; 1999]. That is why the presence of traps in a GaAs-substrate was investigated in the 0.3×300 μm^2 AlGaAs/InGaAs/GaAs pHEMT.

Figure IV.33 shows the traps density and type effect on the AlGaAs/InGaAs/GaAs pHEMT transconductance. As it can be seen, the presence of acceptor traps in the GaAs substrate can increase the peak transconductance while donor traps reduce it. The acceptor traps increase the depletion region between the substrate and the channel leading to a reduction of the channel thickness. Hence, the improvement of the transconductance may be due to the better 2DEG electrons control by the gate [Singh and Snowden; 1999]. As displayed in Figure IV.34(a), the negative gate-source voltage gives a rise to the parallel conduction in the AlGaAs layer [Singh and Snowden; 1999]. Meanwhile, the presence of the substrate acceptor traps decrease this effect as depicted in Figure IV.34 (b). On the other hand, the donor traps significantly degrades the peak transconductance by reducing the space charge region between the channel and the substrate, leading to an increase of the parallel conductionin contrastto the case of the acceptor.

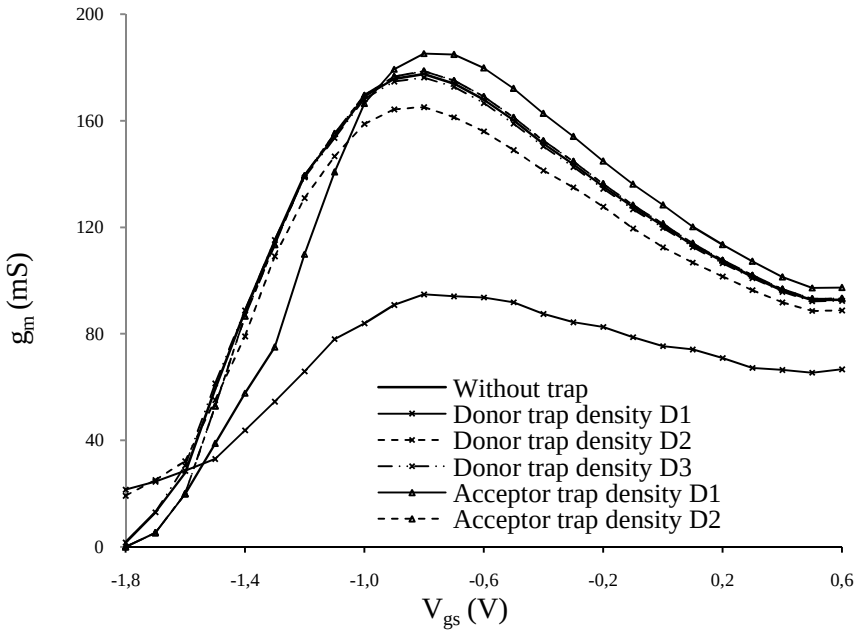


Figure IV.33: The effect of the presence of substrate traps and their type on the 0.3×300 μm^2 AlGaAs/InGaAs/GaAs pHEMT transconductance with respect to the gate-source bias V_{gs} and drain-source V_{ds} = 0.5 V. The trap densities are: $D_1 = 10^{16}/cm^3$, $D_2 = 10^{15}/cm^3$, $D_3 = 10^{14}/cm^3$.

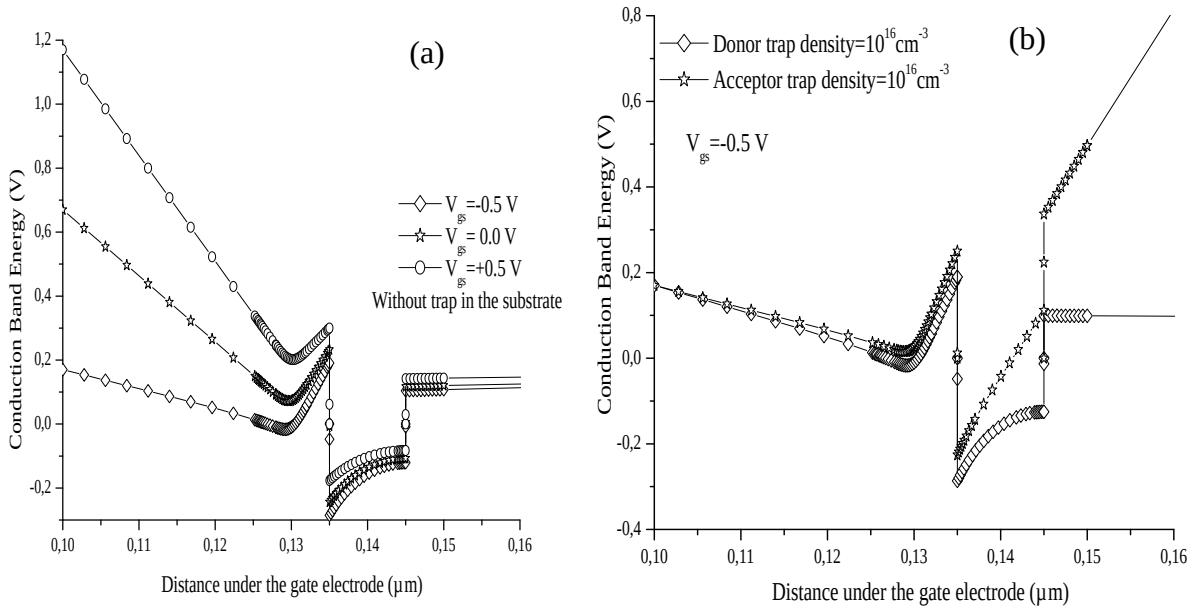


Figure IV.34: The type of deep level effect on the drain current of the 0.3×300 µm^2 AlGaAs/InGaAs/GaAs pHEMT versus gate-source V_{gs} with substrate trap density of $10^{16}cm^{-3}$ at drain-source V_{ds}=0.5V.

Figure IV.35 shows the effect of the different traps on the current versus the gate-source voltage characteristics. In contrast to the improvement of the transconductance by the acceptor traps, the current is reduced due to the widening of the space charge region at the channel-substrate interface.

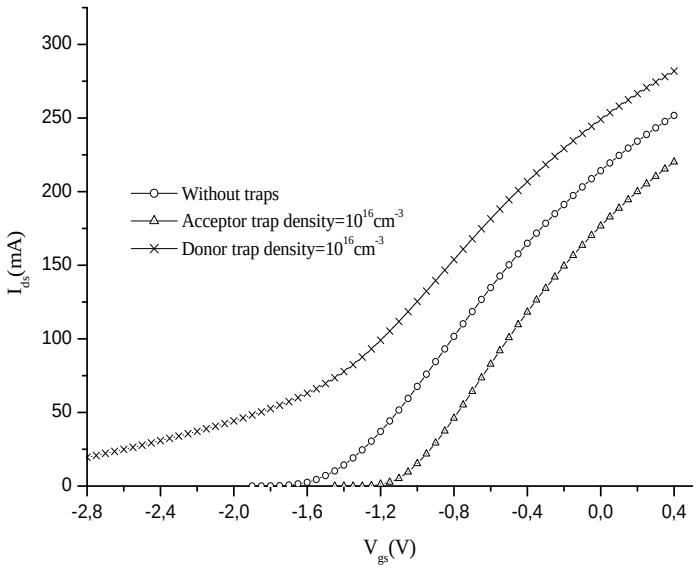


Figure IV.35: The type of deep level effect on the drain current of the 0.3×300 µm^2 AlGaAs/InGaAs/GaAs pHEMT versus gate-source V_{gs} with substrate trap density of $10^{16}cm^{-3}$ at drain-source V_{ds}=0.5V.

Note that such tendency can be also highlighted as function of the output voltage V_{ds}. An improvement of both the transconductance and output conductance by the acceptor trap is shown in Figure IV.36.

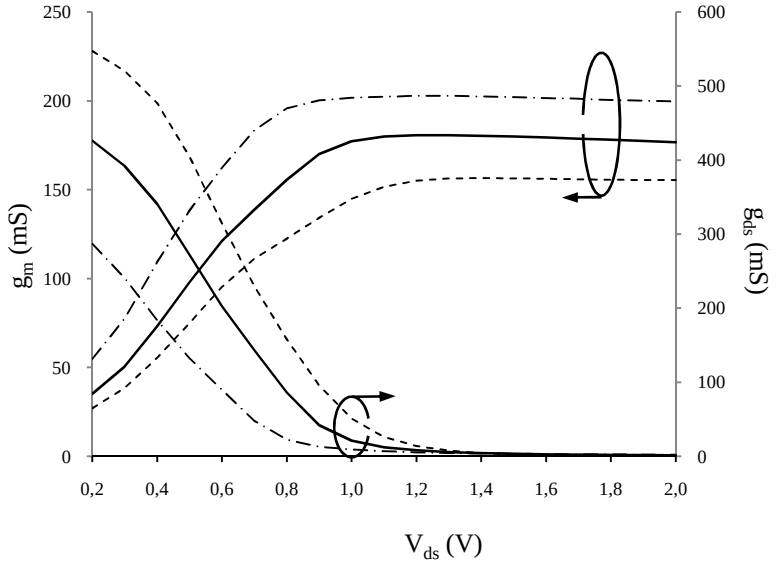


Figure IV.36: The Effect of the trap types in the 0.3×300 µm^2 AlGaAs/InGaAs/GaAsp HEMT substrate on the transconductance and the output conductance versus the drain-source V_{ds}. Without trap (solid line), donor (---) and acceptor (·–·) trap density: 10^{16}cm^{-3}.

IV.5 Summary:

In this chapter, we first investigated the effects of deep levels in the substrate of Gallium Arsenide based Field Effect Transistors (GaAs FETs) on the device characteristics. The transistor used in this case is planar, and an in-house software was used to simulate the effect of different types of deep levels in the substrate on the channel conductance. This software uses the drift diffusion model (DDM) to numerically solve the partial differential equations applied to the transistor. The Backgating phenomenon, which is the reduction of the conductance by the deep levels densities or their types, was numerically modelled as a function of the density of deep acceptors and donors and the presence of a buffer layer. The presence of deep acceptors in the substrate increases the backgating, while the donors reduce the backgating since they make the substrate less p-type; hence the depletion region inside the channel decreases. The buffer layer also reduces backgating. Therefore, the solution to reduce backgating would be to add high density of deep donors to compensate deep acceptors and the presence of buffer layer is also a mean to degrade this effect.

The hydrodynamic model (HDM) used in this work is a two dimensional physical model that solves a set of four coupled nonlinear partial differential equations. We also applied the internal physical model of a commercial software, namely SILVACO MERCURY, to in sub-micron MESFETs and HEMTs. Physical and electrical modellingapproaches were combined by MERCURY to obtain the DC current-voltage (I-V) characteristics and the AC (high frequency) scattering parameters (S-parameters) of sub-micronic MESFET and HEMTs. The proposed hydrodynamic model was validated for a recessed gate MESFET by comparing its I-V characteristics and S-parameters to measurements and also to the simulated results obtained by a commercial circuit simulator namely, Advanced Design System software (ADS).

Firstly, the NE71000 MESFET was selected as an example of low-noise Ku-K band recessed gate GaAs MESFETs. Its I-V characteristics and S-parameters simulated in MERCURY were in good agreement with those measured.

At a second step, we simulated the I-V characteristics and S-parameters in ADS and successfully compared the obtained results to measurements. However, some slight differences were noted in the higher part of the frequency spectrum. Hence, in order to take into account the wave propagation effects due to high operating frequencies and the miniaturization of our MESFET, the transistor terminals were considered as transmission lines, and the parasitic elements of the circuit (NE71000 MESFET) were modeled as distributed elements. The S-parameters were then re-simulated by ADS and compared to both measurements and S-parameters simulated by MERCURY. The Mercury HDM model gives also a sufficient agreement versus measurements, thus validating the physical modelling by MERCURY using HDM.

The effects of the gate lengths and recess depth on the device performance were also investigated. With increasing the gate length of the recess gate GaAs MESFET and of the AlGaAs/InGaAs/GaAs pHEMT, the saturated drain current and the output conductance are reduced. Increasing the gate length reduced the channel current, mainly due to the increase of the lateral electric field. Since the channel current is proportional to the electric field, thus inversely proportional to the gate length, the channel current increases when the gate length was scaled down from 0.3 µm to 0.15 µm. The reduction of the output conductance was also observed, since the output conductance is inversely proportional to the gate length. Regarding the reduction of recess depth on the drain current and the output conductance, the same remarks were obtained. Increasing the recess depth under the gate decreases the channel thickness and therefore the drain current. Meanwhile, the vertical electric field increases,

leading to the reduction of the carrier transfer in the channel. Consequently, the drain current and the output conductance were reduced versus the increasing of the recess gate depth.

The maximum value of the transconductance g_{max} of the recess gate GaAs MESFET and the AlGaAs/InGaAs/GaAs pHEMT was observed to increase with decreasing the gate length or by increasing the recess depth, thus improving the device performance. An improvement of the transconductance leads to an increase of the cutoff and the maximum oscillation frequencies, therefore a lower noise figure and higher gain.

Capacitances were also affected by varying the recess depth or the length of the gate. As the gate–source capacitance C_{gs} represents the depletion region under the gate at source end, decreasing the gate length will decrease this depletion region and thus, the value of C_{gs} will decrease, which in turn improves the cutoff frequency.

The drain-source capacitance C_{gd} was observed to decrease with decreasing the gate length, which improves the device performance. However, it increases with increasing the recess depth. This can be overcome, since C_{gd} is much smaller compared to C_{gs}, hence, $C_g(C_{gs}+C_{gd})$ is reduced.

The physical model also gives accurate results over various device operation regions, especially in the linear and saturation regions, thus, the ability of the model to follow the small variation of the C_{gd} with V_{gs} and C_{gs} with V_{ds}.

Consequently, from the point of view of device processing, and in order to have higher MESFET or pHEMT transconductance and thus, good device performance, the gate length must be as small as possible and the gate recess depth must be carefully controlled.

Delta doped effect on the AlGaAs/InGaAs/GaAs pHEMT performance was also studied. It was observed that by increasing the delta doping density, the maximum value of transconductance g_{max} increased. Thus, another way of improving the device performances is the control of doped layer properties. The delta doped layer is indeed one of the best routes to improve the transfer efficiency of electrons from the delta-doped AlGaAs layer to the InGaAs channel.

Therefore, from the point view of materials, the transfer efficiency of electrons from the delta-doped AlGaAs layer to the InGaAs channel is very important for good control ability of electrons by the gate.

The physical model (HDM) was also used to study the effect of the deep levels (traps) substrate on the performance of the pHEMT. Although, the deep levels are located in the substrate, their densities and types were found to affect the transconductance and the output

conductance. The acceptors improve the maximum transconductance by reducing the parallel conductance while the donors act inversely. This can directly affect the device performance, since the cutoff frequency and the maximum oscillation frequency are directly proportional to the transconductance.

Conclusion and Future Work

Simulation of the effects of deep levels in the substrate of Gallium Arsenide based Field Effect Transistors (GaAs FETs) on their characteristics was carried out through an in-house software. The drift diffusion model (DDM) was employed to numerically solve the partial differential equations applied to the transistor. The Backgating phenomenon was numerically modelled as a function of type and density of deep substrate traps and the presence of a buffer layer. Thus, the presence of deep acceptors in the substrate increases the backgating, while the donors reduce it since they make the substrate less p-type; hence the depletion region inside the channel decreases. The buffer layer also reduces backgating. Consequently, adding high density of deep donors to compensate deep acceptors is a solution to reduce Backgating phenomenon.

A new physical/electrical approach for analyzing microwave field effect transistors has been proposed. To demonstrate the proposed technique, a low-noise Ku-K band GaAs MESFET was modeled and the obtained simulated values successfully compared with measured data. Based on physical/electrical parameters, the full wave physical modelling of active devices can efficiently characterize their high-frequency behavior. To further improve the proposed approach, wave-propagation effects have been included to take into account the miniaturization effects associated to high frequency operation. The derived equation was solved using the FDTD technique, thus showing that by increasing the frequency up to the mm-wave range, the proposed model is more accurate than the physical model. This is due to wave propagation and phase cancellation effects.

Moreover, to demonstrate the capabilities of our approach, the presence of traps in a GaAs substrate was investigated in AlGaAs/InGaAs/GaAs pHEMT devices though their I-V characteristics and S-parameters. To get a higher transconductance and thus, better performance, two key design points for AlGaAs/InGaAs/GaAs pHEMTs or GaAs MESFETs are required. From the point view of material, the transfer efficiency of the electrons from δ-doped AlGaAs to the InGaAs channel must be high, and from the point view of device processing, the gate recess depth and length must be carefully controlled.

The full hydrodynamic model, coupled to the time-domain Maxwell's equations, allowed us to accurately account for the interactions between the carriers and the propagating wave inside the semiconductor devices. The electrodynamics wave propagation was added to the

semiconductor transport phenomenon, to better surround the transistor behavior from the physics perspectives.

The outcome of this work lies in the contribution of the implementation of a full-wave physical-based model of a semiconductor device valid up to the millimeter-wave range.

This objective was achieved and demonstrated through the publication of two papers namely,

> "Dependence of backgating on the type of deep centers in the substrate of GaAs FETs" Solid State Electronics, vol. 52, pp. 1039–1042, 2008.
> "Small-signal time-domain physical/electrical FET modeling approach," IEEE 25th Canadian Conf. on Electrical and Computer Engineering (CCECE 2012), Montreal, QC, Canada, April 29-May 2, 2012, pp. 1-4.

Based on the above contributions, several future directions can be highlighted:

1. The hydrodynamic model could be extended to estimate the S-parameters of the device. This will enable a designer to obtain the device physical parameters directly from electrical measurements.
2. The tool we developed could be employed in device simulation software which involves submicron GaAs FETs to predict their DC and AC characteristics. Thus, it can be used to study more complicated devices such as double delta doped HEMTs as well as dual-gate transistors.
3. The small- and large-signal modelling approaches can be also applied to other structures. Developing temperature dependent large-signal models for dual-gate MESFETs can be also quite attractive in power applications.
4. The large-signal model can be applied to other technologies especially to the promising GaN transistors which usually do not have specific large signal models available on the market.

Appendix A:
Helpful definitions

A.I. Introduction

As semiconductor feature sizes shrink into the nanometer scale regime, even conventional device behavior becomes increasingly complicated as new physical phenomena at short dimensions occur, and limitations in material properties are reached [Ferry and Goodnick; 1997]**.** In addition to the problems related to the understanding of actual operation of ultra-small devices, the reduced feature sizes require more complicated and time-consuming manufacturing processes. This fact signifies that a pure trial-and-error approach to device optimization will become impossible because it is too expensive and consuming time. As far as computers are considerably cheaper resources, simulation is becoming an indispensable tool for the device engineer. Besides offering the possibility to test hypothetical devices which have not (or could not) yet been manufactured, simulation offers unique insight into device behavior by allowing the observation of phenomena which cannot be measured on real devices.

The physical simulation of semiconductor devices refers in term to the charge transport and the corresponding electrical behavior. There are two main kernels, which must be solved self-consistently with one another, the transport equations governing charge flow, and the field driving charge flow. Both are coupled strongly to one another, and hence must be solved simultaneously. The field arises from external sources, as well as the charge and current densities which act as sources for the time varying electric and magnetic field obtained from the solution of Maxwell's equations. Under appropriate conditions, only the quasi-static electric field arising from the solution of Poisson's equation is necessary. The fields, in turn, are driving forces for charge transport. Figure A.1 illustrates the various levels of approximation within a hierarchical structure ranging from compact modeling at the top to an exact quantum mechanical description at the bottom.

At the beginnings of semiconductor technology, the electrical device characteristics could be estimated using simple analytical models relying on the drift-diffusion (DDM) formalism. Various approximations had to be made to obtain closed-form solutions, but the resulting models captured the basic features of the devices [Shur; 1969].

These approximations include simplified doping profiles and device geometries. With the ongoing refinement and improvements in technology, these approximations lost their basis

and more accurate description was required. This goal could be achieved by solving the DD equations numerically. Numerical simulation of carrier transport in semiconductor devices dates back to the famous work of Scharfetter and Gummel [Scharfetter and Gummel; 1969**]** who proposed a robust discretization of the DD equations which is still in use today. However, as semiconductor devices were scaled into the submicrometer regime, the assumptions underlying the DD model lost their validity. Therefore, the transport models have been continuously refined and extended to more accurately capture transport phenomena occurring in these devices.

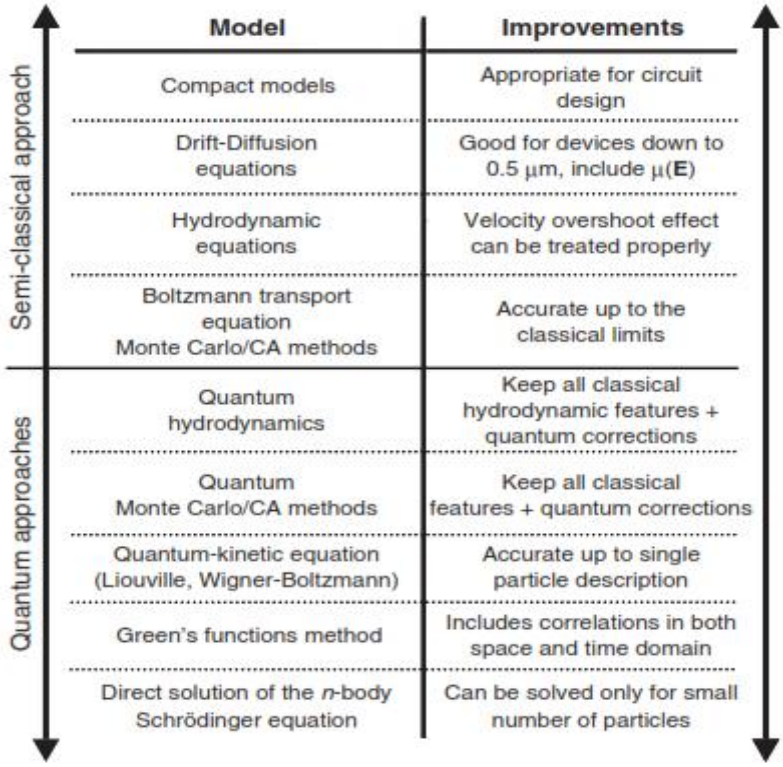


Figure A.1: Illustration of the hierarchy of transport models.

As the supply voltages cannot be scaled accordingly without jeopardizing the circuit performance, the electric field inside the devices has increased. A large electric field, which rapidly changes over small length scales, gives rise to non-local and hot-carrier effects which begin to dominate device performance. An accurate description of these phenomena is required and is becoming a primary concern for industrial applications.

To overcome some of the limitations of the DD model, extensions have been proposed which basically add an additional balance equation for the average carrier energy. Furthermore, an additional driving term is added to the current expression which is proportional to the gradient of the carrier temperature. However, a vast number of these models exist, and there is a considerable amount of confusion such as their relation to each other.

It is now a common practice in industry to use standard hydrodynamic models in trying to understand the operation of as-fabricated devices, by adjusting any number of phenomenological parameters (example: mobility, impact ionization coefficient).

A.II. Some helpful electron transport model definitions

A. II.1 Boltzmann's transport equation:

The Boltzmann equation expresses the general electron transport characteristics of two dimensional system containing many scattering centers in terms of a balance between acceleration, due to the Lorentz force, and deceleration, due to collisions with the scattering centers[Ashcroft and Mermin; 1976, Ziman; 1975].

If the electron system in equilibrium and no electric or magnetic fields present, the electrons will be distributed according to the Fermi-Dirac function. At low temperature the occupied states fill the Fermi circle as shown in figure.A.3, which is centred around $k = (k_x,k_y) = 0$, This distribution has no net momentum and therefore no net current flows.

When electric and magnetic field are switched on, the electrons will be accelerated by Lorentz force. An electron initially in a state k with velocity v_k will receive acceleration:

$$\frac{\partial v_k}{\partial t} = \frac{\hbar}{m^*}\frac{dk}{dt} = \frac{q}{m^*}\left(E + v_k \wedge B\right) \tag{A.1}$$

where q is the electron charge, E the electric field, B the magnetic field, m^*, are the effective mass and $\hbar$ Planck constant.

This acceleration will cause the electron distribution f to evolve in time $f \rightarrow f(k,t)$

The distribution function is $f(k,t)d^2k/(2\circledR)^2$ defined as the average number of electrons occupying the infinitesimal volume of k-space d^2k around wave vector k at time t.with quantifying the evolution of f with thinking of the acceleration dk/dt as velocity in k-space. This concept is illustrated in figA.2. any electrons occupying a small volume of k-space around wave vector k (box1) with velocity $\dot{k}$ at time t will move so that they are in a small volume of k-space around $k'=k+\dot{k}dt$ (box2) at time $t+dt$. This implies that:

$$f(k,t) = f\left(k + \dot{k}\,dt, t + dt\right) \tag{A.2}$$

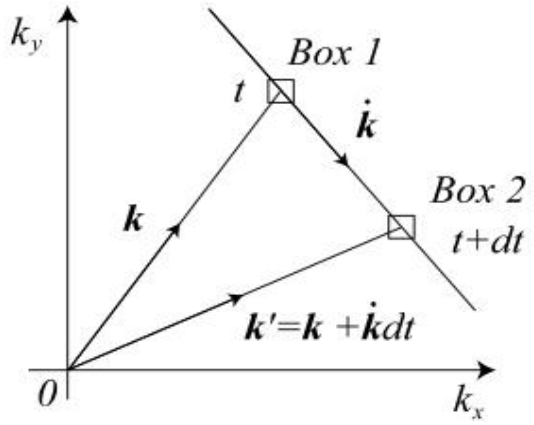


Figure: A.2: Motion in k-space du to the Lorentz Force.

If the change in *f* is a small perturbation on f_0, and that the small application of small magnetic and electric fields will not alter the system significantly. We can make a Taylor expansion of the last equation. To the first order in *dt* this is:

$$\approx f(k,t) + \nabla_k f . \dot{k}\, dt + \frac{\partial f}{\partial t} dt$$

$$0 = \nabla_k f . \dot{k} + \frac{\partial f}{\partial t} \tag{A.3}$$

So that the rate of change f with respect to time from the Lorentz force has the form:

$$\left.\frac{\partial f}{\partial t}\right|_{lorentzforce} = -\nabla_k f . \dot{k} \tag{A.4}$$

If the acceleration of electrons in the system ran unchecked by any mechanism, the assumption that the new distribution function is a small perturbation on the zero field distribution would certainly be wrong. In real systems there are many compensating factors:
(1) Electrons may scatter from impurities or crystal defects. At low temperatures this is typically the dominant mechanism.
(2) They can scatter from phonons. This mechanism becomes dominant at higher temperatures.
(3) They can collide with each other since they are charged particles.
After switching on the electric and magnetic fields for a short time an excess distribution given by:

$$g(k,t) = f(k,t) - f_0(k) \tag{A.5}$$

will build up. If the fields are then switched we will expect that this excess distribution will decay away through collision processes at a rate proportional to the excess

$$\left.\frac{\partial g(k,t)}{\partial t}\right|_{coll} = -\frac{g(k,t)}{\tau_k} \tag{A.6}$$

The characteristic time for this decay to occur τ_k is referred to as the relaxation time. Since the initial distribution function f_0 is independent of time, the time derivative of equation.A.5 gives

$$\left.\frac{\partial g(k,t)}{\partial t}\right|_{coll} = \left.\frac{\partial f(k,t)}{\partial t}\right|_{coll} \tag{A.7}$$

Equation A.6 describes what is known as the time approximation. If one thinks of the detailed quantum mechanical multiple scattering between impurities that must occur at low temperatures, where phase coherence becomes important, this approximation will clearly break down.

Now, we have two different mechanisms that cause the electron distribution to change: the Lorentz force which tends to accelerate conduction electrons; and collisions which tend to decelerate them. Under the application of small electric fields the two-dimensional electron gas can therefore find a new dynamic equilibrium

$$\left.\frac{\partial f(k,t)}{\partial t}\right|_{lorentzforce} + \left.\frac{\partial f(k,t)}{\partial t}\right|_{coll} = 0 \tag{A.8}$$

Substituting equations A.1,A.4-A.6 into A.8, one can get the nonlinear Boltzmann equation as follow:

$$\nabla_k (g + f_0).\frac{q}{\hbar}(E + v_k \wedge B) = \frac{g}{\tau_k} \tag{A.9}$$

Equation A.9 is the nonlinear first order partial equation in *g*. If we expand the bracket in the last equation, the first term is:

$$\nabla_k f_0 . \frac{q}{\hbar} v_k \wedge B = 0 \tag{A.10}$$

It is equal zero because

$$\nabla_k f_0 = \frac{\partial f_0}{\partial t}\hbar v_k \tag{A.11}$$

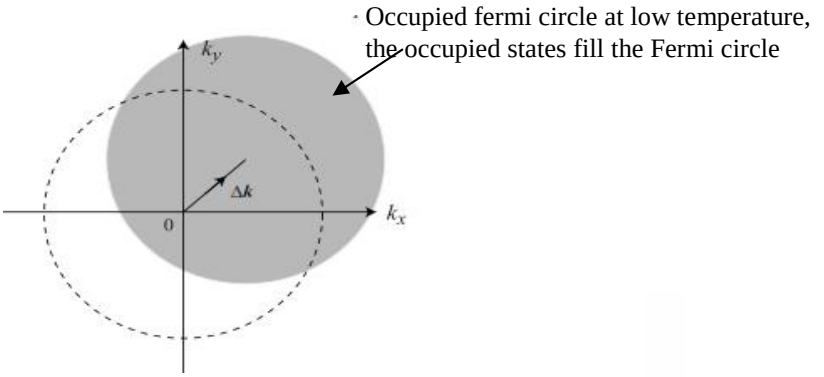


Figure A.3: Shift of the Fermi circle owing to external electric field $\Delta k = -q\tau E/\hbar$.

and $v_k . v_k \Lambda B = 0$. The second term is nonlinear term $\nabla_k g . \frac{q}{\hbar} E$

It is nonlinear because it is a product of the electric field E and the excess distribution g that the electric field produces. Removing these terms results in the linear Boltzmann equation:

$$\nabla_k g . \frac{q}{\hbar} v_k \wedge B + \nabla_k f_0 . \frac{q}{\hbar} E = \frac{g}{\tau_k} \tag{A.12}$$

It will be valid if the excess distribution g is small. In zero magnetic field the solution to the linear Boltzmann equation is trivial since the only term containing a derivative is multiplied by the magnetic field B. The solution is:

$$g(k) = \frac{q^2 \tau_k}{\hbar} \nabla_k f_0 . E \tag{A.13}$$

Substituting equation A.5, one can get

$$f = f_0 + \frac{q^2 \tau_k}{\hbar} \nabla_k f_0 . E \tag{A.14}$$

With the assumption that the relaxation time τ_k is constant $\tau_k = \tau$. The last equation yields a very simple picture of transport in a two-dimensional system. The equation.A.14 may rewrite to the same order of approximation as:

$$f = f_0 \left(k + \frac{q^2 \tau_k}{\hbar} E \right) \tag{A.15}$$

This equation indicates that under the influence of an electric field the new dynamic equilibrium is represented by shifting the zero-field Fermi circle in the opposite direction to

the applied electric field (opposite since electronic charge is negative) by an amount $\Delta k = -q\tau E/\hbar$ in k-space. This is shown Figure.A.3, this shift may be viewed as each electron picking up an additional drift velocity v_d owing to the influence of the electric field. This drift velocity is defined by:

$$\frac{m^* v_d}{\hbar} = \Delta k = -\frac{q^2}{\hbar} E \tag{A.16}$$

From this equation it is clear that the longer the relaxation time τ the larger the drift velocity v_d will be for a given electric field E. Using equation.A.16 the electron mobility μ can be written:

$$\mu = \frac{|v_d|}{|E|} = \frac{q^2}{m^*} \tag{A.17}$$

Mobility is a measure of the purity of a system. For example, good electron mobilities in GaAs-AlGaAs hetero-structures are μ = 50 $m^2/Vs \rightarrow 1000 m^2/Vs$. This implies relaxation times of τ= 19 ps →380 ps and typical drift velocities in a low temperature measurement of $|v_d|$= 0.6 $ms^{-1} \rightarrow 12.5\ ms^{-1}$ assuming a 1mV potential difference across an 80 μm sample.

Remark

The position vector **r** has dimensions of length, the ***k***-vector has dimensions of reciprocal length, so ***k*** is the frequency analogue of ***r***. Physical phenomena can be described using either the positions of particles, or their moment. Both formulations equivalently provide the same information about the system in consideration. Usually ***r*** is more intuitive and simpler than ***k***, so in the following section, the position vector ***r*** will be used rather than ***k***.

A.II.2 The drift diffusion model

For traditional semiconductor device modeling, the predominant model corresponds to solutions of the so-called drift-diffusion equations, which are 'local' in terms of the driving forces (electric fields and spatial gradients in the carrier density), i.e., the current at a particular point in space only depends on the instantaneous electric fields and concentration gradient at that point. The complete drift-diffusion model is based on the following set of equations:

(1) Current equations for each carrier type is:

$$J_n(r,t) = qn(r,t)\mu_n E + qD_n \frac{\partial n(r,t))}{\partial r}$$

$$J_p(r,t) = qp(r,t)\mu_p E - qD_p \frac{\partial p(r,t))}{\partial r} \quad \text{(A.18)}$$

(2) The Continuity equations are so deduced:

$$\frac{\partial n(r,t)}{\partial t} = \frac{1}{q}\frac{\partial}{\partial r} J_n(r,t) + U_n$$

$$\frac{\partial p(r,t)}{\partial t} = -\frac{1}{q}\frac{\partial}{\partial r} J_p(r,t) + U_p \quad \text{(A.19)}$$

(3) Poisson's equation

$$\nabla.(\pounds\nabla\ddot{}) = -(p(r,t) - n(r,t) + N_d^+(r,t) - N_a^-(r,t)) \quad \text{(A.20)}$$

Where μ_n, μ_p are the mobilities for the electron and hole respectively and D_n, D_p are the diffusion coefficients, $U_{n,p}$ are the net generation-recombination rates. ε is the permittivity and φ is the electrostatic potential. The continuity equations are the conservation laws for the charge carriers, which may be easily derived taking *the zeroth moment* of the time dependent BTE. A numerical scheme which solves the continuity equations should:

1. Conserve the total charge inside the device, as well as that entering and leaving.

2. Respect the local positive definite nature of carrier density. Negative density is unphysical. 3. Respect monotonicity of the solution (i.e. it should not introduce spurious space oscillations).

Conservative schemes are usually achieved by subdivision of the computational domain into patches (boxes) surrounding the mesh points. The currents are then defined on the boundaries of these elements. Thus, enforcing conservation (the current exiting one element side is exactly equal to the current entering the neighboring element through the side in common). In the absence of generation recombination terms, the only contributions to the overall device current arise from the contacts. And since electrons have negative charge, the particle flux is opposite to the current flux. When the equations are discretized, using finite differences for instance, there are limitations on the choice of mesh size and time step:

(1) The mesh size Δx is limited by the Debye length.

(2) The time step is limited by the dielectric relaxation time.

A mesh size must be smaller than the Debye length where one has to resolve charge variations in space. A simple example is the carrier redistribution at an interface between two regions with different doping levels. Carriers diffuse into the lower doped region creating excess carrier distribution which at equilibrium decays in space down to the bulk concentration with approximately exponential behavior. The spatial decay constant is the Debye length.

$$L_D = \sqrt{\frac{£K_B T}{q^2 N}} \tag{A.21}$$

where N is the doping density. In GaAs and Si, at room temperature the Debye length is approximately 400 Å when $N \sim 10^{16}$ cm^{-3}and decreases to about only 50 Å when $N \sim 10^{18}$cm^{-3}. The dielectric relaxation time, on the other hand, is the characteristic time for charge fluctuations to decay under the influence of the field that they produce. The dielectric relaxation time may be estimated using

$$²_{dr} = \frac{£}{qN\mu} \tag{A.22}$$

The drift-diffusion semiconductor equations constitute a coupled nonlinear set. It is not possible, in general, to obtain a solution directly in one step, but a nonlinear iteration method is required. The two most popular methods for solving the discretized equations are the Gummel's iteration method [Gummel; 1964] and the Newton's method [Apostol; 1969]. It is very difficult to determine an optimum strategy for the solution, since this will depend on a number of details related to the particular device under study. Finally, the discretization of the continuity equations in conservation form requires the determination of the currents on the mid-points of mesh lines connecting neighboring grid nodes. Since the solutions are accessible only on the grid nodes, interpolation schemes are needed to determine the currents. The approach by Scharfetter and Gummel [Scharfetter and Gummel; 1969] has provided an optimal solution to this problem, although the mathematical properties of the proposed scheme have been fully recognized much later.

A.II.3 Deriving hydrodynamic equations from the Boltzmann equation

As the Boltzmann equation describes the evolution of distribution function of particles Gas over a time intervals Δt superior at the characteristic period of collision and much less than the relaxation time τ. At this step where ($\Delta t \ll \tau$) the hydrodynamic model is convenient. The Gaz is then described by the average (density, velocity and energy).

The hydrodynamic model takes into account the carrier's acceleration under the external forces and it can simulate the submicron- structures as well as a transition phenomena. In this approach the energy relaxation *w* of the carries will be described. The evolution in time and space of w, *n* the density and the *v* velocity are described with taking the three first order of moment's method, thus, the model is macroscopic approach.

Firstly, we can take the equation A6 for the distribution function and make a Taylor expansion of with using *r* position. To the first order in *dt* this is:

$$\frac{\partial f(r,v,t)}{\partial t}+\frac{\partial r}{\partial t}\frac{\partial f(r,v,t)}{\partial r}+\frac{\partial v}{\partial t}\frac{\partial f(r,v,t)}{\partial v}=\left.\frac{\partial f(r,v,t))}{\partial t}\right|_{coll} \tag{A. 23}$$

with $\frac{\partial r}{\partial t}=v\ and\ \frac{\partial v}{\partial t}=\frac{F}{m^*}=\frac{-qE}{m^*}$, substituting these last parameters into equation A.23 taking into account the equation A.6,7, the equation A.23 will be as:

$$\frac{\partial f(r,v,t)}{\partial t}+v\frac{\partial f(r,v,t)}{\partial r}-\frac{qE}{m^*}\frac{\partial f(r,v,t)}{\partial v}=-\frac{f(r,v,t)-f_0(r,v,t)}{\tau} \tag{A.24}$$

The transition from the Boltzmann equation A.24 to the density, velocity and energy equations is done through the moments method by multiplied the Boltzmann equation by V^m, where m is order moment index.

$$\frac{\partial}{\partial t}\int_v f(r,v,t)d^3v+\frac{\partial}{\partial r}\int_v f(r,v,t)vd^3v-\frac{qE}{m^*}[f]_{-\infty}^{+\infty}=-\int_v\frac{f(r,v,t)}{\tau}d^3v-\int_v\frac{f_0(r,v,t)}{\tau}d^3v \tag{A.25}$$

Since the electronic velocity is a finite value, the occupation probability of the state $|r,v\rangle$ tends to zero when$|v|$ tends to infinity, in fact $|f|_{-\infty}^{+\infty}=0$ and as:

$$n=\int_v f(r,v,t)d^3v$$
$$v=\frac{\int_v vf(r,v,t)d^3v}{\int_v f(r,v,t)d^3v} \tag{A.26}$$

The zero moment equation is given as follow:

$$\frac{\partial n(r,t)}{\partial t}+\frac{\partial}{\partial r}\left(n(r,t)\bar{v}(r,t)\right)=-\frac{n(r,t)-n_0}{\tau_n} \tag{A.27}$$

where n_0 is the electron density at thermodynamic equilibrium and τ_n is the relaxation time of electron density. Assuming that the generation and recombination terms are neglected, the electron density can be given as:

$$\frac{\partial n}{\partial t} + \frac{\partial}{\partial r}(n\bar{v}) = 0 \tag{A.28}$$

In general case, we can define **A(r,v,t)** as moment function. Its equation is given by

$$\begin{aligned}&\bar{A}(r,t)\frac{\partial n(r,t)}{\partial t} + n(r,t)\frac{\partial \bar{A}(r,t)}{\partial r} + \frac{\partial}{\partial r}n(r,t)\overline{A(r,t)v(r,t)} - \frac{qE}{m^*}n(r,t)\frac{\partial \overline{A(r,t)}}{\partial v}\\ &= \frac{\bar{A}(r,t) - A_0(r,t)}{\tau_A}n(r,t)\end{aligned} \tag{A.29}$$

By associating the continuity equation and making some developments, one can get the following expression:

$$\begin{aligned}&\frac{\partial \bar{A}(r,t)}{\partial t} + \bar{v}(r,t)\frac{\partial \bar{A}(r,t)}{\partial r} + \frac{1}{n(r,t)}\frac{\partial}{\partial r}n(r,t)\left[\overline{A(r,t)v(r,t)} - \bar{A}(r,t)\bar{v}(r,t)\right] - \frac{qE}{m^*}n(r,t)\frac{\partial \overline{A(r,t)}}{\partial v}\\ &= \frac{\overline{A(r,t)} - A_0(r,t)}{\tau_A}\end{aligned} \tag{A.30}$$

Substituting the first order moment, which is the velocity, we can get:

$$\frac{\partial \overline{v(r,t)}}{\partial t} + \bar{v}(r,t)\frac{\partial \bar{v}(r,t)}{\partial r} + \frac{1}{n(r,t)}\frac{\partial}{\partial r}n(r,t)\left[\overline{v^2(r,t)} - \bar{v}^2(r,t)\right] - \frac{qE}{m^*} = \frac{\bar{v}(r,t)}{\tau_v} \tag{A.31}$$

where τ_v is the velocity time relaxation. **The first order moment** known as the velocity conservation equation can be written as:

$$\frac{\partial \bar{v}}{\partial t} + \bar{v}\frac{\partial \bar{v}}{\partial r} + \frac{1}{n}\frac{\partial}{\partial r}n\left[\overline{v^2} - \bar{v}^2\right] - \frac{qE}{m^*} = \frac{\bar{v}}{\tau_v} \tag{A.32}$$

If we put: $A = \mathcal{E} = \frac{1}{2}m^*v^2$

The moments method applied to the second order moments gives:

$$\frac{\partial \overline{\mathcal{E}(r,t)}}{\partial t} + \bar{v}(r,t)\frac{\partial \bar{\mathcal{E}}(r,t)}{\partial r} + \frac{1}{n(r,t)}\frac{\partial}{\partial r}n(r,t)\left[\overline{v(r,t)\mathcal{E}(r,t)} - \bar{v}(r,t)\mathcal{E}(r,t)\right] - \frac{qE}{m^*}\frac{\partial \bar{\mathcal{E}}(r,t)}{\partial r} = \frac{\bar{\mathcal{E}}(r,t) - \mathcal{E}_0}{\tau_{\mathcal{E}}} \tag{A.33}$$

This last equation is the **third moment** which is the energy conservation equation and has the following expression:

$$\frac{\partial \bar{v}}{\partial t} + \bar{v}\frac{\partial \bar{v}}{\partial r} + \frac{1}{n}\frac{\partial}{\partial r}n\left[\overline{v\mathcal{E}} - \bar{v}\bar{\mathcal{E}}\right] - \frac{qE}{m^*}\frac{\partial \bar{\mathcal{E}}}{\partial v} = \frac{\bar{\mathcal{E}} - \mathcal{E}_0}{\tau_\varepsilon} \tag{A.34}$$

with $\frac{\partial \bar{\mathcal{E}}}{\partial v} = m^* \bar{v}$ and τ_ε is the energy relaxation time.

The equations system A.27, A.32 and A.34 has three unknowns $n(r,t), \bar{v}(r,t)$ and $\bar{\mathcal{E}}(r,t)$ and six parameters $m^*, \tau_n, \tau_v, \tau_\varepsilon, \overline{\delta v^2}$ and $\overline{\delta v \delta \mathcal{E}}$ which have to be correctly defined.

With the assumption that these parameters are only dependent on the average local energy at a given point and the relations which link these parameters to the energy are expressed in the same manner such as the case of homogeneous material in stationary state. So, the relaxation time of the velocity and energy will be obtained by cancellation of the spatial and temporal derivatives in the equation A27 and A.30, thus,

$$\tau_v = \frac{\bar{v} m^*}{qE} \tag{A.35}$$

and

$$\tau_\varepsilon = \frac{\bar{\mathcal{E}} - \mathcal{E}_0}{qE\bar{v}} \tag{A.36}$$

where ε_0 is the average energy at zero field.

These parameters are the input data of the hydrodynamic model. They are obtained as function of material parameters and calculated by the microscopic Monte Carlo simulation.

A.III Monte Carlo Method

Monte Carlo is a statistic approach to solve the problems which not necessary have to be random. In microelectronic case and especially in the electronic transport simulation of the semiconductor, this method permit to model the partical displacement as free flight sequences interrupted by collisions.

In order to solve the transport equation, Monte Carlo method decomposed the carrier trajectories in large number of sequence as illustrated in Figure A.4, each sequence started by a free flight during which the particle moves under field of exterior force (Newton Law). This free flight followed by a collision or interaction of the carriers and the lattice.

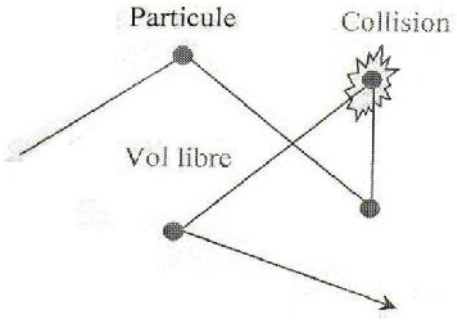


Figure A.4: Illustration of particle trajectory.

To generate such random sequences, it must:

- Randomly select the duration of free flight;
- Randomly select the type of interaction experienced at the end of free flight and its effect.

A large number of particles is simulated and the ensemble motion gives the macroscopic characteristics: drift velocity, the average mobility and energy. The simulation may be more accurate as the number of particles is large. The choice of the representation of dispersion relations and interaction frequency is the heart of the physical modelling of transport simulation. Firstly, we will describe the trajectory during the free flight then we detailed the calculation of frequency interaction. The problem is simply to determine the evolution of the wave vector *K(t*) under the action of external forces *F* during the free flight, which means to resolve the fundamental dynamic equation given by:

$$\frac{d\vec{K}(t)}{dt} = \frac{\vec{F}}{\hbar} \tag{A.37}$$

During one step and *Δt*, *F* remains constant and the wave vector after the movement is $\vec{K}(t+\Delta t)$ is given as:

$$\vec{K}(t+\Delta t) = \vec{K}(t) + \frac{\Delta t}{\hbar}\vec{F} \tag{A.38}$$

The carrier which is in no parabolic band with wave vector *k(t)* has a movement quantity and kenitic energy as follow :

$$¥(£) = £(1+\sim£) = \frac{\hbar^2 K^2}{2m^*} \tag{A.39}$$

$$£(t) = \frac{\left(\left(1+\frac{2\sim\hbar^2 K^2}{m^*}\right)^{\frac{1}{2}} - 1\right)}{2\sim} \tag{A.40}$$

where $\hbar$ denotes the Plank constant is the non-parabolicity coefficient. The carrier move with the group velocity $\vec{v}$ given as:

$$\vec{v}(t) = \frac{\hbar \vec{K}(t)}{m^*(1+2\sim\pounds(t))} \tag{A.41}$$

and accelerated by the wave vector variation which was defined by Newton under the effect of the electrical field *E*.

$$\frac{d\vec{K}}{dt} = \frac{1}{\hbar} q\vec{E} \tag{A.42}$$

This permit to describe the equation A.36 under the following expression:

$$\vec{K}(t+\Delta t) = \vec{K}(t) + \frac{\Delta t}{\hbar}\vec{E} \tag{A.43}$$

Thus, Monte Carlo simulation of the mean free path of the carriers is to calculate the final state as function of the initial state, and consider it as a new initial state to calculate the final state after.

Appendix B
Defining terms

Bias voltage or current: The DC power applied to a transistor allowing it to operate as an active amplifying or signal-generating device. Typical voltage levels in GaAs FETs used in receivers are 1 to 7 volts between the drain and source terminals, and 0 to –5 volts between the gate and source terminals. For microwave systems, DC voltages and currents provided by batteries or AC/DC converters required to bias transistors to a region of operation where they will either amplify, mix or frequency translate, or generate (oscillators) microwave energy. Since energy can be neither created or destroyed, microwave energy amplification or creation is accomplished at the expense of DC energy.

DC: Direct current/voltage: Constant voltage or current with no variation over time. This can be considered in general terms as an alternating current/voltage (AC) with a frequency of variation of zero, or a zero frequency signal. For microwave systems, DC voltages and currents, provided by batteries or AC/DC converters required to bias transistors to a region of operation where they will either amplify, mix or frequency translate, or generate (oscillators) microwave energy.

FET: Field Effect Transistor: The MESFET (Metal-Electrode-Semiconductor-Field-Effect-Transistor) is a specific type of FET that is the dominant active (amplifying) device in GaAs MMICs. A FET is composed of three terminals called the gate, drain, and source, and a conducting "channel." In an amplifier application, the source is connected to ground, and DC bias is applied between the drain and source causing a current to flow in the channel. The current flow is controlled and modulated by the AC or DC voltage applied to the gate.

Frequency: The repetition rate of a periodic signal used to represent or process a communication signal. Frequency is expressed in units of Hertz (Hz). One Hz represents one cycle per second, 1 MHz represents one million cycles per second, and 1 GHz represents one billion cycles per second. Gain: Ratio of the output signal over the input signal of a component.

Ku-Band: Frequency band of approximately 11 to 12 GHz.

L-Band: Frequency band of approximately 1 to 2 GHz.

Microwave: Term used to refer to a radio signal at a very high frequency. One broad definition gives the microwave frequency range as that from 300 MHz to 300 GHz.

MMIC: Monolithic Microwave Integrated Circuit, in the word monolith refers to a single block of stone that does not (in general) permit individual variations. MMICs are made of

gallium arsenide (GaAs), silicon, or other semiconducting materials. In a MMIC, all of the components needed to make a circuit (resistors, inductors, capacitors, transistors, diodes, and transmission lines) that are formed onto a single wafer of material using a series of process steps. Attractive features of MMICs over competing hybrid (combination of two or more technologies) circuits are that a multitude of nearly identical circuits which can be processed simultaneously with no assembly (soldering) using batch processing manufacturing techniques. The main disadvantage is that circuit adjustment after manufacture is difficult or impossible. As a consequence, significantly more effort is required to use accurate computer-aided design (CAD) techniques to design MMICs that will perform as desired without adjustment. Of course, eventually assembly and packaging of MMICs is performed in order to connect them into a system such as a DBS receiver (Direct broadcast satellite (DBS) is a term used to refer to satellite television broadcasts intended for home reception). MMICs are only cost effective for very high volume applications because the cost of the initial design is very high, as is the cost of wafer manufacture. These costs can only be recovered through high volume manufacture.

Noise: Random perturbations/distortions in signal voltage, current, or power.

Noise figure: Property of a microwave component that describes the amount of noise added to a signal passing through the component. Technically defined as the signal-to-noise ratio at the component input to the signal-to-noise ratio at the component output. For a transistor, the noise figure is highly dependent on the impedance the transistor sees when it looks back at the input matching network from its input (gate for FET) terminal. The minimum noise figure F_{min} is the lowest noise figure that a FET can exhibit under optimum input impedance matching conditions (Z_{opt} or in terms of reflection coefficient G_{opt}). Noise figure is usually specified in decibels.

Package: In MMIC technology, die or chips have to ultimately be packaged to be useful. An example opt of a package is the T07 "can." The MMIC chip is connected within the can with bond wires connecting from pads on the chip to lead pins on the package. The package protects the chip from the environment and allows easy connection of the chip with other components needed to assemble an entire system, such as a DBS TV receiver.

Radio frequency RF: A general term used to refer to radio signals in the general frequency range from thousands of cycles per second (kHz) to millions of cycles per second (MHz). Also, it is often used generically and interchangeably with the term microwave to distinguish the high frequency AC portion of a circuit or signal from the DC bias signal or the down converted intermediate frequency (IF) signal.

Large-signal modeling is a common analysis method used to describe nonlinear devices in terms of the underlying nonlinear equations. In circuits containing nonlinear elements such as transistors, diodes, and vacuum tubes, under "large signal conditions", AC signals have high enough magnitude that nonlinear effects must be considered. Large signal is the opposite of small signal, which means that the circuit can be reduced to a linearized equivalent circuit around its operating point with sufficient accuracy. The differences between small signal and large signal is that, the small signal model takes a circuit and based on an operating point (bias) and linearizes all the components. Nothing changes because the assumption is that the signal is so small that the operating point (gain, capacitance etc.) doesn't change. A large signal model on the other hand, takes into account the fact that the large signal actually affects the operating point and takes into account that elements are non-linear and that circuits can be limited by power supply values.

Delta doped: formation of the doped layers which are atomic-layer thick; formed in the course of Molecular Beam Epitaxy (MBE) of multilayer structures such as superlattices.

The doping distributions in semiconductors are scaled down in one dimension to their ultimate spatial limit. This limit will be reached if the dopants are confined to a single or few monolayers of the semiconductor lattice. The thickness of the doped region is comparable to the lattice constant, i.e., only few angstroms thick. The doping distribution is then narrower than other relevant length scales, most importantly the free carrier de Broglie wave-length. Such narrow doping profiles can be mathematically described by Dirac's delta function. Semiconductors with such dopant distributions will be referred to as δ-doped semiconductors.

Superlattices: semiconductor structure is comprising of several ultra-thin layers (atomic layers) engineered to obtain specific electronic and photonic properties. Slight modifications of chemical composition of each layer result in slight variations of energy bandgap from layer to layer: bandgap engineering; fabrication of superlattices requires high-precision heteroepitaxial deposition methods such as MBE and MOCVD; typically involves III-V semiconductors.

Velocity overshoot is a result of transit times of a charge carrier going from source to drain being smaller than the time required to emit an optical phonon. The velocity therefore exceeds the saturation velocity, which leads to faster field-effect transistor switching. This notion is utilized when the gate length is reduced to increase the switching speed.

Breakdown voltage BV_{gd} is gate-drain breakdown voltage which is one of the important parameters Field Effect Transistors. Presently, the BV_{gd} of domestic GaAs MESFET is only

more than 10V, which limits the output power of GaAs MESFET. Improving the BV_{gd} and meliorating the power characteristics have the important field focuces by researchers

pHEMT: GaAs-based high-electron mobility transistors (HEMTs) and pseudomorphic HEMT (or pHEMTs) are field-effect transistors. Other commonly used names for HEMTs include MODFET (modulation doped FET), TEGFET (two-dimensional electron gas FET) and SDHT (selectively doped heterojunction transistor). The basic principles of their operation are very similar to those of the MESFET. The main difference between HEMTs and MESFETs is the epitaxial layer structure where in the MESFET the electrons must transit through the doped channel, while in HEMT, the dopant channel is separated from the electrons transit channel. In the HEMT structure, compositionally different layers are grown in order to optimize and to extend the performance of the FET. For III–V semiconductors using a GaAs substrate, the common materials used are $Al_xGa_{1-x}As$ and GaAs. For most device applications, the Al_xAs mole fraction is between $0.2< x < 0.3$. The pHEMT also incorporates $In_xGa_{1-x}As$, where In_xAs is constrained to $x < 0.3$ for GaAs-based devices. These different layers form heterojunctions since each layer has a different band gap. Structures grown with the same lattice constant but different band gaps are simply referred to as lattice-matched HEMTs. Those structures grown with slightly different lattice constants are called pseudomorphic HEMTs or pHEMTs. Figure B.1 shows the band-gap energy as a function of lattice constant for the III–V semiconductors.

Substitution of InGaAs layer for GaAs as the two-dimensional electron gas channel improves transport properties due to the higher mobility InGaAs and stronger electron confinement associated with the quantum well at the heterojunction. Thus, injection of electrons back into the AlGaAs from the InGaAs is significantly reduced; thereby improving the transport properties.

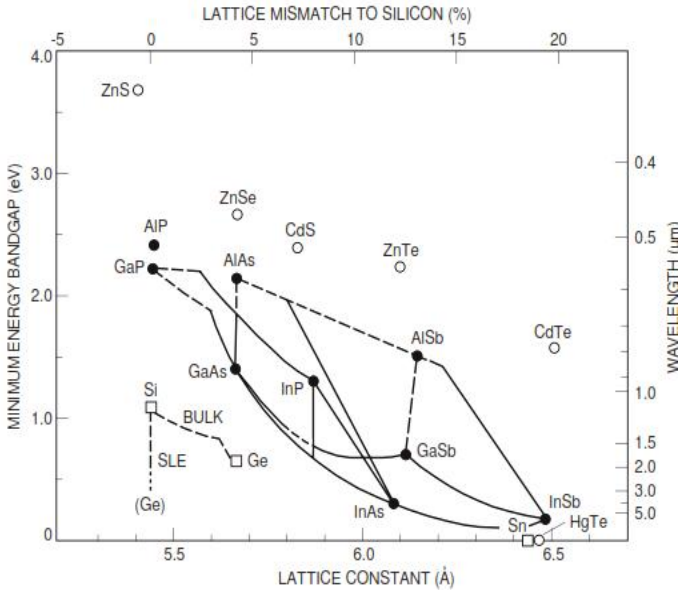


Figure B.1: Minimum bandgap energy vs lattice constant data for III–V semi-conductors. The right axis indicates the wavelengths of light that would be emitted by a laser or LED for a material of the corresponding bandgap. Connecting lines give information for alloys of the materials at the endpoints of a given line segment. Solid lines indicate a direct bandgap and dashed lines an indirect bandgap. For Ge–Si, the line denoted BULK corresponds to unstrained, lattice-mismatched growth and the line SLE to strained layer epitaxy of Ge–Si on unstrained Si [Bean; 1990].

The larger conduction band discontinuity at the AlGaAs/InGaAs heterojunction allows a higher 2DEG density and hence a higher current density and transconductance. Additionally, the electron mobility and peak velocity can be further improved by increasing the indium concentration (Figure B.2). Although InGaAs is not lattice matched to either the AlGaAs donor or the GaAs buffer layers Figure B.1, the strain associated with the lattice mismatch can be elastically accommodated within the InGaAs layer. For example, for a pHEMT structure like AlGaAs/$In_xGa_{1-x}As$/ GaAs where x is in the range of 0.15 to 0.20, the InGaAs layer must be smaller than the critical thickness ~150 Å (15 nm) . Above the critical thickness, lattice dislocations form, while for a thickness less than ~ 50 Å (5 nm), quantum size effects substantially reduce electron confinement and increase electron scattering [Coleman and Dapkus; 1985, Hoke et al; 1990].

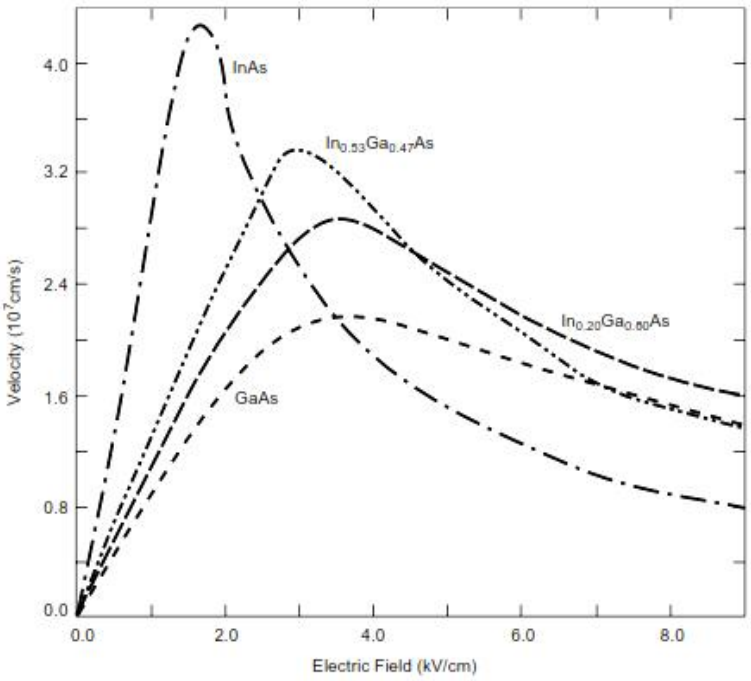


Figure B.2: Electron velocity as a function of electric field for variety of In concentrations of InGaAs [Reid; 2008].

Radio Frequency Band Designations:

IEEE Standard Radar Band Nomenclature (*IEEE Std. 521-2002, IEEE Standard Letter Designations for Radar-Frequency Bands)		
Designation	**Frequency**	**Wavelength**
HF	3 - 30 MHz	100 m - 10 m
VHF	30 - 300 MHz	10 m - 1 m
UHF	300 - 1000 MHz	100 cm - 30 cm
L Band	1 - 2 GHz	30 cm - 15 cm
S Band	2 - 4 GHz	15 cm - 7.5 cm
C Band	4 - 8 GHz	7.5 cm - 3.75 cm
X Band	8 - 12 GHz	3.75 cm - 2.50 cm
Ku Band	12 - 18 GHz	2.50 cm - 1.67 cm
K Band	18 - 27 GHz	1.67 cm - 1.11 cm
Ka Band	27 - 40 GHz	1.11 cm - .75 cm
V Band	40 - 75 GHz	7.5 mm - 4.0 mm
W Band	75 - 110 GHz	4.0 mm - 2.7 mm
mm Band	110 - 300 GHz	2.7 mm - 1.0 mm

International Telecommunications Union (ITU)_Radar Band Nomenclature (ITU classifications are based on region-2 radiolocation service allocations)	
Band Designation	**Frequency**
VHF	138 - 144 MHz 216 - 225 MHz
UHF	420 - 450 MHz 890 - 942 MHz
L	1.215 - 1.400 GHz
S	2.3 - 2.5 GHz 2.7 - 3.7 GHz
C	5.250 - 5.925 GHz
X	8.500 - 10.680 GHz
Ku	13.4 - 14.0 GHz 15.7 - 17.7 GHz
K	24.05 - 24.25 GHz 24.65 - 24.75 GHz
Ka	33.4 - 36.0 GHz
V	59.0 - 64.0 GHz
W	76.0 - 81.0 GHz 92.0 - 100.0 GHz
mm	126.0 - 142.0 GHz 144.0 - 149.0 GHz 231.0 - 235.0 GHz 238.0 - 248.0 GHz

Military Radar Band Designations		
Band	**Frequency**	**Wavelength**
HF	3 - 30 MHz	100 m - 10 m
VHF	30 - 300 MHz	10 m - 1 m
UHF	300 - 1000 MHz	100 cm - 30 cm
L	1 - 2 GHz	30 cm - 15 cm
S	2 - 4 GHz	15 cm - 7.5 cm
C	4 - 8 GHz	7.5 cm - 3.75 cm
X	8 - 12 GHz	3.75 cm - 2.50 cm
Ku	12 - 18 GHz	2.50 cm - 1.67 cm
K	18 - 27 GHz	1.67 cm - 1.11 cm
Ka	27 - 40 GHz	1.11 cm - .75 cm
mm	40 - 300 GHz	7.5 mm - 1.0 mm

ITU Frequency Band Nomenclature			
ITU Band	**Designation**	**Frequency**	**Wavelength**
1	ELF	3 - 30 Hz	100,000 km - 10,000 km
2	SLF	30 - 300 Hz	10,000 km - 1000 km
3	ULF	300 - 3000 Hz	1000 km - 100 km
4	VLF	3 - 30 kHz	100 km - 10 km
5	LF	30 - 300 kHz	10 km - 1 km
6	MF	300 - 3000 kHz	1 km - 100 m
7	HF	3 - 30 MHz	100 m - 10 m
8	VHF	30 - 300 MHz	10 m - 1 m
9	UHF	300 - 3000 MHz	1 m - 10 cm
10	SHF	3 - 30 GHz	10 cm - 1 cm
11	EHF	30 - 300 GHz	1 cm - 1 mm

Band Designation Acronyms
Extremely Low Frequency (ELF) Super Low Frequency (SLF) Ultra Low Frequency (ULF) Very Low Frequency (VLF) Low Frequency (LF) Medium Frequency (MF) High Frequency (HF) Very High Frequency (VHF) Ultra High frequency (UHF) Super High Frequency (SHF) Extremely High Frequency (EHF)

IEEE Std 521-2002 (IEEE Standard Letter Designations for Radar-Frequency Bands): IEEE Standard 521 reaffirms the use of letter band designations for radar frequency bands. It relates the letter designators in common usage to the frequency ranges that they represent.

Microwave Frequency Bands: The UHF (upper), SHF and EHF regions of the electromagnetic frequency spectrum are generally classified as microwave frequencies. The letter designations (L, S, C, X, Ku, K, Ka) were meant to be used for radar, but have become commonly used for other microwave frequency applications.

Key power FET parameters: An ideal RF power transistor has high breakdown voltage, high saturation current, large gain, low knee voltage and low gate leakage current.

Output power: the main output power limiting factors of typical FET are combined effects of gate conduction and reverse gate-drain breakdown [Santos et al; 2004].Considering the I-V

characteristics of hypothetical FET under large signal input power conditions, the RF drain current and voltage swings are bounded by these limiting factors at the two extremes of the RF loadline as shown in Figure B. . As the RF output signal swings to the upper left corner of I-V characteristics, the gate draws forward current and the output current wave is clipped by the gate conduction and by the channel current [Frensley; 1981].

At the other end of the loadline, the large positive drain voltage and the negative gate voltage will lead to gate-to-drain breakdown. Obviously, where the output current starts to clip first depend on the operating class (e.g. simultaneous clipping for class A operation). The approximate output power, P_{out}, is given by [Golio; 2003] as:

$$P_{out} = \frac{1}{8}(\Delta I \times \Delta V) = \frac{1}{8} I_{max}\left(BV_{gd} - V_{kee}\right) \qquad \text{(B.1)}$$

where the ΔI *and* ΔV are the RF current and voltage swing, respectively. I_{max}, $BV_{gd}$and V_{kee} are the saturation current, gate-drain breakdown voltage and knee voltage, respectively.

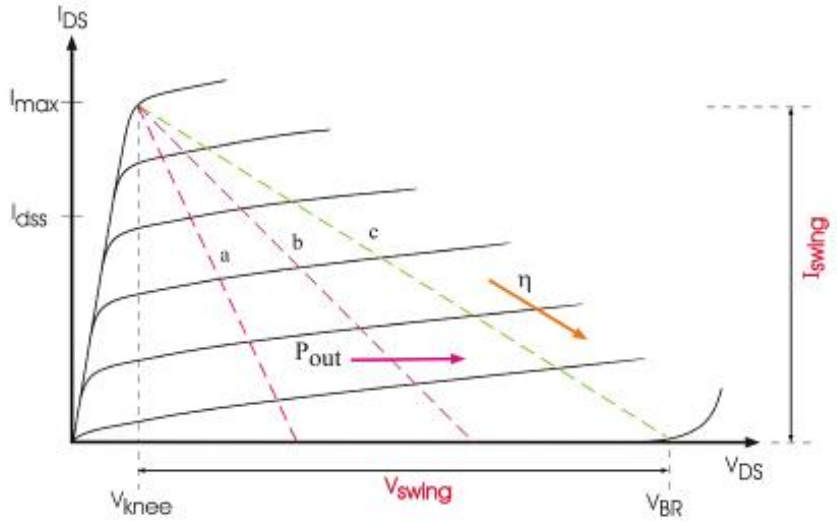


Figure B.3: loadlines for maximum output power superimposed on idealized I-V characteristics of a FET. Arrows indicate direction of output power and efficiency as function of the device operating bias point [Endalkachew; 2008].

S_{11} is the input port voltage reflection coefficient; **S_{12}** is the reverse voltage gain.
$S_{21}$is the forward voltage gain; **S_{22}** is the output port voltage reflection**.**

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