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Numerical simulation of the response of substrate traps to a voltage applied to the gate of a gallium arsenide field effect transistor

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ABSTRACT

We report on a numerical simulation of the response of substrate traps to a voltage applied to the gate of a gallium arsenide field effect transistor (GaAs FET) using proprietary simulation software. The substrate is assumed to contain shallow acceptors compensated by deep levels. The ratio between the densities of deep and shallow levels is considered to be one hundred, which is a typical value for semi-insulating substrates. Although several traps may be present in the substrate but only the most commonly observed ones are considered, namely hole traps related to Cu and Cr, and the familiar native electron trap EL2. The current–voltage characteristics of the GaAs FET are calculated in the absence as well as in the presence of the above mentioned traps. It was found that the hole traps are affected by the gate voltage while the electron trap is not. This effect on the response of hole traps is explained by the fact that the quasi-hole Fermi level in the substrate is dependent on the gate voltage. However, the electron quasi-Fermi level in the substrate is insensitive to the gate voltage and therefore electron traps are not perturbed.

1. Introduction

Gallium arsenide (GaAs) based devices such as field effect transistors (FETs), high electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs) are used in many applications in the electronics industry. GaAs FETs and HEMTs are the main components in monolithic microwave integrated circuits (MMICs), which are widely used in high speed and high frequency applications. Discrete devices as well as integrated circuits are fabricated on semi-insulating (SI) substrates, where the residual shallow donors and/or acceptors are compensated by deep-level traps. The semi-insulating property enables good isolation between adjacent devices in MMICs, and hence minimizes parasitic capacitances. However, deep-level traps in the SI substrate are believed to cause many undesirable effects in GaAs devices and circuits including drain and gate lag [1–3], frequency dispersion of conductance and transconductance [4–7], low frequency oscillation [8] and backgating [9–13]. Great efforts have been made to suppress or at least reduce substrate trapping effects for example by inserting a buried p-layer between the conducting channel and the SI-substrate [14]. However, these traps are still of great concerns for GaAs and other III–V based devices and circuits [15–17].

Unlike in simple structures, such as p–n and Schottky junctions, deep traps need not only to be identified but also accurately located in the more complicated geometry of a GaAs FET. Since its introduction in 1974 by Lang [18],

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Deep Level Transient Spectroscopy (DLTS) has become the most common method to characterise deep-level traps. A common observation in DLTS spectra of GaAs FETs is the presence of electron-like traps (deep donors) such as the nativeEL2 level and a large number of hole-like traps (deep acceptors) with large concentrations [19]. The possible location of traps in GaAs FETs can be (i) at the surface of the un-gated regions of the channel, (ii) in the channel, (iii) in the SI substrate or (vi) at the channel/SI substrate interface. However, hole-like traps are not likely to be active in the n-type channel since the hole quasi-Fermi level cannot cross their energy levels [20]. In addition, hole-like traps are not expected to be located near the channel/SI substrate interface or in the SI substrate due to the fact that there is a response to a voltage applied to the gate. Zylberstejn et al. [20] suggested that the ability of a gate voltage to disturb the population of SI-substrate related traps is due to the relative displacement of the quasi-Fermi levels in the Schottky and the channel/substrate interface regions. However, as far as the authors know, there was no attempt to elucidate this phenomenon by any means except for the analytical modelling of the drain current transient caused by a substrate trap following a pulse on the gate [21]. In Ref. [20] it was assumed that a space charge exists at the channel/SI substrate interface, and the process of trapping/de-trapping charges widens or narrows it. Previously we have used a numerical simulation to correlate the existence or absence of a backgating threshold voltage to the type of deep levels in SI substrates (acceptors or donors) [22]. In this work we use the ATLAS module of the SILVACO TCAD software [23] to investigate the effect of the different traps present in the substrate on the current–voltage characteristics of the transistor. The quasi-Fermi levels are used to explain the ability of some SI substrate traps to respond to the gate voltage. Numerical simulation has the unique feature that internal parameters, such as the potential profile, the trap occupation and the quasi-Fermi levels, can be evaluated. This, obviously, cannot be achieved by experimental work or analytical modelling.

2. Sample structure

The channel of the GaAs FET used in this work is n-type with a density of 5×10^{16} cm^{-3} shallow levels. The gate is a metal which induces a Schottky type potential barrier, assumed to be around 0.7 V, resulting from the difference between the metal and semiconductor work functions [24]. The substrate is assumed to contain shallow levels compensated by deep levels with the density of the latter exceeding that of shallow levels [25]. In this work we have considered a ratio of 100 between the densities of deep and shallow levels which is an acceptable value for typical semi-insulating substrates. Although there may exist several traps in the SI substrate we only took into account the most commonly observed ones: namely HL1, HL4 and EL2 [26,27]. HL1 and HL4 are hole-like traps and are related to Cu and Cr, respectively, while EL2 is the familiar electron trap. EL2 is a native defect which is almost present in any GaAs sample and may be its alloys like AlGaAs. More details can be found in Ref. [25]. The channel and substrate thicknesses are 0.2 and 10 μm, respectively. A two dimensional cross section along the channel of the GaAs MESFET structure used in this work is shown in Fig. 1.

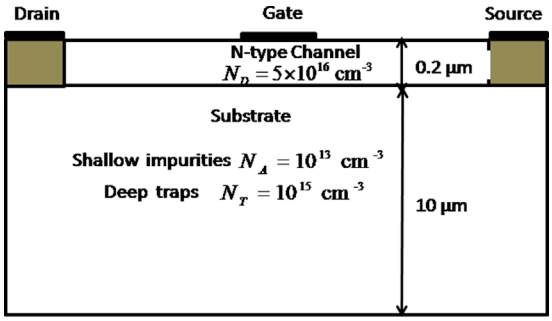

Fig. 1. A two dimensional view of the GaAs MESFET structure simulated in this work. The channel is 0.2 μm thick and doped with $N_D = 5\times 10^{16}$ donors/cm^{-3}, the substrate is 10 μm thick where shallow residual impurities $N_A = 10^{13}$ acceptors/cm^{-3} are compensated by $N_T = 10^{15}$ traps/cm^{-3}.

3. Numerical simulation

In order to characterise semiconductor devices and correlate the observed effects to each other, extensive experimental work has to be carried out. In some cases, analytical or qualitative modelling has to be used to relate these experimentally observed effects. The experimental characterisation is time consuming and can be very expensive. The analytical modelling includes several simplifications. Numerical simulation is an alternative and a powerful tool. Many parameters can be varied to model the observed phenomenon. In this present study the variables are the defects and the phenomenon is the current–voltage characteristics as well as the quasi-Fermi levels. Numerical simulation can also offer a physical explanation of the observed phenomenon since the internal parameters can be calculated including the electrical field and the free carrier densities.

The electrical characteristics of the devices are calculated using ATLAS of SILVACO. It is a physically-based two and three dimensional device simulator. It predicts the electrical behavior of specified semiconductor structures and provides insight into the internal physical mechanisms associated with device operation. The simulator is based on a mathematical model valid for any semiconductor device. This model consists of a set of fundamental equations, which link together the electrostatic potential and the carrier densities, within some simulation domain. These equations, which are solved inside any general purpose device simulator, have been derived from Maxwell's laws and consist of Poisson's equation, the carrier continuity equations and the transport equations.

The current density equations, or charge transport models, are usually obtained by applying approximations and simplifications to the Boltzmann Transport Equation. These assumptions can result in a number of different transport models. The simplest model of charge transport that is useful is the drift–diffusion model [24]. This model is adequate for nearly all devices that can be technologically fabricated. This model is based on the two first equations cited above.

The Poisson's equation which relates the electrostatic potential to the space charge density is given by

$$div(\varepsilon\nabla\psi) = -\rho \tag{1}$$

where ψ is the electrostatic potential, ε is the local permittivity, and ρ is the local space charge density.

The continuity equations for both electrons and holes are expressed as:

$$\frac{\partial n}{\partial t} = \frac{1}{q} div\vec{J_n} + G_n - R_n \tag{2.a}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} div\vec{J_p} + G_p - R_p \tag{2.b}$$

where n and p are the electron and hole concentration, $\vec{J_n}$ and $\vec{J_p}$ are the electron and hole current densities, G_n and G_p are the generation rates for electrons and holes, R_n and R_p are the recombination rates for electrons and holes, and q is the electron charge.

In steady state these equations become

$$0 = \frac{1}{q} div\vec{J_n} + G_n - R_n \tag{3.a}$$

$$0 = -\frac{1}{q} div\vec{J_p} + G_p - R_p \tag{3.b}$$

By default ATLAS includes both Eqs. (2.a) and (2.b). In some circumstances, however, it is sufficient to solve only one carrier continuity equation.

In the drift–diffusion model, the current densities are expressed in terms of the quasi-Fermi levels ϕ_n and ϕ_p as:

$$\vec{J}_n = -q\mu_n n\nabla\phi_n \tag{4.a}$$

$$\vec{J}_p = -q\mu_p p\nabla\phi_p \tag{4.b}$$

where μ_n and μ_p are the electron and hole mobilities, respectively. The quasi-Fermi levels are then linked to the carrier concentrations and the potential through the two Boltzmann approximations:

$$n = n_i \exp\left(\frac{\psi - \phi_n}{k_B T}\right) \tag{5.a}$$

$$p = n_i \exp\left(-\frac{\psi - \phi_p}{k_B T}\right) \tag{5.b}$$

where n_i is the effective intrinsic concentration and T is the lattice temperature. These two equations may then be re-written to define the quasi-Fermi potentials

$$\phi_n = \psi - \frac{k_B T}{q} \ln\frac{n}{n_i} \tag{6.a}$$

$$\phi_p = \psi + \frac{k_B T}{q} \ln\frac{p}{n_i} \tag{6.b}$$

By substituting these equations into the current density expressions, the following current relationships are obtained

$$\vec{J}_n = qD_n\nabla n - q\mu_n n\nabla\psi - \mu_n n k_B T\nabla \ln(n_i) \tag{7.a}$$

$$\vec{J}_p = -qD_p\nabla p - q\mu_p p\nabla\psi + \mu_p p k_B T\nabla \ln(n_i) \tag{7.b}$$

In (7.a) and (7.b) it is assumed that the Einstein relationship holds, that is:

$$D_n = \frac{k_B T}{q}\mu_n$$

$$D_p = \frac{k_B T}{q}\mu_p$$

The last terms in (7.a) and (7.b) account for the gradient in the effective intrinsic carrier concentration, which takes into account the bandgap narrowing effects.

The conventional formulation of drift–diffusion equations is

$$\vec{J}_n = qD_n\nabla n + q\mu_n n\vec{E}_n \tag{8.a}$$

$$\vec{J}_p = -qD_p\nabla p + q\mu_p p\vec{E}_n \tag{8.b}$$

where:

$$\vec{E}_n = -\nabla\psi - \frac{k_B T}{q}\nabla ln(n_i) \tag{9.a}$$

$$\vec{E}_p = -\nabla\psi + \frac{k_B T}{q}\nabla \ln(n_i) \tag{9.b}$$

The electrical characteristics are calculated following the specified physical structure and bias conditions. This is achieved by approximating the operation of the device onto a two dimensional grid, consisting of a number of grid points called nodes. By applying the set of differential equations (Poisson's and continuity equations) onto this grid (or equation's discretisation), the transport of carriers through the structure can be simulated. The finite element grid is used to represent the simulation domain.

Of interest to the present work, the current–voltage characteristics are calculated under different conditions (presence or absence of deep levels). ATLAS usesthe SRH (Shockley-Read-Hall) statistics for the traps as described in Refs. [28,29]. The boundary conditions for the free carrier densities are given by the ideal Ohmic contact condition at the substrate end and the Schottky barrier at the gate [30,31].

4. Results and discussion

In practical cases, the deep levels may have different densities. One way to study their response to the gate voltage is to fix the density of one of the deep levels and to vary that of the others. This is not practical since we will end up with a large number of probabilities to consider. A more practical case would be to consider that they have comparable densities. Furthermore, we will assume that the density of deep traps and shallow impurities are 10^{15} and 10^{13} cm^{-3}, respectively (these are practical values for undoped GaAs substrates [25]). In addition to the density, the trap parameters used in this work are summarised in Table 1 [26,27]. The temperature used in simulations is 300 °K.

In field effect transistors, the channel (or the drain–source) current is monitored versus either the gate or drain voltage while the other is held constant. In either case the current–voltage characteristics are calculated in

Table 1
Activation energies and capture cross sections of the traps used in this work [26,27].

Deep level	Activation energy (eV)	Capture cross (cm^2)
EL2	$E_C-0.559$	$\sigma_n=1.2\times10^{-13}$
HL1	$E_V+0.886$	$\sigma_p=1\times10^{-14}$
HL4	$E_V+0.42$	$\sigma_p=3\times10^{-15}$

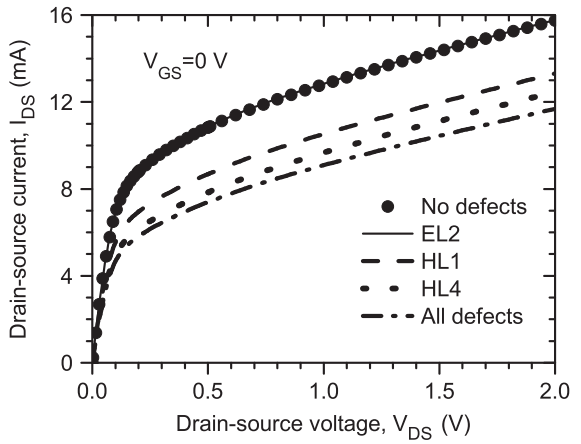

Fig. 2. The drain–source current–drain–source voltage $I_{DS}(V_{DS})$ characteristics of the GaAs MESFET under a gate-source voltage $V_{GS}=0$ V with no defects, in the presence of defects separately and together.

the: (i) absence of traps; (ii) presence of individual traps; and (iii) presence of all traps together. This approach will help elucidate the effect of each substrate trap.

The drain–source current versus the drain–source voltage with no applied gate-source voltage, in the absence and presence of the above mentioned traps (either individually or all together), are presented in Fig. 2. The curve corresponding to the electron trap EL2 (squares) coincides with the curve obtained for the case where there are no defects (solid line). Both HL1 and HL4 reduce the current with the latter having the more pronounced effect. Finally the introduction of all defects merely affects the reduction of the current, as can observed in Fig. 2 where the corresponding curve is just under the curve representing HL4. This means that the hole trap HL4 (the least deep of all defects) has the highest effect on the current.

The drain–source current versus the gate-source voltage for an applied drain–source voltage of 0.1 V, in the absence and presence of the above mentioned traps (separately and altogether), are presented in Fig. 3. Similar effects are also observed in this case, where EL2 has no influence while HL4 having the largest effect on the transistor current.

For both current–voltage characteristics the channel/SI substrate structure behaves like an n–p junction. In the absence of deep traps in the substrate the n–p junction is one sided since $N_D \gg N_A$. Therefore the spread of the depletion region is mainly in the substrate side while it is negligible in the channel side. In the presence of deep traps (two acceptors and one donor), the substrate tends to be more p-type (because of the ionised deep acceptors)

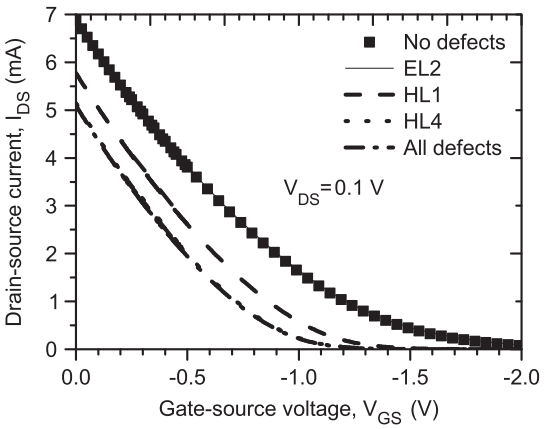

Fig. 3. The drain–source current–gate–source voltage $I_{DS}(V_{GS})$ characteristics of the GaAs MESFET under a drain–source voltage $V_{DS}=0.1$ V with no defects, in the presence of individual defects separately and together.

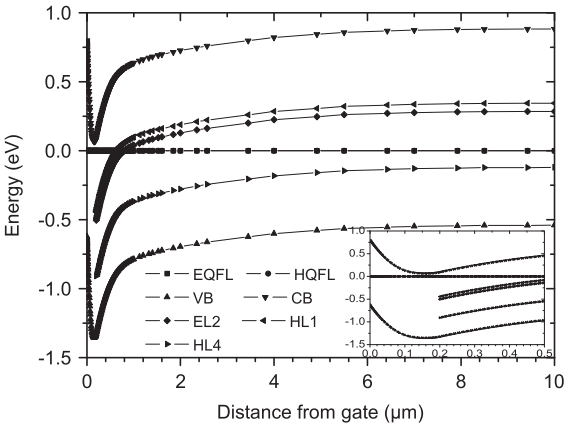

Fig. 4. The energy band diagram across the channel and the substrate of the GaAs MESFET in equilibrium showing the relative position of the defects with respect to the Fermi level. The insert is just a zoom of the channel–substrate interface region.

and therefore the spread of the depletion region in the channel will be larger than the previous case (absence of deep levels) which leads a reduction of the available channel thickness through which the current circulates. Therefore the current will be reduced since it is proportional to the channel thickness. The electron trap has no effect because it is neutral near the channel/SI substrate interface.

In order to explain this difference due to the presence of different traps, the energy position of the traps in the substrate with respect to the Fermi level is shown in Fig. 4. According to Ref. [32], it is worth pointing out that an electron trap is electrically neutral when it is occupied by electrons (below the Fermi level) and positively charged when ionised (above the Fermi level), while a hole trap is electrically neutral when it is occupied by holes (above the Fermi level) and negatively charged when ionised (below the Fermi level). This, in the opinion of the authors, is the simplest definition since it is analogous to the occupation/ionization of the conventional doping shallow levels.

Referring to Fig. 4, the electron trap EL2 is neutral in the region immediately adjacent to the channel/substrate interface. Therefore it has no effect on the charge in the channel, and consequently on the channel (transistor) current. On the other hand both hole traps are ionised in the region immediately adjacent to the channel/substrate interface. Therefore they, especially the shallower trap HL4, have a pronounced effect on the charge in the channel and on the channel (transistor) current. The insert in Fig. 4 has different scaling in the x-axis to show the region around the interface between the channel and the substrate. This is the region where most changes in the trap occupation may appear.

The ability of certain traps to respond to the gate voltage is now considered. The electron and hole quasi-Fermi levels profile across the channel and the substrate for different reverse gate biases are shown in Figs. 5 and 6, respectively. The vertical dashed line in both figures is the channel/substrate interface. In equilibrium (V_{GS}=0 V), the electron Fermi level is horizontal all along the structure as expected. As the gate reverse bias increases, the electron quasi Fermi level in the channel is disturbed by the gate voltage but not in the substrate although the gate voltage largely exceeds the pinch-off voltage. It is worth mentioning that the pinch-off voltage in the presence of all traps is estimated from Fig. 3 and has a value −1.2 V (the required gate voltage to totally deplete the channel). However, the hole quasi-Fermi (HQFL) level respond to the gate voltage in the channel as well as in the substrate. For the latter case, HQFL in the substrate is affected only when the gate voltage largely exceeds the pinch-off voltage. This is in accordance with the suggestion of Zylberstejn et al. [20] and experimental findings [21].

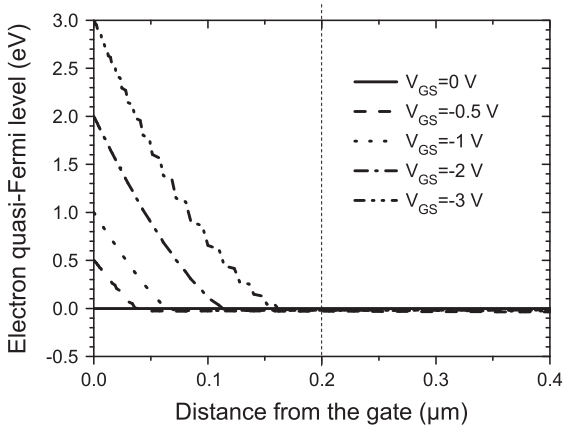

Fig. 5. The electron quasi-Fermi level across the channel and the substrate of the GaAs MESFET for different reverse biases applied to the gate. The vertical line at 0.2 μm is the interface between the channel and the substrate.

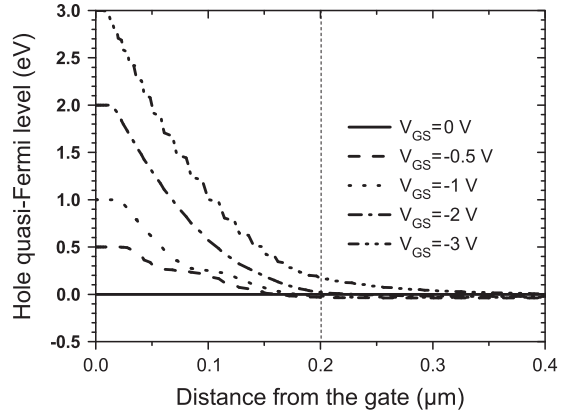

Fig. 6. The hole quasi-Fermi level across the channel and the substrate of the GaAs MESFET for different reverse biases applied to the gate. The vertical line at 0.2 μm is the interface between the channel and the substrate.

5. Conclusion

In this work we have used numerical simulation to explain why traps located in the substrate of a GaAs MESFET respond to a bias applied to the gate. To the best of our knowledge no work has been reported before to explain this phenomenon. The results can be summarised as follows: (i) the electron trap has no effect on the transistor I–V characteristics because it is neutral in the region adjacent to the channel/substrate interface; (ii) the hole traps have an effect because they are ionised near the channel/substrate interface.

The ability of certain traps in the substrate to respond to a bias applied to the gate is explained in terms of the sensitivity of the quasi-Fermi levels to this bias.

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